

[illegible]

[illegible]

ERROR:HDLParasers:821 - "C:/vhdl/NDV_DN/2024/03_WALLACE_ADD/STUDENTI/64210455/wallace
ERROR:HDLParasers:3312 - "C:/vhdl/NDV_DN/2024/03_WALLACE_ADD/STUDENTI/64210455/wallac
ERROR:HDLParasers:1209 - "C:/vhdl/NDV_DN/2024/03_WALLACE_ADD/STUDENTI/64210455/wallac
ERROR:HDLParasers:3324 - "C:/vhdl/NDV_DN/2024/03_WALLACE_ADD/STUDENTI/64210455/wallac
ERROR:HDLParasers:821 - "C:/vhdl/NDV_DN/2024/03_WALLACE_ADD/STUDENTI/64210455/wallace
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ERROR:HDLParasers:3312 - "C:/vhdl/NDV_DN/2024/03_WALLACE_ADD/STUDENTI/64210455/wallac
ERROR:HDLParasers:1209 - "C:/vhdl/NDV_DN/2024/03_WALLACE_ADD/STUDENTI/64210455/wallac
ERROR:HDLParasers:3312 - "C:/vhdl/NDV_DN/2024/03_WALLACE_ADD/STUDENTI/64210455/wallac
ERROR:HDLParasers:1209 - "C:/vhdl/NDV_DN/2024/03_WALLACE_ADD/STUDENTI/64210455/wallac

e_addition_unsigned.vhd" Line 12. Undefined symbol 'nrargs'.
e_addition_unsigned.vhd" Line 12. nrargs: Undefined symbol (last report in this block)
_addition_unsigned.vhd" Line 12. The type of the index constraint is not compatible with ArrayOfAddenc
e_addition_unsigned.vhd" Line 17. Entity wallace_addition_unsigned does not exist.
e_addition_unsigned.vhd" Line 25. Actual for index 8 is missing in array aggregate.
e_addition_unsigned.vhd" Line 52. Undefined symbol 'nrargs'.
e_addition_unsigned.vhd" Line 52. nrargs: Undefined symbol (last report in this block)
_addition_unsigned.vhd" Line 52. Deferred constant are allowed only in packages.
e_addition_unsigned.vhd" Line 53. Undefined symbol 'sizeof'.
e_addition_unsigned.vhd" Line 53. sizeof: Undefined symbol (last report in this block)
e_addition_unsigned.vhd" Line 53. Undefined symbol 'width'. Should it be: with?
_addition_unsigned.vhd" Line 53. Deferred constant are allowed only in packages.
e_addition_unsigned.vhd" Line 56. Undefined symbol 'max_sum_size'.
e_addition_unsigned.vhd" Line 56. max_sum_size: Undefined symbol (last report in this block)
e_addition_unsigned.vhd" Line 56. Undefined symbol 'std_logic'.
e_addition_unsigned.vhd" Line 56. std_logic: Undefined symbol (last report in this block)
e_addition_unsigned.vhd" Line 57. Undefined symbol 'stages'.
e_addition_unsigned.vhd" Line 57. stages: Undefined symbol (last report in this block)
e_addition_unsigned.vhd" Line 57. Undefined symbol 'cell_type'.
e_addition_unsigned.vhd" Line 57. cell_type: Undefined symbol (last report in this block)
e_addition_unsigned.vhd" Line 58. Undefined symbol 'W_type'.
e_addition_unsigned.vhd" Line 58. W_type: Undefined symbol (last report in this block)
_addition_unsigned.vhd" Line 58. The type of the element in aggregate does not correspond to any arra
e_addition_unsigned.vhd" Line 62. Undefined symbol 'std_logic_vector'.
e_addition_unsigned.vhd" Line 62. std_logic_vector: Undefined symbol (last report in this block)
e_addition_unsigned.vhd" Line 62. Undefined symbol 'n1'.
e_addition_unsigned.vhd" Line 62. n1: Undefined symbol (last report in this block)
e_addition_unsigned.vhd" Line 69. Undefined symbol 'std_logic_vector'.
e_addition_unsigned.vhd" Line 69. std_logic_vector: Undefined symbol (last report in this block)
e_addition_unsigned.vhd" Line 69. Undefined symbol 'max_sum_size'.
e_addition_unsigned.vhd" Line 69. max_sum_size: Undefined symbol (last report in this block)
e_addition_unsigned.vhd" Line 70. Undefined symbol 'std_logic'.
e_addition_unsigned.vhd" Line 70. std_logic: Undefined symbol (last report in this block)
e_addition_unsigned.vhd" Line 75. Undefined symbol 'x'.
e_addition_unsigned.vhd" Line 75. x: Undefined symbol (last report in this block)
e_addition_unsigned.vhd" Line 75. Undefined symbol 'w'.
e_addition_unsigned.vhd" Line 75. w: Undefined symbol (last report in this block)
_addition_unsigned.vhd" Line 80. - can not have such operands in this context.
e_addition_unsigned.vhd" Line 82. Undefined symbol 'nrargs'.
e_addition_unsigned.vhd" Line 82. nrargs: Undefined symbol (last report in this block)
e_addition_unsigned.vhd" Line 83. Undefined symbol 'W'.
e_addition_unsigned.vhd" Line 83. W: Undefined symbol (last report in this block)
e_addition_unsigned.vhd" Line 83. Undefined symbol 'i'.
e_addition_unsigned.vhd" Line 83. i: Undefined symbol (last report in this block)
e_addition_unsigned.vhd" Line 83. Undefined symbol 'j'.
e_addition_unsigned.vhd" Line 83. j: Undefined symbol (last report in this block)
e_addition_unsigned.vhd" Line 89. Undefined symbol 'stages'.
e_addition_unsigned.vhd" Line 89. stages: Undefined symbol (last report in this block)
e_addition_unsigned.vhd" Line 91. Undefined symbol 'k'.
e_addition_unsigned.vhd" Line 91. k: Undefined symbol (last report in this block)
_addition_unsigned.vhd" Line 94. - can not have such operands in this context.
e_addition_unsigned.vhd" Line 96. Undefined symbol 'prev_lvl_carry_rect'.
e_addition_unsigned.vhd" Line 96. prev_lvl_carry_rect: Undefined symbol (last report in this block)
e_addition_unsigned.vhd" Line 96. Undefined symbol 'width'. Should it be: with?
e_addition_unsigned.vhd" Line 96. width: Undefined symbol (last report in this block)
e_addition_unsigned.vhd" Line 97. Undefined symbol 'num_full_adders_rect'.
e_addition_unsigned.vhd" Line 97. num_full_adders_rect: Undefined symbol (last report in this block)
e_addition_unsigned.vhd" Line 107. Undefined symbol 'num_half_adders_rect'.

e_addition_unsigned.vhd" Line 107. num_half_adders_rect: Undefined symbol (last report in this block)

e_addition_unsigned.vhd" Line 107. Undefined symbol 'nrargs'.

e_addition_unsigned.vhd" Line 107. nrargs: Undefined symbol (last report in this block)

e_addition_unsigned.vhd" Line 107. Undefined symbol 'width'. Should it be: with?

e_addition_unsigned.vhd" Line 107. width: Undefined symbol (last report in this block)

e_addition_unsigned.vhd" Line 107. Undefined symbol 'i'.

e_addition_unsigned.vhd" Line 107. i: Undefined symbol (last report in this block)

e_addition_unsigned.vhd" Line 107. Undefined symbol 'k'.

e_addition_unsigned.vhd" Line 107. k: Undefined symbol (last report in this block)

e_addition_unsigned.vhd" Line 111. Undefined symbol 'W'.

e_addition_unsigned.vhd" Line 111. W: Undefined symbol (last report in this block)

e_addition_unsigned.vhd" Line 117. Undefined symbol 'this_lvl_bits_rect'.

e_addition_unsigned.vhd" Line 117. this_lvl_bits_rect: Undefined symbol (last report in this block)

e_addition_unsigned.vhd" Line 117. Undefined symbol 'nrargs'.

e_addition_unsigned.vhd" Line 117. nrargs: Undefined symbol (last report in this block)

e_addition_unsigned.vhd" Line 117. Undefined symbol 'width'. Should it be: with?

e_addition_unsigned.vhd" Line 117. width: Undefined symbol (last report in this block)

e_addition_unsigned.vhd" Line 117. Undefined symbol 'i'.

e_addition_unsigned.vhd" Line 117. i: Undefined symbol (last report in this block)

e_addition_unsigned.vhd" Line 117. Undefined symbol 'k'.

e_addition_unsigned.vhd" Line 117. k: Undefined symbol (last report in this block)

e_addition_unsigned.vhd" Line 122. Undefined symbol 'W'.

e_addition_unsigned.vhd" Line 122. W: Undefined symbol (last report in this block)

e_addition_unsigned.vhd" Line 126. Undefined symbol 'i'.

e_addition_unsigned.vhd" Line 126. i: Undefined symbol (last report in this block)

lace_addition_unsigned.vhd" Line 75. No sensitivity list and no wait in the process

e_addition_unsigned.vhd" Line 137. Undefined symbol 'W'.

e_addition_unsigned.vhd" Line 137. W: Undefined symbol (last report in this block)

_addition_unsigned.vhd" Line 139. - can not have such operands in this context.

e_addition_unsigned.vhd" Line 141. Undefined symbol 'add_a'.

e_addition_unsigned.vhd" Line 141. add_a: Undefined symbol (last report in this block)

e_addition_unsigned.vhd" Line 141. Undefined symbol 'i'.

e_addition_unsigned.vhd" Line 141. i: Undefined symbol (last report in this block)

e_addition_unsigned.vhd" Line 141. Undefined symbol 'stages'.

e_addition_unsigned.vhd" Line 141. stages: Undefined symbol (last report in this block)

e_addition_unsigned.vhd" Line 142. Undefined symbol 'add_b'.

e_addition_unsigned.vhd" Line 142. add_b: Undefined symbol (last report in this block)

lace_addition_unsigned.vhd" Line 137. No sensitivity list and no wait in the process

e_addition_unsigned.vhd" Line 148. Undefined symbol 'max_sum_size'.

e_addition_unsigned.vhd" Line 148. max_sum_size: Undefined symbol (last report in this block)

e_addition_unsigned.vhd" Line 150. Undefined symbol 'add_a'.

e_addition_unsigned.vhd" Line 150. add_a: Undefined symbol (last report in this block)

e_addition_unsigned.vhd" Line 151. Undefined symbol 'add_b'.

e_addition_unsigned.vhd" Line 151. add_b: Undefined symbol (last report in this block)

e_addition_unsigned.vhd" Line 152. Undefined symbol 'Cin'. Should it be: in, min or Can?

e_addition_unsigned.vhd" Line 152. Cin: Undefined symbol (last report in this block)

e_addition_unsigned.vhd" Line 154. Undefined symbol 'add_sum'.

e_addition_unsigned.vhd" Line 154. add_sum: Undefined symbol (last report in this block)

e_addition_unsigned.vhd" Line 156. Undefined symbol 'sum'.

llace_tree_functions.vhd" Line 83. In the function sizeof, not all control paths contain a return statement.

_addition_unsigned.vhd" Line 63. - can not have such operands in this context.

e_addition_unsigned.vhd" Line 64. Undefined symbol 'i'.

e_addition_unsigned.vhd" Line 64. i: Undefined symbol (last report in this block)

e_addition_unsigned.vhd" Line 64. IN mode Formal this_lvl of prev_lvl_carry_rect with no default value r

e_addition_unsigned.vhd" Line 66. IN mode Formal this_lvl of num_full_adders_rect with no default val

_addition_unsigned.vhd" Line 68. Wrong index type for W.

_addition_unsigned.vhd" Line 68. Wrong index type for W.

_addition_unsigned.vhd" Line 68. Wrong index type for W.

_addition_unsigned.vhd" Line 68. Wrong index type for W.

_addition_unsigned.vhd" Line 69. Wrong index type for W.
e_addition_unsigned.vhd" Line 72. Undefined symbol 'i'.
e_addition_unsigned.vhd" Line 72. i: Undefined symbol (last report in this block)
e_addition_unsigned.vhd" Line 72. IN mode Formal this_lvl of num_half_adders_rect with no default val
_addition_unsigned.vhd" Line 74. Wrong index type for W.
_addition_unsigned.vhd" Line 74. Wrong index type for W.
_addition_unsigned.vhd" Line 74. Wrong index type for W.
_addition_unsigned.vhd" Line 75. Wrong index type for W.
_addition_unsigned.vhd" Line 75. Wrong index type for W.
_addition_unsigned.vhd" Line 75. Wrong index type for W.
e_addition_unsigned.vhd" Line 78. Undefined symbol 'i'.
e_addition_unsigned.vhd" Line 78. i: Undefined symbol (last report in this block)
e_addition_unsigned.vhd" Line 78. IN mode Formal this_lvl of this_lvl_bits_rect with no default value mu
_addition_unsigned.vhd" Line 80. Wrong index type for W.
_addition_unsigned.vhd" Line 80. Wrong index type for W.
e_addition_unsigned.vhd" Line 83. Undefined symbol 'i'.
e_addition_unsigned.vhd" Line 83. i: Undefined symbol (last report in this block)
e_addition_unsigned.vhd" Line 83. Undefined symbol 'this_stage_bits'.
e_addition_unsigned.vhd" Line 83. this_stage_bits: Undefined symbol (last report in this block)
e_addition_unsigned.vhd" Line 86. Undefined symbol 'this_carry_bits'.
e_addition_unsigned.vhd" Line 86. this_carry_bits: Undefined symbol (last report in this block)

Is.

y type.

must be associated with an actual value.
ie must be associated with an actual value.

ue must be associated with an actual value.

ist be associated with an actual value.

Test file: wallace_add.vst		Test file: wallace_add.vst	
Release 14.7 - ver P 20110113 (beta)		Release 14.7 - ver P 20110113 (beta)	
Copyright (c) 1995-2013 Altera Inc. All rights reserved.		Copyright (c) 1995-2013 Altera Inc. All rights reserved.	
--> Parameter: TIMESUPPLY set to: wallace.vst		--> Parameter: TIMESUPPLY set to: wallace.vst	
Total PEKA time to Xst completion: 0.00 secs		Total PEKA time to Xst completion: 0.00 secs	
Total CPU time to Xst completion: 0.32 secs		Total CPU time to Xst completion: 0.23 secs	
--> WARNING: Xst 3164 - Option "debug" found multiple times in the comment line. Only the first occurrence is considered.		--> WARNING: Xst 3164 - Option "debug" found multiple times in the comment line. Only the first occurrence is considered.	
--> HSA Compilation		--> HSA Compilation	
Compiling vstlib file "C:\vhlsim\QV2024403_WALLACE_ADJUSTMENT\wallace_add.vst" in library work.		Compiling vstlib file "C:\vhlsim\QV2024403_WALLACE_ADJUSTMENT\wallace_add.vst" in library work.	
Entry <vstlib_add> completed		Entry <vstlib_add> completed	
Compiling vstlib file "C:\vhlsim\QV2024403_WALLACE_ADJUSTMENT\wallace_vstlib_functions.vst" in library work.		Compiling vstlib file "C:\vhlsim\QV2024403_WALLACE_ADJUSTMENT\wallace_vstlib_functions.vst" in library work.	
Package <vstliblib_vstlib_functions> compiled		Package <vstliblib_vstlib_functions> compiled	
Package body <wallace_vstlib_functions> compiled		Package body <wallace_vstlib_functions> compiled	
Compiling vstlib file "C:\vhlsim\QV2024403_WALLACE_ADJUSTMENT\wallace_add_in_3st.vst" in library work.		Compiling vstlib file "C:\vhlsim\QV2024403_WALLACE_ADJUSTMENT\wallace_add_in_3st.vst" in library work.	
Entry <vstlib_add_in_3st> completed		Entry <vstlib_add_in_3st> completed	
Compiling vstlib file "C:\vhlsim\QV2024403_WALLACE_ADJUSTMENT\wallace_addition_unassigned.vst" in library work.		Compiling vstlib file "C:\vhlsim\QV2024403_WALLACE_ADJUSTMENT\wallace_addition_unassigned.vst" in library work.	
Entry <wallace_addition_unassigned> completed		Entry <wallace_addition_unassigned> completed	
Total PEKA time to Xst completion: 0.00 secs		Total PEKA time to Xst completion: 0.00 secs	
Total CPU time to Xst completion: 0.72 secs		Total CPU time to Xst completion: 1.68 secs	
--		--	
Total memory usage is 4468312 kilobytes		Total memory usage is 4468800 kilobytes	
Number of errors -- 0 / 0 flagged		Number of errors -- 0 / 0 flagged	
Number of warnings -- 1 / 0 flagged		Number of warnings -- 1 / 0 flagged	
When encountered a warning add to sum both one and wallace_add to get top wallace_adder B		When encountered a warning add to sum both one and wallace_add to get top wallace_adder B	
Run P 20110113 (beta) ver QV77080900		Run P 20110113 (beta) ver QV77080900	
Number of CPUs allocated in this system: 8		Number of CPUs allocated in this system: 8	
Turning on multi-threading, number of parallel sub-completion jobs: 16		Turning on multi-threading, number of parallel sub-completion jobs: 16	
Parsing VHDL file "vstlib_add.vst" into library work		Parsing VHDL file "vstlib_add.vst" into library work	
Parsing VHDL file "vstlib_add_in_3st.vst" into library work		Parsing VHDL file "vstlib_add_in_3st.vst" into library work	
Parsing VHDL file "wallace_addition_unassigned.vst" into library work		Parsing VHDL file "wallace_addition_unassigned.vst" into library work	
Parsing VHDL file "wallace_vstlib_functions" into library work		Parsing VHDL file "wallace_vstlib_functions" into library work	
Starting static elaboration		Starting static elaboration	
Completed static elaboration		Completed static elaboration	
Compiling package standard		Compiling package standard	
Compiling package add_in_3st: 1154		Compiling package add_in_3st: 1154	
Compiling package function_vst		Compiling package function_vst	
Compiling package vstlib		Compiling package vstlib	
Compiling package wallace_vstlib_functions		Compiling package wallace_vstlib_functions	
Compiling package vstlib_top: signed		Compiling package vstlib_top: signed	
Compiling architecture lib of entity vstlib_top [vstlib_top_default]		Compiling architecture lib of entity vstlib_top [vstlib_top_default]	
Compiling architecture lib of entity vstlib_top [vstlib_top_add_in_3st1154]		Compiling architecture lib of entity vstlib_top [vstlib_top_add_in_3st1154]	
Compiling architecture wallace_unassigned_addition of entity wallace_addition [wallace_addition05.81]		Compiling architecture wallace_unassigned_addition of entity wallace_addition [wallace_addition05.81]	
Time Elapsed for compilation is 1 sec		Time Elapsed for compilation is 1 sec	
Waiting for 1 sub-completion(s) to finish		Waiting for 1 sub-completion(s) to finish	
Completed 14 VHDL Units		Completed 14 VHDL Units	
Built simulation executable wallace_add_in_3stlib_top.vst		Built simulation executable wallace_add_in_3stlib_top.vst	
Peak Memory Usage: 30484 KB		Peak Memory Usage: 30524 KB	
Peak CPU Usage: 337 ms		Peak CPU Usage: 1000 ms	
--		--	
Total time for wallace_functions_in_3stlib_top.vst and top wallace_functions_in_3stlib_top.vst		Total time for wallace_functions_in_3stlib_top.vst and top wallace_functions_in_3stlib_top.vst	
Run P 20110113 (beta) ver QV77080900		Run P 20110113 (beta) ver QV77080900	
Number of CPUs allocated in this system: 8		Number of CPUs allocated in this system: 8	
Turning on multi-threading, number of parallel sub-completion jobs: 16		Turning on multi-threading, number of parallel sub-completion jobs: 16	
Parsing VHDL file "wallace_vstlib_functions" into library work		Parsing VHDL file "wallace_vstlib_functions" into library work	
Parsing VHDL file "wallace_vstlib_functions_in_3st.vst" into library work		Parsing VHDL file "wallace_vstlib_functions_in_3st.vst" into library work	
Starting static elaboration		Starting static elaboration	

Test file wallace_add.vst		Test file wallace_add.vst	
Release 14.7 - sat P 20110113 (m64)		Release 14.7 - sat P 20110113 (m64)	
Copyright (c) 1995-2013 Intel Inc. All rights reserved.		Copyright (c) 1995-2013 Intel Inc. All rights reserved.	
--> Parameter: MEMDIS and its subcomponents		--> Parameter: MEMDIS and its subcomponents	
Total PEBA time to Xat completion: 0.00 secs		Total PEBA time to Xat completion: 0.00 secs	
Total CPU time to Xat completion: 0.24 secs		Total CPU time to Xat completion: 0.23 secs	
--> WARNING: Xat 3164 - Option "debug" found multiple times in the comment line. Only the first occurrence is considered.		--> WARNING: Xat 3164 - Option "debug" found multiple times in the comment line. Only the first occurrence is considered.	
IHL Compilations		IHL Compilations	
Compiling vstlib file "C:\subINOV_P20024503_WALLACE_ADJUSTMENT\issac.vst" in library work		Compiling vstlib file "C:\subINOV_P20024503_WALLACE_ADJUSTMENT\issac.vst" in library work	
Entry vstlib_issac compiled		Entry vstlib_issac compiled	
Compiling vstlib file "C:\subINOV_P20024503_WALLACE_ADJUSTMENT\issac_functions.vst" in library work		Compiling vstlib file "C:\subINOV_P20024503_WALLACE_ADJUSTMENT\issac_functions.vst" in library work	
Package vstlib_issac_functions compiled		Package vstlib_issac_functions compiled	
Package body vstlib_issac_functions compiled		Package body vstlib_issac_functions compiled	
Compiling vstlib file "C:\subINOV_P20024503_WALLACE_ADJUSTMENT\issac_add_316.vst" in library work		Compiling vstlib file "C:\subINOV_P20024503_WALLACE_ADJUSTMENT\issac_add_316.vst" in library work	
Entry vstlib_issac_add_316 compiled		Entry vstlib_issac_add_316 compiled	
Compiling vstlib file "C:\subINOV_P20024503_WALLACE_ADJUSTMENT\issac_addition_unassigned.vst" in library work		Compiling vstlib file "C:\subINOV_P20024503_WALLACE_ADJUSTMENT\issac_addition_unassigned.vst" in library work	
Entry vstlib_addition_unassigned compiled		Entry vstlib_addition_unassigned compiled	
Total PEBA time to Xat completion: 0.00 secs		Total PEBA time to Xat completion: 0.00 secs	
Total CPU time to Xat completion: 0.47 secs		Total CPU time to Xat completion: 1.68 secs	
Total memory usage is 4468316 kibibytes		Total memory usage is 4468320 kibibytes	
Number of errors - 0 / 0 (failed)		Number of errors - 0 / 0 (failed)	
Number of warnings - 1 / 0 (failed)		Number of warnings - 1 / 0 (failed)	
When connecting a wallace_add to some both ones and wallace_add to just-top wallace_adder: B		When connecting a wallace_add to some both ones and wallace_add to just-top wallace_adder: B	
Run P 20110113 (signature 0x77080900)		Run P 20110113 (signature 0x77080900)	
Number of CPUs detected in this system: 8		Number of CPUs detected in this system: 8	
Turning on multi-threading, number of parallel sub-completion jobs: 16		Turning on multi-threading, number of parallel sub-completion jobs: 16	
Parallelizing completion jobs at 14% time		Parallelizing completion jobs at 14% time	
Parsing VHSX file vstlib_issac.vst into library work		Parsing VHSX file vstlib_issac.vst into library work	
Parsing VHSX file vstlib_issac_316.vst into library work		Parsing VHSX file vstlib_issac_316.vst into library work	
Parsing VHSX file vstlib_issac_functions.vst into library work		Parsing VHSX file vstlib_issac_functions.vst into library work	
Parsing VHSX file vstlib_addition_unassigned.vst into library work		Parsing VHSX file vstlib_addition_unassigned.vst into library work	
Parsing VHSX file vstlib_addition_unassigned_316.vst into library work		Parsing VHSX file vstlib_addition_unassigned_316.vst into library work	
Starting static elaboration		Starting static elaboration	
Completed static elaboration		Completed static elaboration	
Compiling package standard		Compiling package standard	
Compiling package issac_top: 1154		Compiling package issac_top: 1154	
Compiling package issac_add_316		Compiling package issac_add_316	
Compiling package issac_addition_unassigned		Compiling package issac_addition_unassigned	
Compiling package issac_top: functions		Compiling package issac_top: functions	
Compiling package issac_top: add_316		Compiling package issac_top: add_316	
Compiling package issac_top: signed		Compiling package issac_top: signed	
Compiling architecture issac of entry issac_add_316.vst into 32011170		Compiling architecture issac of entry issac_add_316.vst into 32011170	
Compiling architecture issac_addition_unassigned of entry wallace_addition_unassigned.vst		Compiling architecture issac_addition_unassigned of entry wallace_addition_unassigned.vst	
Compiling architecture issac_addition_unassigned_316 of entry wallace_addition_unassigned_316		Compiling architecture issac_addition_unassigned_316 of entry wallace_addition_unassigned_316	
Time Required for compilation is 1 sec		Time Required for compilation is 1 sec	
Waiting for 1 sub-completion(s) to finish		Waiting for 1 sub-completion(s) to finish	
Completed 14 VHSX Units		Completed 14 VHSX Units	
Built simulation executable wallace_add_316.vst into both ones		Built simulation executable wallace_add_316.vst into both ones	
Total Memory Usage: 30248.00		Total Memory Usage: 30248.00	
Total CPU Usage: 174 ms		Total CPU Usage: 1000 ms	
Built simulation executable wallace_add_316.vst into both ones and wallace_top: functions into just-top wallace_adder: B		Built simulation executable wallace_add_316.vst into both ones and wallace_top: functions into just-top wallace_adder: B	
Run P 20110113 (signature 0x77080900)		Run P 20110113 (signature 0x77080900)	
Number of CPUs detected in this system: 8		Number of CPUs detected in this system: 8	
Turning on multi-threading, number of parallel sub-completion jobs: 16		Turning on multi-threading, number of parallel sub-completion jobs: 16	
Parallelizing completion jobs at 14% time		Parallelizing completion jobs at 14% time	
Parsing VHSX file vstlib_issac_functions.vst into library work		Parsing VHSX file vstlib_issac_functions.vst into library work	
Parsing VHSX file vstlib_issac_functions_316.vst into library work		Parsing VHSX file vstlib_issac_functions_316.vst into library work	
Starting static elaboration		Starting static elaboration	

Test: lib: wallace, add, int		Test: lib: wallace, add, int	
Release 14.7 - opt P 20110113 (m64)		Release 14.7 - opt P 20110113 (m64)	
Copyright (c) 1995-2013 Intel Inc. All rights reserved.		Copyright (c) 1995-2013 Intel Inc. All rights reserved.	
--> Program: THECDS and its subprograms.exe		--> Program: THECDS and its subprograms.exe	
Total PECS time to Xat completion: 0.00 secs		Total PECS time to Xat completion: 0.00 secs	
Total CPU time to Xat completion: 0.26 secs		Total CPU time to Xat completion: 0.23 secs	
--> WARNING: Xat 3164 - Option "debug" found multiple times in the comment line. Only the first occurrence is considered.		--> WARNING: Xat 3164 - Option "debug" found multiple times in the comment line. Only the first occurrence is considered.	
IHL: Compilation		IHL: Compilation	
Compiling subfile "C:\subINOV_P20024503_WALLACE_ADJUSTMENT\wallace_add.vshf" in library work.		Compiling subfile "C:\subINOV_P20024503_WALLACE_ADJUSTMENT\wallace_add.vshf" in library work.	
Entry <int, add> compiled		Entry <int, add> compiled	
Entry <int, add> in 32-bit architecture already compiled		Entry <int, add> in 32-bit architecture <v> compiled	
Compiling subfile "C:\subINOV_P20024503_WALLACE_ADJUSTMENT\wallace_intn_functions.vshf" in library work.		Compiling subfile "C:\subINOV_P20024503_WALLACE_ADJUSTMENT\wallace_intn_functions.vshf" in library work.	
Package <intn_functions_intn_functions> compiled		Package <intn_functions_intn_functions> compiled	
Package body <Wallace_intn_functions> compiled		Package body <Wallace_intn_functions> compiled	
Compiling subfile "C:\subINOV_P20024503_WALLACE_ADJUSTMENT\wallace_add_in_32.vshf" in library work.		Compiling subfile "C:\subINOV_P20024503_WALLACE_ADJUSTMENT\wallace_add_in_32.vshf" in library work.	
Entry <int, add> in 32-bit compiled		Entry <int, add> in 32-bit compiled	
Entry <int, add> in 32-bit architecture already compiled		Entry <int, add> in 32-bit architecture <v> compiled	
Compiling subfile "C:\subINOV_P20024503_WALLACE_ADJUSTMENT\wallace_addition_unassigned.vshf" in library work.		Compiling subfile "C:\subINOV_P20024503_WALLACE_ADJUSTMENT\wallace_addition_unassigned.vshf" in library work.	
Entry <wallace_addition_unassigned> compiled		Entry <wallace_addition_unassigned> compiled	
Entry <wallace_addition_unassigned> (Architecture <Wallace_unassigned_addition>) compiled		Entry <wallace_addition_unassigned> (Architecture <Wallace_unassigned_addition>) compiled	
Total PECS time to Xat completion: 1.46 secs		Total PECS time to Xat completion: 2.30 secs	
Total CPU time to Xat completion: 0.52 secs		Total CPU time to Xat completion: 1.68 secs	
Total memory usage is 4468393 kibibytes		Total memory usage is 4468393 kibibytes	
Number of errors - 0 / 0 (failed)		Number of errors - 0 / 0 (failed)	
Number of warnings - 1 / 1 (0 (failed)		Number of warnings - 1 / 1 (0 (failed)	
When connecting a wallace_add to some both ones and wallace_add to just one wallace_adder, B		When connecting a wallace_add to some both ones and wallace_add to just one wallace_adder, B	
(Item P 20110113 (signature 0x77080900))		(Item P 20110113 (signature 0x77080900))	
Number of CPUs detected in this system: 8		Number of CPUs detected in this system: 8	
Turning on multi-threading, number of parallel sub-completion jobs: 16		Turning on multi-threading, number of parallel sub-completion jobs: 16	
Parallelizing completion jobs at 14% time		Parallelizing completion jobs at 14% time	
Parsing VHSX file "lib_add.vshf" into library work		Parsing VHSX file "lib_add.vshf" into library work	
Parsing VHSX file "lib_add_in_32.vshf" into library work		Parsing VHSX file "lib_add_in_32.vshf" into library work	
Parsing VHSX file "Wallace_intn_functions.vshf" into library work		Parsing VHSX file "Wallace_intn_functions.vshf" into library work	
Parsing VHSX file "Wallace_addition_unassigned.vshf" into library work		Parsing VHSX file "Wallace_addition_unassigned.vshf" into library work	
Parsing VHSX file "wallace_addition_unassigned_in_32.vshf" into library work		Parsing VHSX file "wallace_addition_unassigned_in_32.vshf" into library work	
Starting static elaboration		Starting static elaboration	
Completed static elaboration		Completed static elaboration	
Compiling package standard		Compiling package standard	
Compiling package int, type: 1164		Compiling package int, type: 1164	
Compiling package numeric_int		Compiling package numeric_int	
Compiling package tests		Compiling package tests	
Compiling package wallace_intn_functions		Compiling package wallace_intn_functions	
Compiling package int, type: 1036		Compiling package int, type: 1036	
Compiling package int, type: 1036		Compiling package int, type: 1036	
Compiling architecture lib of entry int, add, in_32 (int, add, in_32) (1171)		Compiling architecture lib of entry int, add, in_32 (int, add, in_32) (1171)	
Compiling architecture wallace_unassigned_addition of entry wallace_addition (wallace_addition) (513)		Compiling architecture wallace_unassigned_addition of entry wallace_addition (wallace_addition) (513)	
Time Resolution for completion is 1 sec		Time Resolution for completion is 1 sec	
Waiting for 1 sub-completion(s) to finish		Waiting for 1 sub-completion(s) to finish	
Completed 14 VHSX Units		Completed 14 VHSX Units	
Built simulation executable wallace_add_in_32.vshf, lib_add		Built simulation executable wallace_add_in_32.vshf, lib_add	
Final Memory Usage: 3036K, 90		Final Memory Usage: 3036K, 90	
Final CPU Usage: 1041 ms		Final CPU Usage: 1003 ms	
Built simulation executable wallace_intn_functions, lib_add, int, lib_add, int, lib_add, int		Built simulation executable wallace_intn_functions, lib_add, int, lib_add, int, lib_add, int	
(Item P 20110113 (signature 0x77080900))		(Item P 20110113 (signature 0x77080900))	
Number of CPUs detected in this system: 8		Number of CPUs detected in this system: 8	
Turning on multi-threading, number of parallel sub-completion jobs: 16		Turning on multi-threading, number of parallel sub-completion jobs: 16	
Parallelizing completion jobs at 14% time		Parallelizing completion jobs at 14% time	
Parsing VHSX file "Wallace_intn_functions.vshf" into library work		Parsing VHSX file "Wallace_intn_functions.vshf" into library work	
Parsing VHSX file "Wallace_intn_functions_in_32.vshf" into library work		Parsing VHSX file "Wallace_intn_functions_in_32.vshf" into library work	
Starting static elaboration		Starting static elaboration	

Test: lib: wallace, add, int		Test: lib: wallace, add, int	
Release 14.7 - opt P 20110113 (m68k)		Release 14.7 - opt P 20110113 (m68k)	
Copyright (c) 1995-2013 Intel, Inc. All rights reserved.		Copyright (c) 1995-2013 Intel, Inc. All rights reserved.	
--> Program: THECDS and its subprograms.exe		--> Program: THECDS and its subprograms.exe	
Total PECS time to Xat completion: 0.00 secs		Total PECS time to Xat completion: 0.00 secs	
Total CPU time to Xat completion: 0.32 secs		Total CPU time to Xat completion: 0.33 secs	
--> WARNING: Xat 3164 - Option "debug" found multiple times in the comment line. Only the first occurrence is considered.		--> WARNING: Xat 3164 - Option "debug" found multiple times in the comment line. Only the first occurrence is considered.	
IHL: Compilation		IHL: Compilation	
Compiling subfile "C:\subINOV_P20024503_WALLACE_ADJUSTMENT\wallace_add.vshf" in library work.		Compiling subfile "C:\subINOV_P20024503_WALLACE_ADJUSTMENT\wallace_add.vshf" in library work.	
Entry <int, add> in "Wallace" already compiled		Entry <int, add> in "Wallace" already compiled	
Compiling subfile "C:\subINOV_P20024503_WALLACE_ADJUSTMENT\wallace_inte_functions.vshf" in library work.		Compiling subfile "C:\subINOV_P20024503_WALLACE_ADJUSTMENT\wallace_inte_functions.vshf" in library work.	
Package <inte_functions> in "Wallace" compiled		Package <inte_functions> in "Wallace" compiled	
Package body <Wallace> in "Wallace" compiled		Package body <Wallace> in "Wallace" compiled	
Compiling subfile "C:\subINOV_P20024503_WALLACE_ADJUSTMENT\wallace_add_in_3d.vshf" in library work.		Compiling subfile "C:\subINOV_P20024503_WALLACE_ADJUSTMENT\wallace_add_in_3d.vshf" in library work.	
Entry <int, add> in "3d" already compiled		Entry <int, add> in "3d" already compiled	
Compiling subfile "C:\subINOV_P20024503_WALLACE_ADJUSTMENT\wallace_addition_unassigned.vshf" in library work.		Compiling subfile "C:\subINOV_P20024503_WALLACE_ADJUSTMENT\wallace_addition_unassigned.vshf" in library work.	
Entry <wallace> addition <int> in "Wallace" already compiled		Entry <wallace> addition <int> in "Wallace" already compiled	
Total PECS time to Xat completion: 1.49 secs		Total PECS time to Xat completion: 2.30 secs	
Total CPU time to Xat completion: 0.72 secs		Total CPU time to Xat completion: 1.68 secs	
Total memory usage is 4469316 kilobytes		Total memory usage is 4469303 kilobytes	
Number of errors - 0 / 0 (failed)		Number of errors - 0 / 0 (failed)	
Number of warnings - 1 / 1 (0 failed)		Number of warnings - 1 / 1 (0 failed)	
When connecting a wallace <add> to some both one- and wallace <add> to get-top wallace <adder> to		When connecting a wallace <add> to some both one- and wallace <add> to get-top wallace <adder> to	
[Item P 20110113 (signature 0x77080900)]		[Item P 20110113 (signature 0x77080900)]	
Number of CPUs detected in this system: 8		Number of CPUs detected in this system: 8	
Turning on multi-threading, number of parallel sub-completion jobs: 16		Turning on multi-threading, number of parallel sub-completion jobs: 16	
Parallelizing completion jobs at 14% time		Parallelizing completion jobs at 14% time	
Parsing VHSX file "lib_3d.vshf" into library work		Parsing VHSX file "lib_3d.vshf" into library work	
Parsing VHSX file "lib_3d.vshf" into library work		Parsing VHSX file "lib_3d.vshf" into library work	
Parsing VHSX file "Wallace_3d.vshf" into library work		Parsing VHSX file "Wallace_3d.vshf" into library work	
Parsing VHSX file "Wallace_addition_unassigned.vshf" into library work		Parsing VHSX file "Wallace_addition_unassigned.vshf" into library work	
Parsing VHSX file "Wallace_addition_unassigned_in_3d.vshf" into library work		Parsing VHSX file "Wallace_addition_unassigned_in_3d.vshf" into library work	
Starting static elaboration		Starting static elaboration	
Completed static elaboration		Completed static elaboration	
Compiling package standard		Compiling package standard	
Compiling package int, type: 1154		Compiling package int, type: 1154	
Compiling package integer_int		Compiling package integer_int	
Compiling package tests		Compiling package tests	
Compiling package wallace, type: functions		Compiling package wallace, type: functions	
Compiling package int, type: 1000		Compiling package int, type: 1000	
Compiling package int, type: 1000		Compiling package int, type: 1000	
Compiling architecture lib of entry int, add, in_3d, 3d, add, in_3d (1111)		Compiling architecture lib of entry int, add, in_3d, 3d, add, in_3d (1111)	
Compiling architecture wallace, unassigned, addition of entry wallace, addition (function, addition(5,3))		Compiling architecture wallace, unassigned, addition of entry wallace, addition (function, addition(5,3))	
Time (seconds) for simulation to finish		Time (seconds) for simulation to finish	
Waiting for 1 sub-completion(s) to finish		Waiting for 1 sub-completion(s) to finish	
Completed 14 VHSX units		Completed 14 VHSX units	
Built simulation executable wallace_add_in_3d.vshf.exe		Built simulation executable wallace_add_in_3d.vshf.exe	
Total Memory Usage: 38173.90		Total Memory Usage: 38024.08	
Peak CPU Usage: 184 ms		Peak CPU Usage: 1000 ms	
IHL: Compilation		IHL: Compilation	
Compiling subfile "C:\subINOV_P20024503_WALLACE_ADJUSTMENT\wallace_inte_functions_in_3d.vshf" in library work.		Compiling subfile "C:\subINOV_P20024503_WALLACE_ADJUSTMENT\wallace_inte_functions_in_3d.vshf" in library work.	
Entry <int, add> in "3d" already compiled		Entry <int, add> in "3d" already compiled	
Compiling subfile "C:\subINOV_P20024503_WALLACE_ADJUSTMENT\wallace_inte_functions_in_3d.vshf" in library work.		Compiling subfile "C:\subINOV_P20024503_WALLACE_ADJUSTMENT\wallace_inte_functions_in_3d.vshf" in library work.	
Package <inte_functions_in_3d> in "Wallace" compiled		Package <inte_functions_in_3d> in "Wallace" compiled	
Package body <Wallace> in "Wallace" compiled		Package body <Wallace> in "Wallace" compiled	
Compiling subfile "C:\subINOV_P20024503_WALLACE_ADJUSTMENT\wallace_addition_unassigned.vshf" in library work.		Compiling subfile "C:\subINOV_P20024503_WALLACE_ADJUSTMENT\wallace_addition_unassigned.vshf" in library work.	
Entry <wallace> addition <int> in "Wallace" already compiled		Entry <wallace> addition <int> in "Wallace" already compiled	
Total PECS time to Xat completion: 1.49 secs		Total PECS time to Xat completion: 2.30 secs	
Total CPU time to Xat completion: 0.72 secs		Total CPU time to Xat completion: 1.68 secs	
Total memory usage is 4469316 kilobytes		Total memory usage is 4469303 kilobytes	
Number of errors - 0 / 0 (failed)		Number of errors - 0 / 0 (failed)	
Number of warnings - 1 / 1 (0 failed)		Number of warnings - 1 / 1 (0 failed)	
When connecting a wallace <add> to some both one- and wallace <add> to get-top wallace <adder> to		When connecting a wallace <add> to some both one- and wallace <add> to get-top wallace <adder> to	
[Item P 20110113 (signature 0x77080900)]		[Item P 20110113 (signature 0x77080900)]	
Number of CPUs detected in this system: 8		Number of CPUs detected in this system: 8	
Turning on multi-threading, number of parallel sub-completion jobs: 16		Turning on multi-threading, number of parallel sub-completion jobs: 16	
Parallelizing completion jobs at 14% time		Parallelizing completion jobs at 14% time	
Parsing VHSX file "lib_3d.vshf" into library work		Parsing VHSX file "lib_3d.vshf" into library work	
Parsing VHSX file "Wallace_3d.vshf" into library work		Parsing VHSX file "Wallace_3d.vshf" into library work	
Parsing VHSX file "Wallace_addition_unassigned.vshf" into library work		Parsing VHSX file "Wallace_addition_unassigned.vshf" into library work	
Starting static elaboration		Starting static elaboration	


```

>xst -ifn wallace_add.xst
Release 14.7 - xst P.20131013 (nt64)
Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.
--> Parameter TMPDIR set to ./xst/projnav.tmp
Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.23 secs

--> WARNING:Xst:3164 - Option "-debug" found multiple times in the command line. Only the first occurrence
*          HDL Compilation          *
Compiling vhdl file "C:/vhdl/NDV_DN/2024/03_WALLACE_ADD/STUDENTI//cla_gp.vhd" in Library work
Entity <cla_gp> compiled.
Entity <cla_gp> (Architecture <>) compiled.
Compiling vhdl file "C:/vhdl/NDV_DN/2024/03_WALLACE_ADD/STUDENTI//Wallace_tree_functions.vhdl" in Library work
Package <Wallace_tree_functions> compiled.
Package body <Wallace_tree_functions> compiled.
Compiling vhdl file "C:/vhdl/NDV_DN/2024/03_WALLACE_ADD/STUDENTI//cla_add_n_bit.vhd" in Library work
Entity <cla_add_n_bit> compiled.
Entity <cla_add_n_bit> (Architecture <>) compiled.
Compiling vhdl file "C:/vhdl/NDV_DN/2024/03_WALLACE_ADD/STUDENTI//wallace_addition_unsigned.vhdl" in Library work
Entity <wallace_addition> compiled.
Entity <wallace_addition> (Architecture <Wallace_unsigned_addition>) compiled.
Total REAL time to Xst completion: 2.00 secs
Total CPU time to Xst completion: 1.68 secs

-->
Total memory usage is 4468880 kilobytes
Number of errors   : 0 (0 filtered)
Number of warnings : 1 (0 filtered)
Number of infos   : 0 (0 filtered)
>fuse -incremental -o wallace_add_tb_isim_beh.exe -prj wallace_add_tb.prj -top wallace_adder_tb
ISim P.20131013 (signature 0x7708f090)
Number of CPUs detected in this system: 8
Turning on mult-threading, number of parallel sub-compilation jobs: 16
Determining compilation order of HDL files
Parsing VHDL file "cla_gp.vhd" into library work
Parsing VHDL file "cla_add_n_bit.vhd" into library work
Parsing VHDL file "Wallace_tree_functions.vhdl" into library work
Parsing VHDL file "wallace_addition_unsigned.vhdl" into library work
Parsing VHDL file "wallace_addition_unsigned_tb.vhd" into library work
Starting static elaboration
Completed static elaboration
Compiling package standard
Compiling package std_logic_1164
Compiling package numeric_std
Compiling package textio
Compiling package wallace_tree_functions
Compiling package std_logic_arith
Compiling package std_logic_signed
Compiling architecture of entity cla_gp [cla_gp_default]
Compiling architecture of entity cla_add_n_bit [cla_add_n_bit(11)]
Compiling architecture wallace_unsigned_addition of entity wallace_addition [wallace_addition(8,8)]
Compiling architecture tb of entity wallace_adder_tb
Time Resolution for simulation is 1ps.
Waiting for 1 sub-compilation(s) to finish...
Compiled 14 VHDL Units
Built simulation executable wallace_add_tb_isim_beh.exe
Fuse Memory Usage: 38292 KB
Fuse CPU Usage: 1000 ms

```

```

>fuse -incremental -o wallace_functions_tb_isim_beh.exe -prj Wallace_tree_functions_tb.prj -top wallac
ISim P.20131013 (signature 0x7708f090)
Number of CPUs detected in this system: 8
Turning on mult-threading, number of parallel sub-compilation jobs: 16
Determining compilation order of HDL files
Parsing VHDL file "Wallace_tree_functions.vhd" into library work
Parsing VHDL file "Wallace_tree_functions_tb.vhd" into library work
Starting static elaboration
Completed static elaboration
Compiling package standard
Compiling package std_logic_1164
Compiling package numeric_std
Compiling package textio
Compiling package std_logic_textio
Compiling package wallace_tree_functions
Compiling architecture tb of entity wallace_functions_tb
Time Resolution for simulation is 1ps.
Compiled 7 VHDL Units
Built simulation executable wallace_functions_tb_isim_beh.exe
Fuse Memory Usage: 36728 KB
Fuse CPU Usage: 781 ms
>fuse -incremental -o wallace_using__functions_tb_isim_beh.exe -prj wallace_add_using__functions_t
ISim P.20131013 (signature 0x7708f090)
Number of CPUs detected in this system: 8
Turning on mult-threading, number of parallel sub-compilation jobs: 16
Determining compilation order of HDL files
Parsing VHDL file "cla_gp.vhd" into library work
Parsing VHDL file "cla_add_n_bit.vhd" into library work
Parsing VHDL file "Wallace_tree_functions_.vhd" into library work
Parsing VHDL file "wallace_addition_unsigned.vhd" into library work
Parsing VHDL file "wallace_add_using__functions_tb.vhd" into library work
Starting static elaboration
Completed static elaboration
Compiling package standard
Compiling package std_logic_1164
Compiling package numeric_std
Compiling package textio
Compiling package wallace_tree_functions
Compiling package std_logic_arith
Compiling package std_logic_signed
Compiling architecture of entity cla_gp [cla_gp_default]
Compiling architecture of entity cla_add_n_bit [cla_add_n_bit(11)]
Compiling architecture wallace_unsigned_addition of entity wallace_addition [wallace_addition(8,8)]
Compiling architecture tb of entity wallace_add_using__function...
Time Resolution for simulation is 1ps.
Waiting for 1 sub-compilation(s) to finish...
Compiled 14 VHDL Units
Built simulation executable wallace_using__functions_tb_isim_beh.exe
Fuse Memory Usage: 38164 KB
Fuse CPU Usage: 1046 ms
>fuse -incremental -o Wallace_tree_functions_detailed_tb_5x4_isim_beh.exe -prj Wallace_tree_funcio
ISim P.20131013 (signature 0x7708f090)
Number of CPUs detected in this system: 8
Turning on mult-threading, number of parallel sub-compilation jobs: 16
Determining compilation order of HDL files
Parsing VHDL file "Wallace_tree_functions.vhd" into library work
Parsing VHDL file "Wallace_tree_functions_detailed_tb.vhd" into library work
Starting static elaboration
Completed static elaboration

```

Compiling package standard
 Compiling package std_logic_1164
 Compiling package numeric_std
 Compiling package textio
 Compiling package std_logic_textio
 Compiling package wallace_tree_functions
 Compiling architecture tb of entity wallace_tree_functions_detailed_...
 Time Resolution for simulation is 1ps.
 Waiting for 1 sub-compilation(s) to finish...
 Compiled 7 VHDL Units
 Built simulation executable Wallace_tree_functions_detailed_tb_5x4_isim_beh.exe
 Fuse Memory Usage: 36808 KB
 Fuse CPU Usage: 812 ms
 >fuse -incremental -o Wallace_tree_functions_detailed_tb_6x5_isim_beh.exe -prj Wallace_tree_funcio
 ISim P.20131013 (signature 0x7708f090)
 Number of CPUs detected in this system: 8
 Turning on mult-threading, number of parallel sub-compilation jobs: 16
 Determining compilation order of HDL files
 Parsing VHDL file "Wallace_tree_functions.vhd" into library work
 Parsing VHDL file "Wallace_tree_functions_detailed_tb.vhd" into library work
 Starting static elaboration
 Completed static elaboration
 Compiling package standard
 Compiling package std_logic_1164
 Compiling package numeric_std
 Compiling package textio
 Compiling package std_logic_textio
 Compiling package wallace_tree_functions
 Compiling architecture tb of entity wallace_tree_functions_detailed_...
 Time Resolution for simulation is 1ps.
 Compiled 7 VHDL Units
 Built simulation executable Wallace_tree_functions_detailed_tb_6x5_isim_beh.exe
 Fuse Memory Usage: 36724 KB
 Fuse CPU Usage: 937 ms
 >fuse -incremental -o Wallace_tree_functions_detailed_tb_7x6_isim_beh.exe -prj Wallace_tree_funcio
 ISim P.20131013 (signature 0x7708f090)
 Number of CPUs detected in this system: 8
 Turning on mult-threading, number of parallel sub-compilation jobs: 16
 Determining compilation order of HDL files
 Parsing VHDL file "Wallace_tree_functions.vhd" into library work
 Parsing VHDL file "Wallace_tree_functions_detailed_tb.vhd" into library work
 Starting static elaboration
 Completed static elaboration
 Compiling package standard
 Compiling package std_logic_1164
 Compiling package numeric_std
 Compiling package textio
 Compiling package std_logic_textio
 Compiling package wallace_tree_functions
 Compiling architecture tb of entity wallace_tree_functions_detailed_...
 Time Resolution for simulation is 1ps.
 Compiled 7 VHDL Units
 Built simulation executable Wallace_tree_functions_detailed_tb_7x6_isim_beh.exe
 Fuse Memory Usage: 36972 KB
 Fuse CPU Usage: 827 ms
 >fuse -incremental -o Wallace_tree_functions_detailed_tb_8x7_isim_beh.exe -prj Wallace_tree_funcio
 ISim P.20131013 (signature 0x7708f090)
 Number of CPUs detected in this system: 8
 Turning on mult-threading, number of parallel sub-compilation jobs: 16

Determining compilation order of HDL files
 Parsing VHDL file "Wallace_tree_functions.vhd" into library work
 Parsing VHDL file "Wallace_tree_functions_detailed_tb.vhd" into library work
 Starting static elaboration
 Completed static elaboration
 Compiling package standard
 Compiling package std_logic_1164
 Compiling package numeric_std
 Compiling package textio
 Compiling package std_logic_textio
 Compiling package wallace_tree_functions
 Compiling architecture tb of entity wallace_tree_functions_detailed_...
 Time Resolution for simulation is 1ps.
 Compiled 7 VHDL Units
 Built simulation executable Wallace_tree_functions_detailed_tb_8x7_isim_beh.exe
 Fuse Memory Usage: 36752 KB
 Fuse CPU Usage: 827 ms
 >wallace_add_tb_isim_beh.exe -tclbatch isim.tcl -wdb wallace_add_tb_isim_beh.wdb
 ISim P.20131013 (signature 0x7708f090)
 WARNING: A WEBPACK license was found.
 WARNING: Please use Xilinx License Configuration Manager to check out a full ISim license.
 WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for more information on t
 This is a Lite version of ISim.
 Time resolution is 1 ps
 Simulator is doing circuit initialization process.
 at 0 ps: Note: Stage: 0 of 3 (/wallace_adder_tb/UUT/).
 at 0 ps: Note: Bit#/Total 10/0EA: 0HA: 0C: 0W: 0 (/wallace_adder_tb/UUT/).
 at 0 ps: Note: Bit#/Total 9/0EA: 0HA: 0C: 0W: 0 (/wallace_adder_tb/UUT/).
 at 0 ps: Note: Bit#/Total 8/0EA: 0HA: 0C: 3W: 0 (/wallace_adder_tb/UUT/).
 at 0 ps: Note: Bit#/Total 7/8EA: 2HA: 1C: 3W: 0 (/wallace_adder_tb/UUT/).
 at 0 ps: Note: Bit#/Total 6/8EA: 2HA: 1C: 3W: 0 (/wallace_adder_tb/UUT/).
 at 0 ps: Note: Bit#/Total 5/8EA: 2HA: 1C: 3W: 0 (/wallace_adder_tb/UUT/).
 at 0 ps: Note: Bit#/Total 4/8EA: 2HA: 1C: 3W: 0 (/wallace_adder_tb/UUT/).
 at 0 ps: Note: Bit#/Total 3/8EA: 2HA: 1C: 3W: 0 (/wallace_adder_tb/UUT/).
 at 0 ps: Note: Bit#/Total 2/8EA: 2HA: 1C: 3W: 0 (/wallace_adder_tb/UUT/).
 at 0 ps: Note: Bit#/Total 1/8EA: 2HA: 1C: 3W: 0 (/wallace_adder_tb/UUT/).
 at 0 ps: Note: Bit#/Total 0/8EA: 2HA: 1C: 0W: 0 (/wallace_adder_tb/UUT/).
 at 0 ps: Note: Stage: 1 of 3 (/wallace_adder_tb/UUT/).
 at 0 ps: Note: Bit#/Total 10/0EA: 0HA: 0C: 0W: 0 (/wallace_adder_tb/UUT/).
 at 0 ps: Note: Bit#/Total 9/0EA: 0HA: 0C: 1W: 0 (/wallace_adder_tb/UUT/).
 at 0 ps: Note: Bit#/Total 8/3EA: 1HA: 0C: 2W: 0 (/wallace_adder_tb/UUT/).
 at 0 ps: Note: Bit#/Total 7/6EA: 2HA: 0C: 2W: 0 (/wallace_adder_tb/UUT/).
 at 0 ps: Note: Bit#/Total 6/6EA: 2HA: 0C: 2W: 0 (/wallace_adder_tb/UUT/).
 at 0 ps: Note: Bit#/Total 5/6EA: 2HA: 0C: 2W: 0 (/wallace_adder_tb/UUT/).
 at 0 ps: Note: Bit#/Total 4/6EA: 2HA: 0C: 2W: 0 (/wallace_adder_tb/UUT/).
 at 0 ps: Note: Bit#/Total 3/6EA: 2HA: 0C: 2W: 0 (/wallace_adder_tb/UUT/).
 at 0 ps: Note: Bit#/Total 2/6EA: 2HA: 0C: 2W: 0 (/wallace_adder_tb/UUT/).
 at 0 ps: Note: Bit#/Total 1/6EA: 2HA: 0C: 1W: 0 (/wallace_adder_tb/UUT/).
 at 0 ps: Note: Bit#/Total 0/3EA: 1HA: 0C: 0W: 0 (/wallace_adder_tb/UUT/).
 at 0 ps: Note: Stage: 2 of 3 (/wallace_adder_tb/UUT/).
 at 0 ps: Note: Bit#/Total 10/0EA: 0HA: 0C: 0W: 0 (/wallace_adder_tb/UUT/).
 at 0 ps: Note: Bit#/Total 9/1EA: 0HA: 0C: 1W: 1 (/wallace_adder_tb/UUT/).
 at 0 ps: Note: Bit#/Total 8/3EA: 1HA: 0C: 1W: 0 (/wallace_adder_tb/UUT/).
 at 0 ps: Note: Bit#/Total 7/4EA: 1HA: 0C: 1W: 1 (/wallace_adder_tb/UUT/).
 at 0 ps: Note: Bit#/Total 6/4EA: 1HA: 0C: 1W: 1 (/wallace_adder_tb/UUT/).
 at 0 ps: Note: Bit#/Total 5/4EA: 1HA: 0C: 1W: 1 (/wallace_adder_tb/UUT/).
 at 0 ps: Note: Bit#/Total 4/4EA: 1HA: 0C: 1W: 1 (/wallace_adder_tb/UUT/).
 at 0 ps: Note: Bit#/Total 3/4EA: 1HA: 0C: 1W: 1 (/wallace_adder_tb/UUT/).
 at 0 ps: Note: Bit#/Total 2/4EA: 1HA: 0C: 1W: 1 (/wallace_adder_tb/UUT/).

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at 800 ns(6): Note: Bit#/Total 5/3EA: 1HA: 0C: 1W: 0 (/wallace_adder_tb/UUT/).

at 800 ns(6): Note: Bit#/Total 4/3EA: 1HA: 0C: 1W: 0 (/wallace_adder_tb/UUT/).

at 800 ns(6): Note: Bit#/Total 3/3EA: 1HA: 0C: 1W: 0 (/wallace_adder_tb/UUT/).

at 800 ns(6): Note: Bit#/Total 2/3EA: 1HA: 0C: 0W: 0 (/wallace_adder_tb/UUT/).

at 800 ns(6): Note: Bit#/Total 1/1EA: 0HA: 0C: 0W: 1 (/wallace_adder_tb/UUT/).

at 800 ns(6): Note: Bit#/Total 0/1EA: 0HA: 0C: 0W: 1 (/wallace_adder_tb/UUT/).

at 800 ns(6): Note: Last stage (/wallace_adder_tb/UUT/).

>wallace_functions_tb_isim_beh.exe -tclbatch isim.tcl -wdb wallace_functions_tb_isim_beh.wdb

ISim P.20131013 (signature 0x7708f090)

WARNING: A WEBPACK license was found.

WARNING: Please use Xilinx License Configuration Manager to check out a full ISim license.

WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for more information on t

This is a Lite version of ISim.

Time resolution is 1 ps

Simulator is doing circuit initialization process.

Finished circuit initialization process.

>wallace_using__functions_tb_isim_beh.exe -tclbatch isim.tcl -wdb wallace_using__functions_tb_isim_

ISim P.20131013 (signature 0x7708f090)

WARNING: A WEBPACK license was found.

WARNING: Please use Xilinx License Configuration Manager to check out a full ISim license.

WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for more information on t

This is a Lite version of ISim.

Time resolution is 1 ps

Simulator is doing circuit initialization process.

at 0 ps: Note: Stage: 0 of 3 (/wallace_add_using__functions_tb/UUT/).

at 0 ps: Note: Bit#/Total 10/0EA: 0HA: 0C: 0W: 0 (/wallace_add_using__functions_tb/UUT/).

at 0 ps: Note: Bit#/Total 9/0EA: 0HA: 0C: 0W: 0 (/wallace_add_using__functions_tb/UUT/).

at 0 ps: Note: Bit#/Total 8/0EA: 0HA: 0C: 3W: 0 (/wallace_add_using__functions_tb/UUT/).

at 0 ps: Note: Bit#/Total 7/8EA: 2HA: 1C: 3W: 0 (/wallace_add_using__functions_tb/UUT/).

at 0 ps: Note: Bit#/Total 6/8EA: 2HA: 1C: 3W: 0 (/wallace_add_using__functions_tb/UUT/).

at 0 ps: Note: Bit#/Total 5/8EA: 2HA: 1C: 3W: 0 (/wallace_add_using__functions_tb/UUT/).

at 0 ps: Note: Bit#/Total 4/8EA: 2HA: 1C: 3W: 0 (/wallace_add_using__functions_tb/UUT/).

at 0 ps: Note: Bit#/Total 3/8EA: 2HA: 1C: 3W: 0 (/wallace_add_using__functions_tb/UUT/).

at 0 ps: Note: Bit#/Total 2/8EA: 2HA: 1C: 3W: 0 (/wallace_add_using__functions_tb/UUT/).

at 0 ps: Note: Bit#/Total 1/8EA: 2HA: 1C: 3W: 0 (/wallace_add_using__functions_tb/UUT/).

at 0 ps: Note: Bit#/Total 0/8EA: 2HA: 1C: 0W: 0 (/wallace_add_using__functions_tb/UUT/).

at 0 ps: Note: Stage: 1 of 3 (/wallace_add_using__functions_tb/UUT/).

at 0 ps: Note: Bit#/Total 10/0EA: 0HA: 0C: 0W: 0 (/wallace_add_using__functions_tb/UUT/).

at 0 ps: Note: Bit#/Total 9/0EA: 0HA: 0C: 1W: 0 (/wallace_add_using__functions_tb/UUT/).

at 0 ps: Note: Bit#/Total 8/3EA: 1HA: 0C: 2W: 0 (/wallace_add_using__functions_tb/UUT/).

at 0 ps: Note: Bit#/Total 7/6EA: 2HA: 0C: 2W: 0 (/wallace_add_using__functions_tb/UUT/).

at 0 ps: Note: Bit#/Total 6/6EA: 2HA: 0C: 2W: 0 (/wallace_add_using__functions_tb/UUT/).

at 0 ps: Note: Bit#/Total 5/6EA: 2HA: 0C: 2W: 0 (/wallace_add_using__functions_tb/UUT/).

at 0 ps: Note: Bit#/Total 4/6EA: 2HA: 0C: 2W: 0 (/wallace_add_using__functions_tb/UUT/).

at 0 ps: Note: Bit#/Total 3/6EA: 2HA: 0C: 2W: 0 (/wallace_add_using__functions_tb/UUT/).

at 0 ps: Note: Bit#/Total 2/6EA: 2HA: 0C: 2W: 0 (/wallace_add_using__functions_tb/UUT/).

at 0 ps: Note: Bit#/Total 1/6EA: 2HA: 0C: 1W: 0 (/wallace_add_using__functions_tb/UUT/).

at 0 ps: Note: Bit#/Total 0/3EA: 1HA: 0C: 0W: 0 (/wallace_add_using__functions_tb/UUT/).

at 0 ps: Note: Stage: 2 of 3 (/wallace_add_using__functions_tb/UUT/).

at 0 ps: Note: Bit#/Total 10/0EA: 0HA: 0C: 0W: 0 (/wallace_add_using__functions_tb/UUT/).

at 0 ps: Note: Bit#/Total 9/1EA: 0HA: 0C: 1W: 1 (/wallace_add_using__functions_tb/UUT/).

at 0 ps: Note: Bit#/Total 8/3EA: 1HA: 0C: 1W: 0 (/wallace_add_using__functions_tb/UUT/).

at 0 ps: Note: Bit#/Total 7/4EA: 1HA: 0C: 1W: 1 (/wallace_add_using__functions_tb/UUT/).

at 0 ps: Note: Bit#/Total 6/4EA: 1HA: 0C: 1W: 1 (/wallace_add_using__functions_tb/UUT/).

at 0 ps: Note: Bit#/Total 5/4EA: 1HA: 0C: 1W: 1 (/wallace_add_using__functions_tb/UUT/).

at 0 ps: Note: Bit#/Total 4/4EA: 1HA: 0C: 1W: 1 (/wallace_add_using__functions_tb/UUT/).

at 0 ps: Note: Bit#/Total 3/4EA: 1HA: 0C: 1W: 1 (/wallace_add_using__functions_tb/UUT/).

at 0 ps: Note: Bit#/Total 2/4EA: 1HA: 0C: 1W: 1 (/wallace_add_using__functions_tb/UUT/).

at 0 ps: Note: Bit#/Total 1/3EA: 1HA: 0C: 0W: 0 (/wallace_add_using__functions_tb/UUT/).

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at 800 ns(6): Note: Bit#/Total 4/3EA: 1HA: 0C: 1W: 0 (/wallace_add_using__functions_tb/UUT/).

at 800 ns(6): Note: Bit#/Total 3/3EA: 1HA: 0C: 1W: 0 (/wallace_add_using__functions_tb/UUT/).

at 800 ns(6): Note: Bit#/Total 2/3EA: 1HA: 0C: 0W: 0 (/wallace_add_using__functions_tb/UUT/).

at 800 ns(6): Note: Bit#/Total 1/1EA: 0HA: 0C: 0W: 1 (/wallace_add_using__functions_tb/UUT/).

at 800 ns(6): Note: Bit#/Total 0/1EA: 0HA: 0C: 0W: 1 (/wallace_add_using__functions_tb/UUT/).

at 800 ns(6): Note: Last stage (/wallace_add_using__functions_tb/UUT/).

>Wallace_tree_functions_detailed_tb_5x4_isim_beh.exe -tclbatch isim.tcl -wdb Wallace_tree_functions

ISim P.20131013 (signature 0x7708f090)

WARNING: A WEBPACK license was found.

WARNING: Please use Xilinx License Configuration Manager to check out a full ISim license.

WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for more information on t

This is a Lite version of ISim.

Time resolution is 1 ps

Simulator is doing circuit initialization process.

Finished circuit initialization process.

>Wallace_tree_functions_detailed_tb_6x5_isim_beh.exe -tclbatch isim.tcl -wdb Wallace_tree_functions

ISim P.20131013 (signature 0x7708f090)

WARNING: A WEBPACK license was found.

WARNING: Please use Xilinx License Configuration Manager to check out a full ISim license.

WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for more information on t

This is a Lite version of ISim.

Time resolution is 1 ps

Simulator is doing circuit initialization process.

Finished circuit initialization process.

>Wallace_tree_functions_detailed_tb_7x6_isim_beh.exe -tclbatch isim.tcl -wdb Wallace_tree_functions

ISim P.20131013 (signature 0x7708f090)

WARNING: A WEBPACK license was found.

WARNING: Please use Xilinx License Configuration Manager to check out a full ISim license.

WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for more information on t

This is a Lite version of ISim.

Time resolution is 1 ps

Simulator is doing circuit initialization process.

Finished circuit initialization process.

>Wallace_tree_functions_detailed_tb_8x7_isim_beh.exe -tclbatch isim.tcl -wdb Wallace_tree_functions

ISim P.20131013 (signature 0x7708f090)

WARNING: A WEBPACK license was found.

WARNING: Please use Xilinx License Configuration Manager to check out a full ISim license.

WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for more information on t

This is a Lite version of ISim.

Time resolution is 1 ps

Simulator is doing circuit initialization process.

Finished circuit initialization process.

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o.prj -top wallace_add_using__functions_tb

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ns_detailed_tb.prj -top Wallace_tree_functions_detailed_tb -generic_top "width=5" -generic_top "nrargs

ns_detailed_tb.prj -top Wallace_tree_functions_detailed_tb -generic_top "width=6" -generic_top "nrargs

ns_detailed_tb.prj -top Wallace_tree_functions_detailed_tb -generic_top "width=7" -generic_top "nrargs

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;-detailed_tb_5x4_isim_beh.wdb

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;-detailed_tb_6x5_isim_beh.wdb

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;-detailed_tb_7x6_isim_beh.wdb

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;-detailed_tb_8x7_isim_beh.wdb

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