

Primerjava porabe primitivov in zakasnitve vezja

Vpisna številka	Vseh Primitivov	LUT3	LUT4	LUT6	Zakasnitev vezja	Vseh Primitivov	LUT3	LUT4	LUT5	LUT6	Zakasnitev vezja
64000225	BELS:1555	LUT3:1088	LUT4:208	LUT6:259	10.106ns	BELS:6			LUT5:3	LUT6:3	6.355ns
64190088	BELS:1555	LUT3:1088	LUT4:208	LUT6:259	10.106ns	BELS:59		LUT4:3		LUT6:32	7.522ns
64200100	BELS:1555	LUT3:1088	LUT4:208	LUT6:259	10.106ns	BELS:59		LUT4:3		LUT6:32	7.522ns
64200112	BELS:1555	LUT3:1088	LUT4:208	LUT6:259	10.106ns	BELS:59		LUT4:3		LUT6:32	7.522ns
64200163	BELS:1555	LUT3:1088	LUT4:208	LUT6:259	10.106ns	BELS:59		LUT4:3		LUT6:32	7.522ns
64200238	BELS:1555	LUT3:1088	LUT4:208	LUT6:259	10.106ns	BELS:59		LUT4:3		LUT6:32	7.522ns
64200288	BELS:1555	LUT3:1088	LUT4:208	LUT6:259	10.106ns	BELS:59		LUT4:3		LUT6:32	7.522ns
64200296	BELS:1555	LUT3:1088	LUT4:208	LUT6:259	10.106ns	BELS:59		LUT4:3		LUT6:32	7.522ns
64200385	BELS:1555	LUT3:1088	LUT4:208	LUT6:259	10.106ns	BELS:6			LUT5:3	LUT6:3	6.355ns
64210132	BELS:1555	LUT3:1088	LUT4:208	LUT6:259	10.106ns	BELS:59		LUT4:3		LUT6:32	7.522ns
64210290	BELS:1555	LUT3:1088	LUT4:208	LUT6:259	10.106ns	BELS:59		LUT4:3		LUT6:32	7.522ns
64210382	BELS:1555	LUT3:1088	LUT4:208	LUT6:259	10.106ns	BELS:59		LUT4:3		LUT6:32	7.522ns
64210384	BELS:1555	LUT3:1088	LUT4:208	LUT6:259	10.106ns	BELS:59		LUT4:3		LUT6:32	7.522ns
64210386	/	/	/	/	/	BELS:59		LUT4:3		LUT6:32	7.522ns
64210445	BELS:1556	/	/	LUT6:1555	10.106ns	BELS:59		LUT4:3		LUT6:32	7.522ns
64210455	BELS:1555	LUT3:1088	LUT4:208	LUT6:259	10.106ns	BELS:69	LUT3:4	LUT4:6	LUT5:11	LUT6:39	14.679ns
64210457	BELS:1555	LUT3:1088	LUT4:208	LUT6:259	10.106ns	BELS:59		LUT4:3		LUT6:32	7.522ns
64240429	BELS:1555	LUT3:1088	LUT4:208	LUT6:259	10.106ns	BELS:49		LUT4:1		LUT6:25	7.767ns
64240430	BELS:1555	LUT3:1088	LUT4:208	LUT6:259	10.106ns	BELS:6			LUT5:3	LUT6:3	6.355ns
IDEAL	BELS:1555	LUT3:1088	LUT4:208	LUT6:259	10.106ns	BELS:59		LUT4:3		LUT6:32	7.522ns

Kazalo

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Kazalo	2
-- **** STUDENT: 64000225	8
# BELS : 1555	12
# LUT3 : 1088	12
# LUT4 : 208	12
# LUT6 : 259	12
Maximum combinational path delay: 10.106ns	13
# BELS : 6	19
# LUT5 : 3	19
# LUT6 : 3	19
Maximum combinational path delay: 6.355ns	20
-- **** STUDENT: 64190088	22
# BELS : 1555	26
# LUT3 : 1088	26
# LUT4 : 208	26
# LUT6 : 259	26
Maximum combinational path delay: 10.106ns	27
# BELS : 59	33
# LUT4 : 3	33
# LUT6 : 32	33
Maximum combinational path delay: 7.522ns	34
-- **** STUDENT: 64200100	36
# BELS : 1555	40
# LUT3 : 1088	40
# LUT4 : 208	40
# LUT6 : 259	40
Maximum combinational path delay: 10.106ns	41
# BELS : 59	47
# LUT4 : 3	47
# LUT6 : 32	47
Maximum combinational path delay: 7.522ns	48
-- **** STUDENT: 64200112	50
# BELS : 1555	54
# LUT3 : 1088	54
# LUT4 : 208	54
# LUT6 : 259	54
Maximum combinational path delay: 10.106ns	55
# BELS : 59	61
# LUT4 : 3	61
# LUT6 : 32	61
Maximum combinational path delay: 7.522ns	62
-- **** STUDENT: 64200163	64
# BELS : 1555	68
# LUT3 : 1088	68
# LUT4 : 208	68
# LUT6 : 259	68

Maximum combinational path delay: 10.106ns	69
# BELS : 59	75
# LUT4 : 3	75
# LUT6 : 32	75
Maximum combinational path delay: 7.522ns	76
-- **** STUDENT: 64200238	78
# BELS : 1555	82
# LUT3 : 1088	82
# LUT4 : 208	82
# LUT6 : 259	82
Maximum combinational path delay: 10.106ns	83
# BELS : 59	89
# LUT4 : 3	89
# LUT6 : 32	89
Maximum combinational path delay: 7.522ns	90
-- **** STUDENT: 64200288	92
# BELS : 1555	96
# LUT3 : 1088	96
# LUT4 : 208	96
# LUT6 : 259	96
Maximum combinational path delay: 10.106ns	97
# BELS : 59	103
# LUT4 : 3	103
# LUT6 : 32	103
Maximum combinational path delay: 7.522ns	104
-- **** STUDENT: 64200296	106
# BELS : 1555	110
# LUT3 : 1088	110
# LUT4 : 208	110
# LUT6 : 259	110
Maximum combinational path delay: 10.106ns	111
# BELS : 59	117
# LUT4 : 3	117
# LUT6 : 32	117
Maximum combinational path delay: 7.522ns	118
-- **** STUDENT: 64200385	120
# BELS : 1555	124
# LUT3 : 1088	124
# LUT4 : 208	124
# LUT6 : 259	124
Maximum combinational path delay: 10.106ns	125
# BELS : 6	131
# LUT5 : 3	131
# LUT6 : 3	131
Maximum combinational path delay: 6.355ns	132
-- **** STUDENT: 64210132	134
# BELS : 1555	138
# LUT3 : 1088	138
# LUT4 : 208	138
# LUT6 : 259	138

Maximum combinational path delay: 10.106ns	139
# BELS : 59	145
# LUT4 : 3	145
# LUT6 : 32	145
Maximum combinational path delay: 7.522ns	146
-- **** STUDENT: 64210290	148
# BELS : 1555	152
# LUT3 : 1088	152
# LUT4 : 208	152
# LUT6 : 259	152
Maximum combinational path delay: 10.106ns	153
# BELS : 59	159
# LUT4 : 3	159
# LUT6 : 32	159
Maximum combinational path delay: 7.522ns	160
-- **** STUDENT: 64210382	162
# BELS : 1555	166
# LUT3 : 1088	166
# LUT4 : 208	166
# LUT6 : 259	166
Maximum combinational path delay: 10.106ns	167
# BELS : 59	173
# LUT4 : 3	173
# LUT6 : 32	173
Maximum combinational path delay: 7.522ns	174
-- **** STUDENT: 64210384	176
# BELS : 1555	180
# LUT3 : 1088	180
# LUT4 : 208	180
# LUT6 : 259	180
Maximum combinational path delay: 10.106ns	181
# BELS : 59	187
# LUT4 : 3	187
# LUT6 : 32	187
Maximum combinational path delay: 7.522ns	188
-- **** STUDENT: 64210386	190
# BELS : 59	196
# LUT4 : 3	196
# LUT6 : 32	196
Maximum combinational path delay: 7.522ns	197
-- **** STUDENT: 64210445	200
# BELS : 1556	205
# LUT6 : 1555	205
Maximum combinational path delay: 10.106ns	206
# BELS : 59	211
# LUT4 : 3	211
# LUT6 : 32	211
Maximum combinational path delay: 7.522ns	212
-- **** STUDENT: 64210455	214
# BELS : 1555	218

# LUT3 : 1088	218
# LUT4 : 208	218
# LUT6 : 259	218
Maximum combinational path delay: 10.106ns	219
# BELS : 69	225
# LUT3 : 4	225
# LUT4 : 6	225
# LUT5 : 11	225
# LUT6 : 39	225
Maximum combinational path delay: 14.679ns	226
-- **** STUDENT: 64210457	229
# BELS : 1555	233
# LUT3 : 1088	233
# LUT4 : 208	233
# LUT6 : 259	233
Maximum combinational path delay: 10.106ns	234
# BELS : 59	240
# LUT4 : 3	240
# LUT6 : 32	240
Maximum combinational path delay: 7.522ns	241
-- **** STUDENT: 64240429	243
# BELS : 1555	247
# LUT3 : 1088	247
# LUT4 : 208	247
# LUT6 : 259	247
Maximum combinational path delay: 10.106ns	248
# BELS : 49	254
# LUT4 : 1	254
# LUT6 : 25	254
Maximum combinational path delay: 7.767ns	255
-- **** STUDENT: 64240430	257
# BELS : 1555	261
# LUT3 : 1088	261
# LUT4 : 208	261
# LUT6 : 259	261
Maximum combinational path delay: 10.106ns	262
# BELS : 6	268
# LUT5 : 3	268
# LUT6 : 3	268
Maximum combinational path delay: 6.355ns	269
-- **** STUDENT: IDEAL	271
# BELS : 1555	275
# LUT3 : 1088	275
# LUT4 : 208	275
# LUT6 : 259	275
Maximum combinational path delay: 10.106ns	276
# BELS : 59	282
# LUT4 : 3	282
# LUT6 : 32	282
Maximum combinational path delay: 7.522ns	283


```
-- *****
-- **** STUDENT: 64000225
-- *****
-- KOMENTARJI K OCENI NALOGE
-- Matej Možek: Ni pripomb
-- *****
```

```
64000225>if not exist "xst" mkdir xst
```

```
64000225>cd XST
```

```
64000225\xst>if not exist "projnav.tmp" mkdir "projnav.tmp"
```

```
64000225\xst>cd ..
```

```
64000225>xst -ifn unary_tree.xst
Release 14.7 - xst P.20131013 (nt64)
Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.
--> Parameter TMPDIR set to xst/projnav.tmp
```

```
Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.32 secs
```

```
--> Parameter xsthdpdir set to xst
```

```
Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.33 secs
```

```
-->
```

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```
=====
*      Synthesis Options Summary      *
=====
```

---- Source Parameters

```
Input File Name      : "unary_tree.prj"
Ignore Synthesis Constraint File : NO
```

---- Target Parameters

```
Output File Name     : "Unary_Op_Bin_Tree"
```


Output Format : NGC
Target Device : xc6slx4-3-tqg144

----- Source Options

Top Module Name : Unary_Op_Bin_Tree
Automatic FSM Extraction : YES
FSM Encoding Algorithm : Auto
Safe Implementation : No
FSM Style : LUT
RAM Extraction : Yes
RAM Style : Auto
ROM Extraction : Yes
Shift Register Extraction : YES
ROM Style : Auto
Resource Sharing : YES
Asynchronous To Synchronous : NO
Shift Register Minimum Size : 2
Use DSP Block : Auto
Automatic Register Balancing : No

----- Target Options

LUT Combining : Auto
Reduce Control Sets : Auto
Add IO Buffers : YES
Global Maximum Fanout : 100000
Add Generic Clock Buffer(BUFG) : 16
Register Duplication : YES
Optimize Instantiated Primitives : NO
Use Clock Enable : Auto
Use Synchronous Set : Auto
Use Synchronous Reset : Auto
Pack IO Registers into IOBs : Auto
Equivalent register Removal : YES

----- General Options

Optimization Goal : Speed
Optimization Effort : 1
Power Reduction : NO
Keep Hierarchy : No
Netlist Hierarchy : As_Optimized
RTL Output : Yes
Global Optimization : AllClockNets
Read Cores : YES
Write Timing Constraints : NO
Cross Clock Analysis : NO
Hierarchy Separator : /
Bus Delimiter : <>
Case Specifier : Maintain
Slice Utilization Ratio : 100
BRAM Utilization Ratio : 100
DSP48 Utilization Ratio : 100
Auto BRAM Packing : NO
Slice Utilization Ratio Delta : 5

=====

=====

* HDL Parsing *

=====

Parsing VHDL file "64000225\unary_op_xor_tree_lut6.vhd" into library work
Parsing entity <XorTreeStage>.
Parsing architecture <tree_of_xor_lut6> of entity <xortreestage>.
Parsing VHDL file "64000225\unary_op_tree.vhd" into library work
Parsing entity <Unary_Op_Bin_Tree>.
Parsing architecture <t> of entity <unary_op_bin_tree>.

```
=====
*          HDL Elaboration          *
=====
```

Elaborating entity <Unary_Op_Bin_Tree> (architecture <t>) with generics from library <work>.

Elaborating entity <XorTreeStage> (architecture <tree_of_xor_lut6>) with generics from library <work>.

Elaborating entity <XorTreeStage> (architecture <tree_of_xor_lut6>) with generics from library <work>.

Elaborating entity <XorTreeStage> (architecture <tree_of_xor_lut6>) with generics from library <work>.

Elaborating entity <XorTreeStage> (architecture <tree_of_xor_lut6>) with generics from library <work>.

Elaborating entity <XorTreeStage> (architecture <tree_of_xor_lut6>) with generics from library <work>.

Elaborating entity <XorTreeStage> (architecture <tree_of_xor_lut6>) with generics from library <work>.

Elaborating entity <XorTreeStage> (architecture <tree_of_xor_lut6>) with generics from library <work>.

Elaborating entity <XorTreeStage> (architecture <tree_of_xor_lut6>) with generics from library <work>.

Elaborating entity <XorTreeStage> (architecture <tree_of_xor_lut6>) with generics from library <work>.

```
=====
*          HDL Synthesis            *
=====
```

Synthesizing Unit <Unary_Op_Bin_Tree>.
Related source file is "64000225\unary_op_tree.vhd".
N = 4096
Summary:
no macro.
Unit <Unary_Op_Bin_Tree> synthesized.

Synthesizing Unit <XorTreeStage_1>.
Related source file is "64000225\unary_op_xor_tree_lut6.vhd".
N = 4096
Summary:
no macro.
Unit <XorTreeStage_1> synthesized.

Synthesizing Unit <XorTreeStage_2>.
Related source file is "64000225\unary_op_xor_tree_lut6.vhd".
N = 682
Summary:
no macro.
Unit <XorTreeStage_2> synthesized.

Synthesizing Unit <XorTreeStage_3>.
Related source file is "64000225\unary_op_xor_tree_lut6.vhd".
N = 113
Summary:
no macro.
Unit <XorTreeStage_3> synthesized.

Synthesizing Unit <XorTreeStage_4>.
Related source file is "64000225\unary_op_xor_tree_lut6.vhd".
N = 18
Summary:
no macro.
Unit <XorTreeStage_4> synthesized.

Synthesizing Unit <XorTreeStage_5>.
Related source file is "64000225\unary_op_xor_tree_lut6.vhd".
N = 3
Summary:
no macro.
Unit <XorTreeStage_5> synthesized.

Synthesizing Unit <XorTreeStage_6>.
Related source file is "64000225\unary_op_xor_tree_lut6.vhd".
N = 19
Summary:
no macro.
Unit <XorTreeStage_6> synthesized.

Synthesizing Unit <XorTreeStage_7>.
Related source file is "64000225\unary_op_xor_tree_lut6.vhd".
N = 4
Summary:
no macro.
Unit <XorTreeStage_7> synthesized.

Synthesizing Unit <XorTreeStage_8>.
Related source file is "64000225\unary_op_xor_tree_lut6.vhd".
N = 114
Summary:
no macro.
Unit <XorTreeStage_8> synthesized.

Synthesizing Unit <XorTreeStage_9>.
Related source file is "64000225\unary_op_xor_tree_lut6.vhd".
N = 683
Summary:
no macro.
Unit <XorTreeStage_9> synthesized.

=====
HDL Synthesis Report

Found no macro

```
=====
*      Advanced HDL Synthesis      *
=====
```

```
=====
Advanced HDL Synthesis Report
=====
```

Found no macro

```
=====
*      Low Level Synthesis      *
=====
```

Optimizing unit <Unary_Op_Bin_Tree> ...

Mapping all equations...

Building and optimizing final netlist ...

Found area constraint ratio of 100 (+ 5) on block Unary_Op_Bin_Tree, actual ratio is 94.

Final Macro Processing ...

```
=====
Final Register Report
=====
```

Found no macro

```
=====
*      Partition Report      *
=====
```

Partition Implementation Status

No Partitions were found in this design.

```
=====
*      Design Summary      *
=====
```

Top Level Output File Name : Unary_Op_Bin_Tree.ngc

Primitive and Black Box Usage:

# BELS	: 1555
# LUT3	: 1088
# LUT4	: 208
# LUT6	: 259
# IO Buffers	: 4097
# IBUF	: 4096
# OBUF	: 1

Device utilization summary:

Selected Device : 6slx4tqg144-3

Slice Logic Utilization:

Number of Slice LUTs: 1555 out of 2400 64%
Number used as Logic: 1555 out of 2400 64%

Slice Logic Distribution:

Number of LUT Flip Flop pairs used: 1555
Number with an unused Flip Flop: 1555 out of 1555 100%
Number with an unused LUT: 0 out of 1555 0%
Number of fully used LUT-FF pairs: 0 out of 1555 0%
Number of unique control sets: 0

IO Utilization:

Number of IOs: 4097
Number of bonded IOBs: 4097 out of 102 4016% (*)

Specific Feature Utilization:

WARNING:Xst:1336 - (*) More than 100% of Device resources are used

Partition Resource Summary:

No Partitions were found in this design.

=====

Timing Report

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.
FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT
GENERATED AFTER PLACE-and-ROUTE.

Clock Information:

No clock signals found in this design

Asynchronous Control Signals Information:

No asynchronous control signals found in this design

Timing Summary:

Speed Grade: -3

Minimum period: No path found
Minimum input arrival time before clock: No path found
Maximum output required time after clock: No path found
Maximum combinational path delay: 10.106ns

Timing Details:

All values displayed in nanoseconds (ns)

```

=====
Timing constraint: Default path analysis
Total number of paths / destination ports: 4096 / 1
-----
Delay: 10.106ns (Levels of Logic = 7)
Source: I<0> (PAD)
Destination: O_Xor (PAD)

Data Path: I<0> to O_Xor
Gate Net
Cell:in->out fanout Delay Delay Logical Name (Net Name)
-----
IBUF:I->O 1 1.222 0.808 I_0_IBUF (I_0_IBUF)
LUT3:I0->O 1 0.339 0.944
U_Xor/Stages.Sixth_1_Tree/Stages.Sixth_1_Tree/Stages.Sixth_1_Tree/Stages.Sixth_1_Tree/Stage_xor_3.XOR3_LUT
(U_Xor/Stages.Sixth_1_Tree/Stages.Sixth_1_Tree/Stages.Sixth_1_Tree/Stages.Sixth1_in)
LUT6:I0->O 1 0.203 0.944
U_Xor/Stages.Sixth_1_Tree/Stages.Sixth_1_Tree/Stages.Sixth_1_Tree/Stages.XOR6_LUT
(U_Xor/Stages.Sixth_1_Tree/Stages.Sixth_1_Tree/Stages.Sixth1_in)
LUT6:I0->O 1 0.203 0.944
U_Xor/Stages.Sixth_1_Tree/Stages.Sixth_1_Tree/Stages.XOR6_LUT
(U_Xor/Stages.Sixth_1_Tree/Stages.Sixth1_in)
LUT6:I0->O 1 0.203 0.944 U_Xor/Stages.Sixth_1_Tree/Stages.XOR6_LUT
(U_Xor/Stages.Sixth1_in)
LUT6:I0->O 1 0.203 0.579 U_Xor/Stages.XOR6_LUT (O_Xor_OBUF)
OBUF:I->O 2.571 O_Xor_OBUF (O_Xor)
-----
Total 10.106ns (4.944ns logic, 5.162ns route)
(48.9% logic, 51.1% route)

=====

Cross Clock Domains Report:
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=====

Total REAL time to Xst completion: 23.00 secs
Total CPU time to Xst completion: 23.50 secs

-->

Total memory usage is 4538348 kilobytes

Number of errors : 0 ( 0 filtered)
Number of warnings : 1 ( 0 filtered)
Number of infos : 0 ( 0 filtered)

64000225>fuse -incremental -o unary_tree_tb_isim_beh.exe -prj unary_tree_tb.prj -
top Unary_Op_Bin_Tree_tb
Running: C:\Xilinx\14.7\ISE_DS\ISE\bin\nt64\unwrapped\fuse.exe -incremental -o
unary_tree_tb_isim_beh.exe -prj unary_tree_tb.prj -top Unary_Op_Bin_Tree_tb
ISim P.20131013 (signature 0x7708f090)
Number of CPUs detected in this system: 8
Turning on mult-threading, number of parallel sub-compilation jobs: 16
Determining compilation order of HDL files

```

```

Parsing VHDL file "slv_image_pkg.vhd" into library work
Parsing VHDL file "unary_op_xor_tree_lut6.vhd" into library work
Parsing VHDL file "unary_op_tree.vhd" into library work
Parsing VHDL file "unary_op_tree_IDEAL_tb.vhd" into library work
Starting static elaboration
Completed static elaboration
Compiling package standard
Compiling package std_logic_1164
Compiling package numeric_std
Compiling package textio
Compiling package std_logic_textio
Compiling package slv_image_pkg
Compiling package vcomponents
Compiling package vital_timing
Compiling package vital_primitives
Compiling package vpkg
Compiling architecture tree_of_xor_lut6 of entity XorTreeStage [\XorTreeStage(2)\]
Compiling architecture lut3_v of entity LUT3 [\LUT3("10010110")(0,7)\]
Compiling architecture tree_of_xor_lut6 of entity XorTreeStage [\XorTreeStage(3)\]
Compiling architecture lut6_v of entity LUT6 [\LUT6("0110100110010110100101100...)]
Compiling architecture tree_of_xor_lut6 of entity XorTreeStage
[\XorTreeStage(16)\]
Compiling architecture t of entity Unary_Op_Bin_Tree [\Unary_Op_Bin_Tree(16)\]
Compiling architecture test of entity unary_op_bin_tree_tb
Time Resolution for simulation is 1ps.
Waiting for 1 sub-compilation(s) to finish...
Compiled 23 VHDL Units
Built simulation executable unary_tree_tb_isim_beh.exe
Fuse Memory Usage: 58344 KB
Fuse CPU Usage: 1203 ms

```

```
64000225>if exist Unary_Op_Bin_Tree.csv del Unary_Op_Bin_Tree.csv
```

```
64000225>if exist Unary_Op_Bin_Tree_64000225.csv del
Unary_Op_Bin_Tree_64000225.csv
```

```

64000225>unary_tree_tb_isim_beh.exe -tclbatch isim.tcl -wdb
unary_tree_tb_isim_beh.wdb
ISim P.20131013 (signature 0x7708f090)
WARNING: A WEBPACK license was found.
WARNING: Please use Xilinx License Configuration Manager to check out a full ISim
license.
WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for
more information on the differences between the Lite and the Full version.
This is a Lite version of ISim.
Time resolution is 1 ps
Simulator is doing circuit initialization process.
Finished circuit initialization process.

```

```
64000225>rem ren Unary_Op_Bin_Tree.csv Unary_Op_Bin_Tree_64000225.csv
```

```

64000225>xst -ifn unary_vhdl93.xst
Release 14.7 - xst P.20131013 (nt64)
Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.
--> Parameter TMPDIR set to xst/projnav.tmp

```

```

Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.24 secs

```

--> Parameter xsthdpdir set to xst

Total REAL time to Xst completion: 0.00 secs

Total CPU time to Xst completion: 0.24 secs

-->

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```
=====
*      Synthesis Options Summary      *
```

----- Source Parameters

Input File Name : "./unary_vhdl93.prj"
Ignore Synthesis Constraint File : NO

----- Target Parameters

Output File Name : "reduction_operators"
Output Format : NGC
Target Device : xc6slx4-3-tqg144

----- Source Options

Top Module Name : reduction_operators
Automatic FSM Extraction : YES
FSM Encoding Algorithm : Auto
Safe Implementation : No
FSM Style : LUT
RAM Extraction : Yes
RAM Style : Auto
ROM Extraction : Yes
Shift Register Extraction : YES
ROM Style : Auto
Resource Sharing : YES
Asynchronous To Synchronous : NO
Shift Register Minimum Size : 2
Use DSP Block : Auto
Automatic Register Balancing : No

----- Target Options

LUT Combining : Auto
Reduce Control Sets : Auto

Add IO Buffers : YES
Global Maximum Fanout : 100000
Add Generic Clock Buffer(BUFG) : 16
Register Duplication : YES
Optimize Instantiated Primitives : NO
Use Clock Enable : Auto
Use Synchronous Set : Auto
Use Synchronous Reset : Auto
Pack IO Registers into IOBs : Auto
Equivalent register Removal : YES

---- General Options

Optimization Goal : Speed
Optimization Effort : 1
Power Reduction : NO
Keep Hierarchy : No
Netlist Hierarchy : As_Optimized
RTL Output : Yes
Global Optimization : AllClockNets
Read Cores : YES
Write Timing Constraints : NO
Cross Clock Analysis : NO
Hierarchy Separator : /
Bus Delimiter : <>
Case Specifier : Maintain
Slice Utilization Ratio : 100
BRAM Utilization Ratio : 100
DSP48 Utilization Ratio : 100
Auto BRAM Packing : NO
Slice Utilization Ratio Delta : 5

=====

=====

* HDL Parsing *

=====

Parsing VHDL file "64000225\unary_operators_vhdl_93.vhd" into library work
Parsing entity <reduction_operators>.
Parsing architecture <vhdl_93_process> of entity <reduction_operators>.

=====

* HDL Elaboration *

=====

Elaborating entity <reduction_operators> (architecture <vhdl_93_process>) with
generics from library <work>.

=====

* HDL Synthesis *

=====

Synthesizing Unit <reduction_operators>.

Related source file is "64000225\unary_operators_vhdl_93.vhd".

N = 10

Summary:

inferred 29 Multiplexer(s).

Unit <reduction_operators> synthesized.

=====

HDL Synthesis Report

Macro Statistics

Multiplexers : 29
1-bit 2-to-1 multiplexer : 29

=====

* Advanced HDL Synthesis *

=====

Advanced HDL Synthesis Report

Macro Statistics

Multiplexers : 29
1-bit 2-to-1 multiplexer : 29

=====

* Low Level Synthesis *

=====

Optimizing unit <reduction_operators> ...

Mapping all equations...

Building and optimizing final netlist ...

Found area constraint ratio of 100 (+ 5) on block reduction_operators, actual ratio is 0.

Final Macro Processing ...

Final Register Report

Found no macro

=====

* Partition Report *

=====

Partition Implementation Status

No Partitions were found in this design.

=====

* Design Summary *

=====

Top Level Output File Name : reduction_operators.ngc

Primitive and Black Box Usage:

```
# BELS      : 6
# LUT5      : 3
# LUT6      : 3
# IO Buffers : 13
# IBUF      : 10
# OBUF      : 3
```

Device utilization summary:

Selected Device : 6slx4tqg144-3

Slice Logic Utilization:

Number of Slice LUTs: 6 out of 2400 0%
Number used as Logic: 6 out of 2400 0%

Slice Logic Distribution:

Number of LUT Flip Flop pairs used: 6
Number with an unused Flip Flop: 6 out of 6 100%
Number with an unused LUT: 0 out of 6 0%
Number of fully used LUT-FF pairs: 0 out of 6 0%
Number of unique control sets: 0

IO Utilization:

Number of IOs: 13
Number of bonded IOBs: 13 out of 102 12%

Specific Feature Utilization:

Partition Resource Summary:

No Partitions were found in this design.

=====

Timing Report

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.
FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT
GENERATED AFTER PLACE-and-ROUTE.

Clock Information:

No clock signals found in this design

Asynchronous Control Signals Information:

No asynchronous control signals found in this design

Timing Summary:

Speed Grade: -3

Minimum period: No path found
Minimum input arrival time before clock: No path found
Maximum output required time after clock: No path found

Maximum combinational path delay: 6.355ns

Timing Details:

All values displayed in nanoseconds (ns)

=====

Timing constraint: Default path analysis

Total number of paths / destination ports: 30 / 3

Delay: 6.355ns (Levels of Logic = 4)

Source: A<4> (PAD)

Destination: reduced_OR (PAD)

Data Path: A<4> to reduced_OR

Gate Net

Cell:in->out fanout Delay Delay Logical Name (Net Name)

IBUF:I->O	3	1.222	0.995	A_4_IBUF	(A_4_IBUF)
-----------	---	-------	-------	----------	------------

LUT5:I0->O	1	0.203	0.580	Mmux_reduced_OR3_SW0	(N01)
------------	---	-------	-------	----------------------	-------

LUT6:I5->O	1	0.205	0.579	Mmux_reduced_OR3	(reduced_OR_OBUF)
------------	---	-------	-------	------------------	-------------------

OBUF:I->O		2.571		reduced_OR_OBUF	(reduced_OR)
-----------	--	-------	--	-----------------	--------------

Total 6.355ns (4.201ns logic, 2.154ns route)
(66.1% logic, 33.9% route)

Cross Clock Domains Report:

=====

Total REAL time to Xst completion: 8.00 secs

Total CPU time to Xst completion: 8.52 secs

-->

Total memory usage is 4487516 kilobytes

Number of errors : 0 (0 filtered)

Number of warnings : 0 (0 filtered)

Number of infos : 0 (0 filtered)

64000225>fuse -incremental -o unary_vhdl93_tb_isim_beh.exe -prj

unary_vhdl93_tb.prj -top reduction_operators_tb

Running: C:\Xilinx\14.7\ISE_DS\ISE\bin\nt64\unwrapped\fuse.exe -incremental -o

unary_vhdl93_tb_isim_beh.exe -prj unary_vhdl93_tb.prj -top reduction_operators_tb

ISim P.20131013 (signature 0x7708f090)

Number of CPUs detected in this system: 8

Turning on mult-threading, number of parallel sub-compilation jobs: 16

Determining compilation order of HDL files

Parsing VHDL file "unary_operators_vhdl_93.vhd" into library work

Parsing VHDL file "unary_operators_vhdl93_IDEAL_tb.vhd" into library work

Starting static elaboration

Completed static elaboration

Compiling package standard

Compiling package std_logic_1164

Compiling package numeric_std

```
Compiling package textio
Compiling package std_logic_textio
Compiling architecture vhdl_93_process of entity reduction_operators
[\reduction_operators(3)\]
Compiling architecture test of entity reduction_operators_tb
Time Resolution for simulation is 1ps.
Waiting for 1 sub-compilation(s) to finish...
Compiled 8 VHDL Units
Built simulation executable unary_vhdl93_tb_isim_beh.exe
Fuse Memory Usage: 36764 KB
Fuse CPU Usage: 905 ms
```

```
64000225>if exist reduction_operators.csv del reduction_operators.csv
```

```
64000225>if exist reduction_operators_64000225.csv del
reduction_operators_64000225.csv
```

```
64000225>unary_vhdl93_tb_isim_beh.exe -tclbatch isim.tcl -wdb
unary_vhdl93_tb_isim_beh.wdb
ISim P.20131013 (signature 0x7708f090)
WARNING: A WEBPACK license was found.
WARNING: Please use Xilinx License Configuration Manager to check out a full ISim
license.
WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for
more information on the differences between the Lite and the Full version.
This is a Lite version of ISim.
Time resolution is 1 ps
Simulator is doing circuit initialization process.
Finished circuit initialization process.
```

```
64000225>rem ren reduction_operators.csv reduction_operators_64000225.csv
```

```
-- *****
-- **** STUDENT: 64190088
-- *****
-- KOMENTARJI K OCENI NALOGE
-- Matej Možek: Ni pripomb
-- *****
```

```
64190088>if not exist "xst" mkdir xst
```

```
64190088>cd XST
```

```
64190088\xst>if not exist "projnav.tmp" mkdir "projnav.tmp"
```

```
64190088\xst>cd ..
```

```
64190088>xst -ifn unary_tree.xst
Release 14.7 - xst P.20131013 (nt64)
Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.
--> Parameter TMPDIR set to xst/projnav.tmp
```

```
Total REAL time to Xst completion: 1.00 secs
Total CPU time to Xst completion: 0.24 secs
```

```
--> Parameter xsthdpdir set to xst
```

```
Total REAL time to Xst completion: 1.00 secs
Total CPU time to Xst completion: 0.25 secs
```

```
-->
```

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```
=====
*      Synthesis Options Summary      *
=====
```

---- Source Parameters

```
Input File Name      : "unary_tree.prj"
Ignore Synthesis Constraint File : NO
```

---- Target Parameters

```
Output File Name     : "Unary_Op_Bin_Tree"
```

Output Format : NGC
Target Device : xc6slx4-3-tqg144

----- Source Options

Top Module Name : Unary_Op_Bin_Tree
Automatic FSM Extraction : YES
FSM Encoding Algorithm : Auto
Safe Implementation : No
FSM Style : LUT
RAM Extraction : Yes
RAM Style : Auto
ROM Extraction : Yes
Shift Register Extraction : YES
ROM Style : Auto
Resource Sharing : YES
Asynchronous To Synchronous : NO
Shift Register Minimum Size : 2
Use DSP Block : Auto
Automatic Register Balancing : No

----- Target Options

LUT Combining : Auto
Reduce Control Sets : Auto
Add IO Buffers : YES
Global Maximum Fanout : 100000
Add Generic Clock Buffer(BUFG) : 16
Register Duplication : YES
Optimize Instantiated Primitives : NO
Use Clock Enable : Auto
Use Synchronous Set : Auto
Use Synchronous Reset : Auto
Pack IO Registers into IOBs : Auto
Equivalent register Removal : YES

----- General Options

Optimization Goal : Speed
Optimization Effort : 1
Power Reduction : NO
Keep Hierarchy : No
Netlist Hierarchy : As_Optimized
RTL Output : Yes
Global Optimization : AllClockNets
Read Cores : YES
Write Timing Constraints : NO
Cross Clock Analysis : NO
Hierarchy Separator : /
Bus Delimiter : <>
Case Specifier : Maintain
Slice Utilization Ratio : 100
BRAM Utilization Ratio : 100
DSP48 Utilization Ratio : 100
Auto BRAM Packing : NO
Slice Utilization Ratio Delta : 5

=====

=====

* HDL Parsing *

=====

Parsing VHDL file "64190088\unary_op_xor_tree_lut6.vhd" into library work
Parsing entity <XorTreeStage>.
Parsing architecture <tree_of_xor_lut6> of entity <xortreestage>.
Parsing VHDL file "64190088\unary_op_tree.vhd" into library work
Parsing entity <Unary_Op_Bin_Tree>.
Parsing architecture <t> of entity <unary_op_bin_tree>.

```
=====
*          HDL Elaboration          *
=====
```

Elaborating entity <Unary_Op_Bin_Tree> (architecture <t>) with generics from library <work>.

Elaborating entity <XorTreeStage> (architecture <tree_of_xor_lut6>) with generics from library <work>.

Elaborating entity <XorTreeStage> (architecture <tree_of_xor_lut6>) with generics from library <work>.

Elaborating entity <XorTreeStage> (architecture <tree_of_xor_lut6>) with generics from library <work>.

Elaborating entity <XorTreeStage> (architecture <tree_of_xor_lut6>) with generics from library <work>.

Elaborating entity <XorTreeStage> (architecture <tree_of_xor_lut6>) with generics from library <work>.

Elaborating entity <XorTreeStage> (architecture <tree_of_xor_lut6>) with generics from library <work>.

Elaborating entity <XorTreeStage> (architecture <tree_of_xor_lut6>) with generics from library <work>.

Elaborating entity <XorTreeStage> (architecture <tree_of_xor_lut6>) with generics from library <work>.

Elaborating entity <XorTreeStage> (architecture <tree_of_xor_lut6>) with generics from library <work>.

```
=====
*          HDL Synthesis            *
=====
```

Synthesizing Unit <Unary_Op_Bin_Tree>.
Related source file is "64190088\unary_op_tree.vhd".
N = 4096
Summary:
no macro.
Unit <Unary_Op_Bin_Tree> synthesized.

Synthesizing Unit <XorTreeStage_1>.
Related source file is "64190088\unary_op_xor_tree_lut6.vhd".
N = 4096
Summary:
no macro.
Unit <XorTreeStage_1> synthesized.

Synthesizing Unit <XorTreeStage_2>.
Related source file is "64190088\unary_op_xor_tree_lut6.vhd".
N = 682
Summary:
no macro.
Unit <XorTreeStage_2> synthesized.

Synthesizing Unit <XorTreeStage_3>.
Related source file is "64190088\unary_op_xor_tree_lut6.vhd".
N = 113
Summary:
no macro.
Unit <XorTreeStage_3> synthesized.

Synthesizing Unit <XorTreeStage_4>.
Related source file is "64190088\unary_op_xor_tree_lut6.vhd".
N = 18
Summary:
no macro.
Unit <XorTreeStage_4> synthesized.

Synthesizing Unit <XorTreeStage_5>.
Related source file is "64190088\unary_op_xor_tree_lut6.vhd".
N = 3
Summary:
no macro.
Unit <XorTreeStage_5> synthesized.

Synthesizing Unit <XorTreeStage_6>.
Related source file is "64190088\unary_op_xor_tree_lut6.vhd".
N = 19
Summary:
no macro.
Unit <XorTreeStage_6> synthesized.

Synthesizing Unit <XorTreeStage_7>.
Related source file is "64190088\unary_op_xor_tree_lut6.vhd".
N = 4
Summary:
no macro.
Unit <XorTreeStage_7> synthesized.

Synthesizing Unit <XorTreeStage_8>.
Related source file is "64190088\unary_op_xor_tree_lut6.vhd".
N = 114
Summary:
no macro.
Unit <XorTreeStage_8> synthesized.

Synthesizing Unit <XorTreeStage_9>.
Related source file is "64190088\unary_op_xor_tree_lut6.vhd".
N = 683
Summary:
no macro.
Unit <XorTreeStage_9> synthesized.

=====
HDL Synthesis Report

Found no macro

```
=====
*      Advanced HDL Synthesis      *
=====
```

```
=====
Advanced HDL Synthesis Report
=====
```

Found no macro

```
=====
*      Low Level Synthesis      *
=====
```

Optimizing unit <Unary_Op_Bin_Tree> ...

Mapping all equations...

Building and optimizing final netlist ...

Found area constraint ratio of 100 (+ 5) on block Unary_Op_Bin_Tree, actual ratio is 94.

Final Macro Processing ...

```
=====
Final Register Report
=====
```

Found no macro

```
=====
*      Partition Report      *
=====
```

Partition Implementation Status

No Partitions were found in this design.

```
=====
*      Design Summary      *
=====
```

Top Level Output File Name : Unary_Op_Bin_Tree.ngc

Primitive and Black Box Usage:

# BELS	: 1555
# LUT3	: 1088
# LUT4	: 208
# LUT6	: 259
# IO Buffers	: 4097
# IBUF	: 4096
# OBUF	: 1

Device utilization summary:

Selected Device : 6slx4tqg144-3

Slice Logic Utilization:

Number of Slice LUTs: 1555 out of 2400 64%
Number used as Logic: 1555 out of 2400 64%

Slice Logic Distribution:

Number of LUT Flip Flop pairs used: 1555
Number with an unused Flip Flop: 1555 out of 1555 100%
Number with an unused LUT: 0 out of 1555 0%
Number of fully used LUT-FF pairs: 0 out of 1555 0%
Number of unique control sets: 0

IO Utilization:

Number of IOs: 4097
Number of bonded IOBs: 4097 out of 102 4016% (*)

Specific Feature Utilization:

WARNING:Xst:1336 - (*) More than 100% of Device resources are used

Partition Resource Summary:

No Partitions were found in this design.

=====

Timing Report

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.
FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT
GENERATED AFTER PLACE-and-ROUTE.

Clock Information:

No clock signals found in this design

Asynchronous Control Signals Information:

No asynchronous control signals found in this design

Timing Summary:

Speed Grade: -3

Minimum period: No path found
Minimum input arrival time before clock: No path found
Maximum output required time after clock: No path found
Maximum combinational path delay: 10.106ns

Timing Details:

All values displayed in nanoseconds (ns)

```

=====
Timing constraint: Default path analysis
Total number of paths / destination ports: 4096 / 1
-----
Delay: 10.106ns (Levels of Logic = 7)
Source: I<0> (PAD)
Destination: O_Xor (PAD)

Data Path: I<0> to O_Xor
Gate Net
Cell:in->out fanout Delay Delay Logical Name (Net Name)
-----
IBUF:I->O 1 1.222 0.808 I_0_IBUF (I_0_IBUF)
LUT3:I0->O 1 0.339 0.944
U_Xor/Stages.Sixth1_Tree/Stages.Sixth1_Tree/Stages.Sixth1_Tree/Stages.Sixth1_Tree/
Stage_xor_3.XOR3_LUT
(U_Xor/Stages.Sixth1_Tree/Stages.Sixth1_Tree/Stages.Sixth1_Tree/Stages.Sixth1_xor)
LUT6:I0->O 1 0.203 0.944
U_Xor/Stages.Sixth1_Tree/Stages.Sixth1_Tree/Stages.Sixth1_Tree/Stages.XOR6_LUT
(U_Xor/Stages.Sixth1_Tree/Stages.Sixth1_Tree/Stages.Sixth1_xor)
LUT6:I0->O 1 0.203 0.944
U_Xor/Stages.Sixth1_Tree/Stages.Sixth1_Tree/Stages.XOR6_LUT
(U_Xor/Stages.Sixth1_Tree/Stages.Sixth1_xor)
LUT6:I0->O 1 0.203 0.944 U_Xor/Stages.Sixth1_Tree/Stages.XOR6_LUT
(U_Xor/Stages.Sixth1_xor)
LUT6:I0->O 1 0.203 0.579 U_Xor/Stages.XOR6_LUT (O_Xor_OBUF)
OBUF:I->O 2.571 O_Xor_OBUF (O_Xor)
-----
Total 10.106ns (4.944ns logic, 5.162ns route)
(48.9% logic, 51.1% route)
=====

```

Cross Clock Domains Report:

```

=====
Total REAL time to Xst completion: 17.00 secs
Total CPU time to Xst completion: 16.63 secs

```

-->

Total memory usage is 4538364 kilobytes

```

Number of errors : 0 ( 0 filtered)
Number of warnings : 1 ( 0 filtered)
Number of infos : 0 ( 0 filtered)

```

```

64190088>fuse -incremental -o unary_tree_tb_isim_beh.exe -prj unary_tree_tb.prj -
top Unary_Op_Bin_Tree_tb
Running: C:\Xilinx\14.7\ISE_DS\ISE\bin\nt64\unwrapped\fuse.exe -incremental -o
unary_tree_tb_isim_beh.exe -prj unary_tree_tb.prj -top Unary_Op_Bin_Tree_tb
ISim P.20131013 (signature 0x7708f090)
Number of CPUs detected in this system: 8
Turning on mult-threading, number of parallel sub-compilation jobs: 16
Determining compilation order of HDL files
Parsing VHDL file "slv_image_pkg.vhd" into library work

```

```

Parsing VHDL file "unary_op_xor_tree_lut6.vhd" into library work
Parsing VHDL file "unary_op_tree.vhd" into library work
Parsing VHDL file "unary_op_tree_IDEAL_tb.vhd" into library work
Starting static elaboration
Completed static elaboration
Compiling package standard
Compiling package std_logic_1164
Compiling package numeric_std
Compiling package textio
Compiling package std_logic_textio
Compiling package slv_image_pkg
Compiling package vcomponents
Compiling package vital_timing
Compiling package vital_primitives
Compiling package vpkg
Compiling architecture tree_of_xor_lut6 of entity XorTreeStage [\XorTreeStage(2)\]
Compiling architecture lut3_v of entity LUT3 [\LUT3("10010110")(0,7)\]
Compiling architecture tree_of_xor_lut6 of entity XorTreeStage [\XorTreeStage(3)\]
Compiling architecture lut6_v of entity LUT6 [\LUT6("0110100110010110100101100...)]
Compiling architecture tree_of_xor_lut6 of entity XorTreeStage
[\XorTreeStage(16)\]
Compiling architecture t of entity Unary_Op_Bin_Tree [\Unary_Op_Bin_Tree(16)\]
Compiling architecture test of entity unary_op_bin_tree_tb
Time Resolution for simulation is 1ps.
Waiting for 1 sub-compilation(s) to finish...
Compiled 23 VHDL Units
Built simulation executable unary_tree_tb_isim_beh.exe
Fuse Memory Usage: 59528 KB
Fuse CPU Usage: 1390 ms

```

```
64190088>if exist Unary_Op_Bin_Tree.csv del Unary_Op_Bin_Tree.csv
```

```
64190088>if exist Unary_Op_Bin_Tree_64190088.csv del
Unary_Op_Bin_Tree_64190088.csv
```

```

64190088>unary_tree_tb_isim_beh.exe -tclbatch isim.tcl -wdb
unary_tree_tb_isim_beh.wdb
ISim P.20131013 (signature 0x7708f090)
WARNING: A WEBPACK license was found.
WARNING: Please use Xilinx License Configuration Manager to check out a full ISim
license.
WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for
more information on the differences between the Lite and the Full version.
This is a Lite version of ISim.
Time resolution is 1 ps
Simulator is doing circuit initialization process.
Finished circuit initialization process.

```

```
64190088>rem ren Unary_Op_Bin_Tree.csv Unary_Op_Bin_Tree_64190088.csv
```

```

64190088>xst -ifn unary_vhdl93.xst
Release 14.7 - xst P.20131013 (nt64)
Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.
--> Parameter TMPDIR set to xst/projnav.tmp

```

```

Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.23 secs

```

```
--> Parameter xsthdpdir set to xst
```

Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.23 secs

-->

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 - 8.4.5) Cross Clock Domains Report

```
=====
*      Synthesis Options Summary      *
=====
```

---- Source Parameters

Input File Name : "./unary_vhdl93.prj"
Ignore Synthesis Constraint File : NO

---- Target Parameters

Output File Name : "reduction_operators"
Output Format : NGC
Target Device : xc6slx4-3-tqg144

---- Source Options

Top Module Name : reduction_operators
Automatic FSM Extraction : YES
FSM Encoding Algorithm : Auto
Safe Implementation : No
FSM Style : LUT
RAM Extraction : Yes
RAM Style : Auto
ROM Extraction : Yes
Shift Register Extraction : YES
ROM Style : Auto
Resource Sharing : YES
Asynchronous To Synchronous : NO
Shift Register Minimum Size : 2
Use DSP Block : Auto
Automatic Register Balancing : No

---- Target Options

LUT Combining : Auto
Reduce Control Sets : Auto
Add IO Buffers : YES

Global Maximum Fanout : 100000
Add Generic Clock Buffer(BUFG) : 16
Register Duplication : YES
Optimize Instantiated Primitives : NO
Use Clock Enable : Auto
Use Synchronous Set : Auto
Use Synchronous Reset : Auto
Pack IO Registers into IOBs : Auto
Equivalent register Removal : YES

---- General Options

Optimization Goal : Speed
Optimization Effort : 1
Power Reduction : NO
Keep Hierarchy : No
Netlist Hierarchy : As_Optimized
RTL Output : Yes
Global Optimization : AllClockNets
Read Cores : YES
Write Timing Constraints : NO
Cross Clock Analysis : NO
Hierarchy Separator : /
Bus Delimiter : <>
Case Specifier : Maintain
Slice Utilization Ratio : 100
BRAM Utilization Ratio : 100
DSP48 Utilization Ratio : 100
Auto BRAM Packing : NO
Slice Utilization Ratio Delta : 5

=====

=====

* HDL Parsing *

=====

Parsing VHDL file "64190088\unary_operators_vhdl_93.vhd" into library work
Parsing entity <reduction_operators>.
Parsing architecture <vhdl_93_process> of entity <reduction_operators>.

=====

* HDL Elaboration *

=====

Elaborating entity <reduction_operators> (architecture <vhdl_93_process>) with
generics from library <work>.

=====

* HDL Synthesis *

=====

Synthesizing Unit <reduction_operators>.

Related source file is "64190088\unary_operators_vhdl_93.vhd".

N = 64

Summary:

inferred 128 Multiplexer(s).

Unit <reduction_operators> synthesized.

=====

HDL Synthesis Report

Macro Statistics

Multiplexers : 128
1-bit 2-to-1 multiplexer : 128
Xors : 1
1-bit xor64 : 1

=====

* Advanced HDL Synthesis *

=====

Advanced HDL Synthesis Report

Macro Statistics

Multiplexers : 128
1-bit 2-to-1 multiplexer : 128
Xors : 1
1-bit xor64 : 1

=====

* Low Level Synthesis *

=====

Optimizing unit <reduction_operators> ...

Mapping all equations...

Building and optimizing final netlist ...

Found area constraint ratio of 100 (+ 5) on block reduction_operators, actual ratio is 1.

Final Macro Processing ...

=====

Final Register Report

Found no macro

=====

* Partition Report *

=====

Partition Implementation Status

No Partitions were found in this design.

=====

* Design Summary *

=====

Top Level Output File Name : reduction_operators.ngc

Primitive and Black Box Usage:

```
-----  
# BELS           : 59  
# GND            : 1  
# LUT4           : 3  
# LUT6           : 32  
# MUXCY          : 22  
# VCC            : 1  
# IO Buffers     : 67  
# IBUF           : 64  
# OBUF           : 3
```

Device utilization summary:

Selected Device : 6slx4tqg144-3

Slice Logic Utilization:

Number of Slice LUTs: 35 out of 2400 1%
Number used as Logic: 35 out of 2400 1%

Slice Logic Distribution:

Number of LUT Flip Flop pairs used: 35
Number with an unused Flip Flop: 35 out of 35 100%
Number with an unused LUT: 0 out of 35 0%
Number of fully used LUT-FF pairs: 0 out of 35 0%
Number of unique control sets: 0

IO Utilization:

Number of IOs: 67
Number of bonded IOBs: 67 out of 102 65%

Specific Feature Utilization:

----- Partition Resource Summary:

No Partitions were found in this design.

=====

Timing Report

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.

FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT
GENERATED AFTER PLACE-and-ROUTE.

Clock Information:

No clock signals found in this design

Asynchronous Control Signals Information:

No asynchronous control signals found in this design

Timing Summary:

Speed Grade: -3

Minimum period: No path found
Minimum input arrival time before clock: No path found
Maximum output required time after clock: No path found
Maximum combinational path delay: 7.522ns

Timing Details:

All values displayed in nanoseconds (ns)

=====
Timing constraint: Default path analysis
Total number of paths / destination ports: 192 / 3

Delay: 7.522ns (Levels of Logic = 5)
Source: A<22> (PAD)
Destination: reduced_XOR (PAD)

Data Path: A<22> to reduced_XOR

	Gate	Net				
Cell:	in->out	fanout	Delay	Delay	Logical Name	(Net Name)

IBUF:I->O	3	1.222	1.015	A_22_IBUF	(A_22_IBUF)
LUT6:I0->O	1	0.203	0.944	Mxor_reduced_XOR_xo<0>3	(Mxor_reduced_XOR_xo<0>2)
LUT6:I0->O	1	0.203	0.580	Mxor_reduced_XOR_xo<0>14_SW0	(N01)
LUT6:I5->O	1	0.205	0.579	Mxor_reduced_XOR_xo<0>14	(reduced_XOR_OBUF)
OBUF:I->O		2.571		reduced_XOR_OBUF	(reduced_XOR)

Total 7.522ns (4.404ns logic, 3.118ns route)
(58.5% logic, 41.5% route)

=====
Cross Clock Domains Report:

=====
Total REAL time to Xst completion: 9.00 secs
Total CPU time to Xst completion: 9.64 secs

-->

Total memory usage is 4487516 kilobytes

Number of errors : 0 (0 filtered)
Number of warnings : 0 (0 filtered)
Number of infos : 0 (0 filtered)

64190088>fuse -incremental -o unary_vhdl93_tb_isim_beh.exe -prj
unary_vhdl93_tb.prj -top reduction_operators_tb
Running: C:\Xilinx\14.7\ISE_DS\ISE\bin\nt64\unwrapped\fuse.exe -incremental -o
unary_vhdl93_tb_isim_beh.exe -prj unary_vhdl93_tb.prj -top reduction_operators_tb
ISim P.20131013 (signature 0x7708f090)
Number of CPUs detected in this system: 8
Turning on mult-threading, number of parallel sub-compilation jobs: 16
Determining compilation order of HDL files

```
Parsing VHDL file "unary_operators_vhdl_93.vhd" into library work
Parsing VHDL file "unary_operators_vhdl93_IDEAL_tb.vhd" into library work
Starting static elaboration
Completed static elaboration
Compiling package standard
Compiling package std_logic_1164
Compiling package numeric_std
Compiling package textio
Compiling package std_logic_textio
Compiling architecture vhdl_93_process of entity reduction_operators
[\\reduction_operators(3)\\]
Compiling architecture test of entity reduction_operators_tb
Time Resolution for simulation is 1ps.
Waiting for 1 sub-compilation(s) to finish...
Compiled 8 VHDL Units
Built simulation executable unary_vhdl93_tb_isim_beh.exe
Fuse Memory Usage: 36788 KB
Fuse CPU Usage: 859 ms
```

```
64190088>if exist reduction_operators.csv del reduction_operators.csv
```

```
64190088>if exist reduction_operators_64190088.csv del
reduction_operators_64190088.csv
```

```
64190088>unary_vhdl93_tb_isim_beh.exe -tclbatch isim.tcl -wdb
unary_vhdl93_tb_isim_beh.wdb
ISim P.20131013 (signature 0x7708f090)
WARNING: A WEBPACK license was found.
WARNING: Please use Xilinx License Configuration Manager to check out a full ISim
license.
WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for
more information on the differences between the Lite and the Full version.
This is a Lite version of ISim.
Time resolution is 1 ps
Simulator is doing circuit initialization process.
Finished circuit initialization process.
```

```
64190088>rem ren reduction_operators.csv reduction_operators_64190088.csv
```

```
-- *****
-- **** STUDENT: 64200100
-- *****
-- KOMENTARJI K OCENI NALOGE
-- Matej Možek: Ni pripomb
-- *****
```

```
64200100>if not exist "xst" mkdir xst
```

```
64200100>cd XST
```

```
64200100\xst>if not exist "projnav.tmp" mkdir "projnav.tmp"
```

```
64200100\xst>cd ..
```

```
64200100>xst -ifn unary_tree.xst
Release 14.7 - xst P.20131013 (nt64)
Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.
--> Parameter TMPDIR set to xst/projnav.tmp
```

```
Total REAL time to Xst completion: 0.00 secs
```

```
Total CPU time to Xst completion: 0.23 secs
```

```
--> Parameter xsthdpdir set to xst
```

```
Total REAL time to Xst completion: 0.00 secs
```

```
Total CPU time to Xst completion: 0.24 secs
```

```
-->
```

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 - 8.4.5) Cross Clock Domains Report

```
=====
*      Synthesis Options Summary      *
=====
```

---- Source Parameters

```
Input File Name      : "unary_tree.prj"
Ignore Synthesis Constraint File : NO
```

---- Target Parameters

```
Output File Name     : "Unary_Op_Bin_Tree"
```

Output Format : NGC
Target Device : xc6slx4-3-tqg144

----- Source Options

Top Module Name : Unary_Op_Bin_Tree
Automatic FSM Extraction : YES
FSM Encoding Algorithm : Auto
Safe Implementation : No
FSM Style : LUT
RAM Extraction : Yes
RAM Style : Auto
ROM Extraction : Yes
Shift Register Extraction : YES
ROM Style : Auto
Resource Sharing : YES
Asynchronous To Synchronous : NO
Shift Register Minimum Size : 2
Use DSP Block : Auto
Automatic Register Balancing : No

----- Target Options

LUT Combining : Auto
Reduce Control Sets : Auto
Add IO Buffers : YES
Global Maximum Fanout : 100000
Add Generic Clock Buffer(BUFG) : 16
Register Duplication : YES
Optimize Instantiated Primitives : NO
Use Clock Enable : Auto
Use Synchronous Set : Auto
Use Synchronous Reset : Auto
Pack IO Registers into IOBs : Auto
Equivalent register Removal : YES

----- General Options

Optimization Goal : Speed
Optimization Effort : 1
Power Reduction : NO
Keep Hierarchy : No
Netlist Hierarchy : As_Optimized
RTL Output : Yes
Global Optimization : AllClockNets
Read Cores : YES
Write Timing Constraints : NO
Cross Clock Analysis : NO
Hierarchy Separator : /
Bus Delimiter : <>
Case Specifier : Maintain
Slice Utilization Ratio : 100
BRAM Utilization Ratio : 100
DSP48 Utilization Ratio : 100
Auto BRAM Packing : NO
Slice Utilization Ratio Delta : 5

=====

=====

* HDL Parsing *

=====

Parsing VHDL file "64200100\unary_op_xor_tree_lut6.vhd" into library work
Parsing entity <XorTreeStage>.
Parsing architecture <tree_of_xor_lut6> of entity <xortreestage>.
Parsing VHDL file "64200100\unary_op_tree.vhd" into library work
Parsing entity <Unary_Op_Bin_Tree>.
Parsing architecture <t> of entity <unary_op_bin_tree>.

```
=====
*          HDL Elaboration          *
=====
```

Elaborating entity <Unary_Op_Bin_Tree> (architecture <t>) with generics from library <work>.

Elaborating entity <XorTreeStage> (architecture <tree_of_xor_lut6>) with generics from library <work>.

Elaborating entity <XorTreeStage> (architecture <tree_of_xor_lut6>) with generics from library <work>.

Elaborating entity <XorTreeStage> (architecture <tree_of_xor_lut6>) with generics from library <work>.

Elaborating entity <XorTreeStage> (architecture <tree_of_xor_lut6>) with generics from library <work>.

Elaborating entity <XorTreeStage> (architecture <tree_of_xor_lut6>) with generics from library <work>.

Elaborating entity <XorTreeStage> (architecture <tree_of_xor_lut6>) with generics from library <work>.

Elaborating entity <XorTreeStage> (architecture <tree_of_xor_lut6>) with generics from library <work>.

Elaborating entity <XorTreeStage> (architecture <tree_of_xor_lut6>) with generics from library <work>.

Elaborating entity <XorTreeStage> (architecture <tree_of_xor_lut6>) with generics from library <work>.

```
=====
*          HDL Synthesis            *
=====
```

Synthesizing Unit <Unary_Op_Bin_Tree>.
Related source file is "64200100\unary_op_tree.vhd".
N = 4096
Summary:
no macro.
Unit <Unary_Op_Bin_Tree> synthesized.

Synthesizing Unit <XorTreeStage_1>.
Related source file is "64200100\unary_op_xor_tree_lut6.vhd".
N = 4096
Summary:
no macro.
Unit <XorTreeStage_1> synthesized.

Synthesizing Unit <XorTreeStage_2>.
Related source file is "64200100\unary_op_xor_tree_lut6.vhd".
N = 683
Summary:
no macro.
Unit <XorTreeStage_2> synthesized.

Synthesizing Unit <XorTreeStage_3>.
Related source file is "64200100\unary_op_xor_tree_lut6.vhd".
N = 114
Summary:
no macro.
Unit <XorTreeStage_3> synthesized.

Synthesizing Unit <XorTreeStage_4>.
Related source file is "64200100\unary_op_xor_tree_lut6.vhd".
N = 19
Summary:
no macro.
Unit <XorTreeStage_4> synthesized.

Synthesizing Unit <XorTreeStage_5>.
Related source file is "64200100\unary_op_xor_tree_lut6.vhd".
N = 4
Summary:
no macro.
Unit <XorTreeStage_5> synthesized.

Synthesizing Unit <XorTreeStage_6>.
Related source file is "64200100\unary_op_xor_tree_lut6.vhd".
N = 3
Summary:
no macro.
Unit <XorTreeStage_6> synthesized.

Synthesizing Unit <XorTreeStage_7>.
Related source file is "64200100\unary_op_xor_tree_lut6.vhd".
N = 113
Summary:
no macro.
Unit <XorTreeStage_7> synthesized.

Synthesizing Unit <XorTreeStage_8>.
Related source file is "64200100\unary_op_xor_tree_lut6.vhd".
N = 18
Summary:
no macro.
Unit <XorTreeStage_8> synthesized.

Synthesizing Unit <XorTreeStage_9>.
Related source file is "64200100\unary_op_xor_tree_lut6.vhd".
N = 682
Summary:
no macro.
Unit <XorTreeStage_9> synthesized.

=====
HDL Synthesis Report

Found no macro

```
=====
*      Advanced HDL Synthesis      *
=====
```

```
=====
Advanced HDL Synthesis Report
=====
```

Found no macro

```
=====
*      Low Level Synthesis      *
=====
```

Optimizing unit <Unary_Op_Bin_Tree> ...

Mapping all equations...

Building and optimizing final netlist ...

Found area constraint ratio of 100 (+ 5) on block Unary_Op_Bin_Tree, actual ratio is 94.

Final Macro Processing ...

```
=====
Final Register Report
=====
```

Found no macro

```
=====
*      Partition Report      *
=====
```

Partition Implementation Status

No Partitions were found in this design.

```
=====
*      Design Summary      *
=====
```

Top Level Output File Name : Unary_Op_Bin_Tree.ngc

Primitive and Black Box Usage:

# BELS	: 1555
# LUT3	: 1088
# LUT4	: 208
# LUT6	: 259
# IO Buffers	: 4097
# IBUF	: 4096
# OBUF	: 1

Device utilization summary:

Selected Device : 6slx4tqg144-3

Slice Logic Utilization:

Number of Slice LUTs: 1555 out of 2400 64%
Number used as Logic: 1555 out of 2400 64%

Slice Logic Distribution:

Number of LUT Flip Flop pairs used: 1555
Number with an unused Flip Flop: 1555 out of 1555 100%
Number with an unused LUT: 0 out of 1555 0%
Number of fully used LUT-FF pairs: 0 out of 1555 0%
Number of unique control sets: 0

IO Utilization:

Number of IOs: 4097
Number of bonded IOBs: 4097 out of 102 4016% (*)

Specific Feature Utilization:

WARNING:Xst:1336 - (*) More than 100% of Device resources are used

Partition Resource Summary:

No Partitions were found in this design.

=====

Timing Report

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.
FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT
GENERATED AFTER PLACE-and-ROUTE.

Clock Information:

No clock signals found in this design

Asynchronous Control Signals Information:

No asynchronous control signals found in this design

Timing Summary:

Speed Grade: -3

Minimum period: No path found
Minimum input arrival time before clock: No path found
Maximum output required time after clock: No path found
Maximum combinational path delay: 10.106ns

Timing Details:

All values displayed in nanoseconds (ns)

```

=====
Timing constraint: Default path analysis
Total number of paths / destination ports: 4096 / 1
-----
Delay:      10.106ns (Levels of Logic = 7)
Source:     I<4092> (PAD)
Destination: O_Xor (PAD)

Data Path: I<4092> to O_Xor
Gate Net
Cell:in->out fanout Delay Delay Logical Name (Net Name)
-----
IBUF:I->O      1 1.222 0.827 I_4092_IBUF (I_4092_IBUF)
LUT4:I0->O     1 0.320 0.944
U_Xor/Stages.N1_Tree/Stages.N1_Tree/Stages.N1_Tree/Stage_xor_4.XOR_
LUT4 (U_Xor/Stages.N1_Tree/Stages.N1_Tree/Stages.N1_Tree/Stages.xor_1)
LUT6:I0->O     1 0.203 0.944
U_Xor/Stages.N1_Tree/Stages.N1_Tree/Stages.N1_Tree/Stages.XOR_LUT6
(U_Xor/Stages.N1_Tree/Stages.N1_Tree/Stages.xor_1)
LUT6:I0->O     1 0.203 0.944 U_Xor/Stages.N1_Tree/Stages.N1_Tree/Stages.XOR_LUT6
(U_Xor/Stages.N1_Tree/Stages.xor_1)
LUT6:I0->O     1 0.203 0.944 U_Xor/Stages.N1_Tree/Stages.XOR_LUT6
(U_Xor/Stages.xor_1)
LUT6:I0->O     1 0.203 0.579 U_Xor/Stages.XOR_LUT6 (O_Xor_OBUF)
OBUF:I->O      2.571 O_Xor_OBUF (O_Xor)
-----
Total      10.106ns (4.925ns logic, 5.181ns route)
          (48.7% logic, 51.3% route)
=====

```

Cross Clock Domains Report:

```

=====
Total REAL time to Xst completion: 16.00 secs
Total CPU time to Xst completion: 16.21 secs

```

-->

Total memory usage is 4538332 kilobytes

```

Number of errors : 0 ( 0 filtered)
Number of warnings : 1 ( 0 filtered)
Number of infos : 0 ( 0 filtered)

```

```

64200100>fuse -incremental -o unary_tree_tb_isim_beh.exe -prj unary_tree_tb.prj -
top Unary_Op_Bin_Tree_tb
Running: C:\Xilinx\14.7\ISE_DS\ISE\bin\nt64\unwrapped\fuse.exe -incremental -o
unary_tree_tb_isim_beh.exe -prj unary_tree_tb.prj -top Unary_Op_Bin_Tree_tb
ISim P.20131013 (signature 0x7708f090)
Number of CPUs detected in this system: 8
Turning on mult-threading, number of parallel sub-compilation jobs: 16
Determining compilation order of HDL files
Parsing VHDL file "slv_image_pkg.vhd" into library work
Parsing VHDL file "unary_op_xor_tree_lut6.vhd" into library work
Parsing VHDL file "unary_op_tree.vhd" into library work

```

```
Parsing VHDL file "unary_op_tree_IDEAL_tb.vhd" into library work
Starting static elaboration
Completed static elaboration
Compiling package standard
Compiling package std_logic_1164
Compiling package numeric_std
Compiling package textio
Compiling package std_logic_textio
Compiling package slv_image_pkg
Compiling package vcomponents
Compiling package vital_timing
Compiling package vital_primitives
Compiling package vpkg
Compiling architecture lut3_v of entity LUT3 [\LUT3("10010110")(0,7)\]
Compiling architecture tree_of_xor_lut6 of entity XorTreeStage [\XorTreeStage(3)\]
Compiling architecture tree_of_xor_lut6 of entity XorTreeStage [\XorTreeStage(2)\]
Compiling architecture lut6_v of entity LUT6 [\LUT6("0110100110010110100101100...")
Compiling architecture tree_of_xor_lut6 of entity XorTreeStage
[\XorTreeStage(16)\]
Compiling architecture t of entity Unary_Op_Bin_Tree [\Unary_Op_Bin_Tree(16)\]
Compiling architecture test of entity unary_op_bin_tree_tb
Time Resolution for simulation is 1ps.
Waiting for 1 sub-compilation(s) to finish...
Compiled 23 VHDL Units
Built simulation executable unary_tree_tb_isim_beh.exe
Fuse Memory Usage: 58952 KB
Fuse CPU Usage: 1280 ms
```

```
64200100>if exist Unary_Op_Bin_Tree.csv del Unary_Op_Bin_Tree.csv
```

```
64200100>if exist Unary_Op_Bin_Tree_64200100.csv del
Unary_Op_Bin_Tree_64200100.csv
```

```
64200100>unary_tree_tb_isim_beh.exe -tclbatch isim.tcl -wdb
unary_tree_tb_isim_beh.wdb
ISim P.20131013 (signature 0x7708f090)
WARNING: A WEBPACK license was found.
WARNING: Please use Xilinx License Configuration Manager to check out a full ISim
license.
WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for
more information on the differences between the Lite and the Full version.
This is a Lite version of ISim.
Time resolution is 1 ps
Simulator is doing circuit initialization process.
Finished circuit initialization process.
```

```
64200100>rem ren Unary_Op_Bin_Tree.csv Unary_Op_Bin_Tree_64200100.csv
```

```
64200100>xst -ifn unary_vhdl93.xst
Release 14.7 - xst P.20131013 (nt64)
Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.
--> Parameter TMPDIR set to xst/projnav.tmp
```

```
Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.23 secs
```

```
--> Parameter xsthdpdir set to xst
```

```
Total REAL time to Xst completion: 0.00 secs
```

Total CPU time to Xst completion: 0.23 secs

-->

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```
=====
*      Synthesis Options Summary      *
=====
```

---- Source Parameters

Input File Name : "./unary_vhd193.prj"
Ignore Synthesis Constraint File : NO

---- Target Parameters

Output File Name : "reduction_operators"
Output Format : NGC
Target Device : xc6slx4-3-tqg144

---- Source Options

Top Module Name : reduction_operators
Automatic FSM Extraction : YES
FSM Encoding Algorithm : Auto
Safe Implementation : No
FSM Style : LUT
RAM Extraction : Yes
RAM Style : Auto
ROM Extraction : Yes
Shift Register Extraction : YES
ROM Style : Auto
Resource Sharing : YES
Asynchronous To Synchronous : NO
Shift Register Minimum Size : 2
Use DSP Block : Auto
Automatic Register Balancing : No

---- Target Options

LUT Combining : Auto
Reduce Control Sets : Auto
Add IO Buffers : YES
Global Maximum Fanout : 100000
Add Generic Clock Buffer(BUFG) : 16

Register Duplication : YES
Optimize Instantiated Primitives : NO
Use Clock Enable : Auto
Use Synchronous Set : Auto
Use Synchronous Reset : Auto
Pack IO Registers into IOBs : Auto
Equivalent register Removal : YES

---- General Options

Optimization Goal : Speed
Optimization Effort : 1
Power Reduction : NO
Keep Hierarchy : No
Netlist Hierarchy : As_Optimized
RTL Output : Yes
Global Optimization : AllClockNets
Read Cores : YES
Write Timing Constraints : NO
Cross Clock Analysis : NO
Hierarchy Separator : /
Bus Delimiter : <>
Case Specifier : Maintain
Slice Utilization Ratio : 100
BRAM Utilization Ratio : 100
DSP48 Utilization Ratio : 100
Auto BRAM Packing : NO
Slice Utilization Ratio Delta : 5

=====

=====

* HDL Parsing *

=====

Parsing VHDL file "64200100\unary_operators_vhdl_93.vhd" into library work
Parsing entity <reduction_operators>.
Parsing architecture <vhdl_93_process> of entity <reduction_operators>.

=====

* HDL Elaboration *

=====

Elaborating entity <reduction_operators> (architecture <vhdl_93_process>) with
generics from library <work>.

=====

* HDL Synthesis *

=====

Synthesizing Unit <reduction_operators>.

Related source file is "64200100\unary_operators_vhdl_93.vhd".

N = 64

Summary:

inferred 128 Multiplexer(s).

Unit <reduction_operators> synthesized.

=====

HDL Synthesis Report

Macro Statistics

```
# Multiplexers          : 128
 1-bit 2-to-1 multiplexer : 128
# Xors                  : 1
 1-bit xor64            : 1
```

=====

=====

```
*      Advanced HDL Synthesis      *
```

=====

=====

Advanced HDL Synthesis Report

Macro Statistics

```
# Multiplexers          : 128
 1-bit 2-to-1 multiplexer : 128
# Xors                  : 1
 1-bit xor64            : 1
```

=====

=====

```
*      Low Level Synthesis      *
```

=====

Optimizing unit <reduction_operators> ...

Mapping all equations...

Building and optimizing final netlist ...

Found area constraint ratio of 100 (+ 5) on block reduction_operators, actual ratio is 1.

Final Macro Processing ...

=====

Final Register Report

Found no macro

=====

=====

```
*      Partition Report      *
```

=====

Partition Implementation Status

No Partitions were found in this design.

=====

```
*      Design Summary      *
```

=====

Top Level Output File Name : reduction_operators.ngc

Primitive and Black Box Usage:

```
-----
# BELS      : 59
# GND       : 1
# LUT4      : 3
# LUT6      : 32
# MUXCY     : 22
# VCC       : 1
# IO Buffers : 67
# IBUF      : 64
# OBUF      : 3
```

Device utilization summary:

Selected Device : 6slx4tqg144-3

Slice Logic Utilization:

Number of Slice LUTs: 35 out of 2400 1%
Number used as Logic: 35 out of 2400 1%

Slice Logic Distribution:

Number of LUT Flip Flop pairs used: 35
Number with an unused Flip Flop: 35 out of 35 100%
Number with an unused LUT: 0 out of 35 0%
Number of fully used LUT-FF pairs: 0 out of 35 0%
Number of unique control sets: 0

IO Utilization:

Number of IOs: 67
Number of bonded IOBs: 67 out of 102 65%

Specific Feature Utilization:

Partition Resource Summary:

No Partitions were found in this design.

=====

Timing Report

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.
FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT
GENERATED AFTER PLACE-and-ROUTE.

Clock Information:

No clock signals found in this design

Asynchronous Control Signals Information:

No asynchronous control signals found in this design

Timing Summary:

Speed Grade: -3

Minimum period: No path found
Minimum input arrival time before clock: No path found
Maximum output required time after clock: No path found
Maximum combinational path delay: 7.522ns

Timing Details:

All values displayed in nanoseconds (ns)

=====

Timing constraint: Default path analysis
Total number of paths / destination ports: 192 / 3

Delay: 7.522ns (Levels of Logic = 5)
Source: A<22> (PAD)
Destination: reduced_XOR (PAD)

Data Path: A<22> to reduced_XOR
Gate Net

Cell:in->out fanout Delay Delay Logical Name (Net Name)

IBUF:I->O 3 1.222 1.015 A_22_IBUF (A_22_IBUF)
LUT6:I0->O 1 0.203 0.944 Mxor_reduced_XOR_xo<0>3 (Mxor_reduced_XOR_xo<0>2)
LUT6:I0->O 1 0.203 0.580 Mxor_reduced_XOR_xo<0>14_SW0 (N01)
LUT6:I5->O 1 0.205 0.579 Mxor_reduced_XOR_xo<0>14 (reduced_XOR_OBUF)
OBUF:I->O 2.571 reduced_XOR_OBUF (reduced_XOR)

Total 7.522ns (4.404ns logic, 3.118ns route)
(58.5% logic, 41.5% route)

Cross Clock Domains Report:

=====

Total REAL time to Xst completion: 9.00 secs
Total CPU time to Xst completion: 9.37 secs

-->

Total memory usage is 4487516 kilobytes

Number of errors : 0 (0 filtered)
Number of warnings : 0 (0 filtered)
Number of infos : 0 (0 filtered)

64200100>fuse -incremental -o unary_vhdl93_tb_isim_beh.exe -prj
unary_vhdl93_tb.prj -top reduction_operators_tb
Running: C:\Xilinx\14.7\ISE_DS\ISE\bin\nt64\unwrapped\fuse.exe -incremental -o
unary_vhdl93_tb_isim_beh.exe -prj unary_vhdl93_tb.prj -top reduction_operators_tb
ISim P.20131013 (signature 0x7708f090)
Number of CPUs detected in this system: 8
Turning on mult-threading, number of parallel sub-compilation jobs: 16
Determining compilation order of HDL files
Parsing VHDL file "unary_operators_vhdl_93.vhd" into library work
Parsing VHDL file "unary_operators_vhdl93_IDEAL_tb.vhd" into library work


```
Starting static elaboration
Completed static elaboration
Compiling package standard
Compiling package std_logic_1164
Compiling package numeric_std
Compiling package textio
Compiling package std_logic_textio
Compiling architecture vhd1_93_process of entity reduction_operators
[\\reduction_operators(3)\\]
Compiling architecture test of entity reduction_operators_tb
Time Resolution for simulation is 1ps.
Compiled 8 VHDL Units
Built simulation executable unary_vhdl93_tb_isim_beh.exe
Fuse Memory Usage: 36888 KB
Fuse CPU Usage: 843 ms
```

```
64200100>if exist reduction_operators.csv del reduction_operators.csv
```

```
64200100>if exist reduction_operators_64200100.csv del
reduction_operators_64200100.csv
```

```
64200100>unary_vhdl93_tb_isim_beh.exe -tclbatch isim.tcl -wdb
unary_vhdl93_tb_isim_beh.wdb
ISim P.20131013 (signature 0x7708f090)
WARNING: A WEBPACK license was found.
WARNING: Please use Xilinx License Configuration Manager to check out a full ISim
license.
WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for
more information on the differences between the Lite and the Full version.
This is a Lite version of ISim.
Time resolution is 1 ps
Simulator is doing circuit initialization process.
Finished circuit initialization process.
```

```
64200100>ren ren reduction_operators.csv reduction_operators_64200100.csv
```

```
-- *****
-- **** STUDENT: 64200112
-- *****
-- KOMENTARJI K OCENI NALOGE
-- Matej Možek: Ni pripomb
-- *****
```

```
64200112>if not exist "xst" mkdir xst
```

```
64200112>cd XST
```

```
64200112\xst>if not exist "projnav.tmp" mkdir "projnav.tmp"
```

```
64200112\xst>cd ..
```

```
64200112>xst -ifn unary_tree.xst
Release 14.7 - xst P.20131013 (nt64)
Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.
--> Parameter TMPDIR set to xst/projnav.tmp
```

```
Total REAL time to Xst completion: 0.00 secs
```

```
Total CPU time to Xst completion: 0.29 secs
```

```
--> Parameter xsthdpdir set to xst
```

```
Total REAL time to Xst completion: 0.00 secs
```

```
Total CPU time to Xst completion: 0.33 secs
```

```
-->
```

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 - 8.4.5) Cross Clock Domains Report

```
=====
*      Synthesis Options Summary      *
```

----- Source Parameters

```
Input File Name      : "unary_tree.prj"
Ignore Synthesis Constraint File : NO
```

----- Target Parameters

```
Output File Name     : "Unary_Op_Bin_Tree"
```

Output Format : NGC
Target Device : xc6slx4-3-tqg144

----- Source Options

Top Module Name : Unary_Op_Bin_Tree
Automatic FSM Extraction : YES
FSM Encoding Algorithm : Auto
Safe Implementation : No
FSM Style : LUT
RAM Extraction : Yes
RAM Style : Auto
ROM Extraction : Yes
Shift Register Extraction : YES
ROM Style : Auto
Resource Sharing : YES
Asynchronous To Synchronous : NO
Shift Register Minimum Size : 2
Use DSP Block : Auto
Automatic Register Balancing : No

----- Target Options

LUT Combining : Auto
Reduce Control Sets : Auto
Add IO Buffers : YES
Global Maximum Fanout : 100000
Add Generic Clock Buffer(BUFG) : 16
Register Duplication : YES
Optimize Instantiated Primitives : NO
Use Clock Enable : Auto
Use Synchronous Set : Auto
Use Synchronous Reset : Auto
Pack IO Registers into IOBs : Auto
Equivalent register Removal : YES

----- General Options

Optimization Goal : Speed
Optimization Effort : 1
Power Reduction : NO
Keep Hierarchy : No
Netlist Hierarchy : As_Optimized
RTL Output : Yes
Global Optimization : AllClockNets
Read Cores : YES
Write Timing Constraints : NO
Cross Clock Analysis : NO
Hierarchy Separator : /
Bus Delimiter : <>
Case Specifier : Maintain
Slice Utilization Ratio : 100
BRAM Utilization Ratio : 100
DSP48 Utilization Ratio : 100
Auto BRAM Packing : NO
Slice Utilization Ratio Delta : 5

=====

=====

* HDL Parsing *

=====

Parsing VHDL file "64200112\unary_op_xor_tree_lut6.vhd" into library work
Parsing entity <XorTreeStage>.
Parsing architecture <tree_of_xor_lut6> of entity <xortreestage>.
Parsing VHDL file "64200112\unary_op_tree.vhd" into library work
Parsing entity <Unary_Op_Bin_Tree>.
Parsing architecture <t> of entity <unary_op_bin_tree>.

```
=====
*          HDL Elaboration          *
=====
```

Elaborating entity <Unary_Op_Bin_Tree> (architecture <t>) with generics from library <work>.

Elaborating entity <XorTreeStage> (architecture <tree_of_xor_lut6>) with generics from library <work>.

Elaborating entity <XorTreeStage> (architecture <tree_of_xor_lut6>) with generics from library <work>.

Elaborating entity <XorTreeStage> (architecture <tree_of_xor_lut6>) with generics from library <work>.

Elaborating entity <XorTreeStage> (architecture <tree_of_xor_lut6>) with generics from library <work>.

Elaborating entity <XorTreeStage> (architecture <tree_of_xor_lut6>) with generics from library <work>.

Elaborating entity <XorTreeStage> (architecture <tree_of_xor_lut6>) with generics from library <work>.

Elaborating entity <XorTreeStage> (architecture <tree_of_xor_lut6>) with generics from library <work>.

Elaborating entity <XorTreeStage> (architecture <tree_of_xor_lut6>) with generics from library <work>.

Elaborating entity <XorTreeStage> (architecture <tree_of_xor_lut6>) with generics from library <work>.

```
=====
*          HDL Synthesis            *
=====
```

Synthesizing Unit <Unary_Op_Bin_Tree>.
Related source file is "64200112\unary_op_tree.vhd".
N = 4096
Summary:
no macro.
Unit <Unary_Op_Bin_Tree> synthesized.

Synthesizing Unit <XorTreeStage_1>.
Related source file is "64200112\unary_op_xor_tree_lut6.vhd".
N = 4096
Summary:
no macro.
Unit <XorTreeStage_1> synthesized.

Synthesizing Unit <XorTreeStage_2>.
Related source file is "64200112\unary_op_xor_tree_lut6.vhd".
N = 683
Summary:
no macro.
Unit <XorTreeStage_2> synthesized.

Synthesizing Unit <XorTreeStage_3>.
Related source file is "64200112\unary_op_xor_tree_lut6.vhd".
N = 114
Summary:
no macro.
Unit <XorTreeStage_3> synthesized.

Synthesizing Unit <XorTreeStage_4>.
Related source file is "64200112\unary_op_xor_tree_lut6.vhd".
N = 19
Summary:
no macro.
Unit <XorTreeStage_4> synthesized.

Synthesizing Unit <XorTreeStage_5>.
Related source file is "64200112\unary_op_xor_tree_lut6.vhd".
N = 4
Summary:
no macro.
Unit <XorTreeStage_5> synthesized.

Synthesizing Unit <XorTreeStage_6>.
Related source file is "64200112\unary_op_xor_tree_lut6.vhd".
N = 3
Summary:
no macro.
Unit <XorTreeStage_6> synthesized.

Synthesizing Unit <XorTreeStage_7>.
Related source file is "64200112\unary_op_xor_tree_lut6.vhd".
N = 113
Summary:
no macro.
Unit <XorTreeStage_7> synthesized.

Synthesizing Unit <XorTreeStage_8>.
Related source file is "64200112\unary_op_xor_tree_lut6.vhd".
N = 18
Summary:
no macro.
Unit <XorTreeStage_8> synthesized.

Synthesizing Unit <XorTreeStage_9>.
Related source file is "64200112\unary_op_xor_tree_lut6.vhd".
N = 682
Summary:
no macro.
Unit <XorTreeStage_9> synthesized.

=====
HDL Synthesis Report

Found no macro

```
=====
*      Advanced HDL Synthesis      *
=====
```

```
=====
Advanced HDL Synthesis Report
=====
```

Found no macro

```
=====
*      Low Level Synthesis      *
=====
```

Optimizing unit <Unary_Op_Bin_Tree> ...

Mapping all equations...

Building and optimizing final netlist ...

Found area constraint ratio of 100 (+ 5) on block Unary_Op_Bin_Tree, actual ratio is 94.

Final Macro Processing ...

```
=====
Final Register Report
=====
```

Found no macro

```
=====
*      Partition Report      *
=====
```

Partition Implementation Status

No Partitions were found in this design.

```
=====
*      Design Summary      *
=====
```

Top Level Output File Name : Unary_Op_Bin_Tree.ngc

Primitive and Black Box Usage:

# BELS	: 1555
# LUT3	: 1088
# LUT4	: 208
# LUT6	: 259
# IO Buffers	: 4097
# IBUF	: 4096
# OBUF	: 1

Device utilization summary:

Selected Device : 6slx4tqg144-3

Slice Logic Utilization:

Number of Slice LUTs: 1555 out of 2400 64%
Number used as Logic: 1555 out of 2400 64%

Slice Logic Distribution:

Number of LUT Flip Flop pairs used: 1555
Number with an unused Flip Flop: 1555 out of 1555 100%
Number with an unused LUT: 0 out of 1555 0%
Number of fully used LUT-FF pairs: 0 out of 1555 0%
Number of unique control sets: 0

IO Utilization:

Number of IOs: 4097
Number of bonded IOBs: 4097 out of 102 4016% (*)

Specific Feature Utilization:

WARNING:Xst:1336 - (*) More than 100% of Device resources are used

Partition Resource Summary:

No Partitions were found in this design.

=====

Timing Report

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.
FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT
GENERATED AFTER PLACE-and-ROUTE.

Clock Information:

No clock signals found in this design

Asynchronous Control Signals Information:

No asynchronous control signals found in this design

Timing Summary:

Speed Grade: -3

Minimum period: No path found
Minimum input arrival time before clock: No path found
Maximum output required time after clock: No path found
Maximum combinational path delay: 10.106ns

Timing Details:

All values displayed in nanoseconds (ns)

```

=====
Timing constraint: Default path analysis
Total number of paths / destination ports: 4096 / 1
-----
Delay:      10.106ns (Levels of Logic = 7)
Source:     I<4092> (PAD)
Destination: O_Xor (PAD)

Data Path: I<4092> to O_Xor
Gate Net
Cell:in->out fanout Delay Delay Logical Name (Net Name)
-----
IBUF:I->O      1 1.222 0.827 I_4092_IBUF (I_4092_IBUF)
LUT4:I0->O     1 0.320 0.944
U_Xor/Stages.Stage1/Stages.Stage1/Stages.Stage1/Stages.Stage1/Stage_xor_4.XOR_LUT4
(U_Xor/Stages.Stage1/Stages.Stage1/Stages.Stage1/Stages.testVar1)
LUT6:I0->O     1 0.203 0.944
U_Xor/Stages.Stage1/Stages.Stage1/Stages.Stage1/Stages.XOR6_LUT6
(U_Xor/Stages.Stage1/Stages.Stage1/Stages.testVar1)
LUT6:I0->O     1 0.203 0.944 U_Xor/Stages.Stage1/Stages.Stage1/Stages.XOR6_LUT6
(U_Xor/Stages.Stage1/Stages.testVar1)
LUT6:I0->O     1 0.203 0.944 U_Xor/Stages.Stage1/Stages.XOR6_LUT6
(U_Xor/Stages.testVar1)
LUT6:I0->O     1 0.203 0.579 U_Xor/Stages.XOR6_LUT6 (O_Xor_OBUF)
OBUF:I->O      2.571 O_Xor_OBUF (O_Xor)
-----
Total      10.106ns (4.925ns logic, 5.181ns route)
          (48.7% logic, 51.3% route)
=====

```

Cross Clock Domains Report:

```

=====
Total REAL time to Xst completion: 16.00 secs
Total CPU time to Xst completion: 16.41 secs

```

-->

Total memory usage is 4538360 kilobytes

```

Number of errors : 0 ( 0 filtered)
Number of warnings : 1 ( 0 filtered)
Number of infos : 0 ( 0 filtered)

```

```

64200112>fuse -incremental -o unary_tree_tb_isim_beh.exe -prj unary_tree_tb.prj -
top Unary_Op_Bin_Tree_tb
Running: C:\Xilinx\14.7\ISE_DS\ISE\bin\nt64\unwrapped\fuse.exe -incremental -o
unary_tree_tb_isim_beh.exe -prj unary_tree_tb.prj -top Unary_Op_Bin_Tree_tb
ISim P.20131013 (signature 0x7708f090)
Number of CPUs detected in this system: 8
Turning on mult-threading, number of parallel sub-compilation jobs: 16
Determining compilation order of HDL files
Parsing VHDL file "slv_image_pkg.vhd" into library work
Parsing VHDL file "unary_op_xor_tree_lut6.vhd" into library work
Parsing VHDL file "unary_op_tree.vhd" into library work

```



```
Parsing VHDL file "unary_op_tree_IDEAL_tb.vhd" into library work
Starting static elaboration
Completed static elaboration
Compiling package standard
Compiling package std_logic_1164
Compiling package numeric_std
Compiling package textio
Compiling package std_logic_textio
Compiling package slv_image_pkg
Compiling package vcomponents
Compiling package vital_timing
Compiling package vital_primitives
Compiling package vpkg
Compiling architecture lut3_v of entity LUT3 [\LUT3("10010110")(0,7)\]
Compiling architecture tree_of_xor_lut6 of entity XorTreeStage [\XorTreeStage(3)\]
Compiling architecture tree_of_xor_lut6 of entity XorTreeStage [\XorTreeStage(2)\]
Compiling architecture lut6_v of entity LUT6 [\LUT6("0110100110010110100101100...")
Compiling architecture tree_of_xor_lut6 of entity XorTreeStage
[\XorTreeStage(16)\]
Compiling architecture t of entity Unary_Op_Bin_Tree [\Unary_Op_Bin_Tree(16)\]
Compiling architecture test of entity unary_op_bin_tree_tb
Time Resolution for simulation is 1ps.
Waiting for 1 sub-compilation(s) to finish...
Compiled 23 VHDL Units
Built simulation executable unary_tree_tb_isim_beh.exe
Fuse Memory Usage: 59068 KB
Fuse CPU Usage: 1311 ms
```

```
64200112>if exist Unary_Op_Bin_Tree.csv del Unary_Op_Bin_Tree.csv
```

```
64200112>if exist Unary_Op_Bin_Tree_64200112.csv del
Unary_Op_Bin_Tree_64200112.csv
```

```
64200112>unary_tree_tb_isim_beh.exe -tclbatch isim.tcl -wdb
unary_tree_tb_isim_beh.wdb
ISim P.20131013 (signature 0x7708f090)
WARNING: A WEBPACK license was found.
WARNING: Please use Xilinx License Configuration Manager to check out a full ISim
license.
WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for
more information on the differences between the Lite and the Full version.
This is a Lite version of ISim.
Time resolution is 1 ps
Simulator is doing circuit initialization process.
Finished circuit initialization process.
```

```
64200112>rem ren Unary_Op_Bin_Tree.csv Unary_Op_Bin_Tree_64200112.csv
```

```
64200112>xst -ifn unary_vhdl93.xst
Release 14.7 - xst P.20131013 (nt64)
Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.
--> Parameter TMPDIR set to xst/projnav.tmp
```

```
Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.22 secs
```

```
--> Parameter xsthdpdir set to xst
```

```
Total REAL time to Xst completion: 0.00 secs
```

Total CPU time to Xst completion: 0.23 secs

-->

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 - 8.4.5) Cross Clock Domains Report

```
=====
*      Synthesis Options Summary      *
=====
```

---- Source Parameters

Input File Name : "./unary_vhd193.prj"
Ignore Synthesis Constraint File : NO

---- Target Parameters

Output File Name : "reduction_operators"
Output Format : NGC
Target Device : xc6slx4-3-tqg144

---- Source Options

Top Module Name : reduction_operators
Automatic FSM Extraction : YES
FSM Encoding Algorithm : Auto
Safe Implementation : No
FSM Style : LUT
RAM Extraction : Yes
RAM Style : Auto
ROM Extraction : Yes
Shift Register Extraction : YES
ROM Style : Auto
Resource Sharing : YES
Asynchronous To Synchronous : NO
Shift Register Minimum Size : 2
Use DSP Block : Auto
Automatic Register Balancing : No

---- Target Options

LUT Combining : Auto
Reduce Control Sets : Auto
Add IO Buffers : YES
Global Maximum Fanout : 100000
Add Generic Clock Buffer(BUFG) : 16

Register Duplication : YES
Optimize Instantiated Primitives : NO
Use Clock Enable : Auto
Use Synchronous Set : Auto
Use Synchronous Reset : Auto
Pack IO Registers into IOBs : Auto
Equivalent register Removal : YES

---- General Options

Optimization Goal : Speed
Optimization Effort : 1
Power Reduction : NO
Keep Hierarchy : No
Netlist Hierarchy : As_Optimized
RTL Output : Yes
Global Optimization : AllClockNets
Read Cores : YES
Write Timing Constraints : NO
Cross Clock Analysis : NO
Hierarchy Separator : /
Bus Delimiter : <>
Case Specifier : Maintain
Slice Utilization Ratio : 100
BRAM Utilization Ratio : 100
DSP48 Utilization Ratio : 100
Auto BRAM Packing : NO
Slice Utilization Ratio Delta : 5

=====

=====

* HDL Parsing *

=====

Parsing VHDL file "64200112\unary_operators_vhdl_93.vhd" into library work
Parsing entity <reduction_operators>.
Parsing architecture <vhdl_93_process> of entity <reduction_operators>.

=====

* HDL Elaboration *

=====

Elaborating entity <reduction_operators> (architecture <vhdl_93_process>) with
generics from library <work>.

=====

* HDL Synthesis *

=====

Synthesizing Unit <reduction_operators>.
Related source file is "64200112\unary_operators_vhdl_93.vhd".
N = 64
Summary:
inferred 128 Multiplexer(s).
Unit <reduction_operators> synthesized.

=====

HDL Synthesis Report

Macro Statistics

```
# Multiplexers          : 128
 1-bit 2-to-1 multiplexer : 128
# Xors                  : 1
 1-bit xor64           : 1
```

=====

=====

```
*      Advanced HDL Synthesis      *
```

=====

=====

Advanced HDL Synthesis Report

Macro Statistics

```
# Multiplexers          : 128
 1-bit 2-to-1 multiplexer : 128
# Xors                  : 1
 1-bit xor64           : 1
```

=====

=====

```
*      Low Level Synthesis      *
```

=====

Optimizing unit <reduction_operators> ...

Mapping all equations...

Building and optimizing final netlist ...

Found area constraint ratio of 100 (+ 5) on block reduction_operators, actual ratio is 1.

Final Macro Processing ...

=====

Final Register Report

Found no macro

=====

=====

```
*      Partition Report      *
```

=====

Partition Implementation Status

No Partitions were found in this design.

=====

```
*      Design Summary      *
```

=====

Top Level Output File Name : reduction_operators.ngc

Primitive and Black Box Usage:

```
-----
# BELS      : 59
# GND       : 1
# LUT4      : 3
# LUT6      : 32
# MUXCY     : 22
# VCC       : 1
# IO Buffers : 67
# IBUF      : 64
# OBUF      : 3
```

Device utilization summary:

Selected Device : 6slx4tqg144-3

Slice Logic Utilization:

Number of Slice LUTs: 35 out of 2400 1%
Number used as Logic: 35 out of 2400 1%

Slice Logic Distribution:

Number of LUT Flip Flop pairs used: 35
Number with an unused Flip Flop: 35 out of 35 100%
Number with an unused LUT: 0 out of 35 0%
Number of fully used LUT-FF pairs: 0 out of 35 0%
Number of unique control sets: 0

IO Utilization:

Number of IOs: 67
Number of bonded IOBs: 67 out of 102 65%

Specific Feature Utilization:

Partition Resource Summary:

No Partitions were found in this design.

=====

Timing Report

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.
FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT
GENERATED AFTER PLACE-and-ROUTE.

Clock Information:

No clock signals found in this design

Asynchronous Control Signals Information:

No asynchronous control signals found in this design

Timing Summary:

Speed Grade: -3

Minimum period: No path found
Minimum input arrival time before clock: No path found
Maximum output required time after clock: No path found
Maximum combinational path delay: 7.522ns

Timing Details:

All values displayed in nanoseconds (ns)

=====

Timing constraint: Default path analysis

Total number of paths / destination ports: 192 / 3

Delay: 7.522ns (Levels of Logic = 5)

Source: A<22> (PAD)

Destination: reduced_XOR (PAD)

Data Path: A<22> to reduced_XOR

Gate Net

Cell:in->out fanout Delay Delay Logical Name (Net Name)

IBUF:I->O 3 1.222 1.015 A_22_IBUF (A_22_IBUF)

LUT6:I0->O 1 0.203 0.944 Mxor_reduced_XOR_xo<0>3 (Mxor_reduced_XOR_xo<0>2)

LUT6:I0->O 1 0.203 0.580 Mxor_reduced_XOR_xo<0>14_SW0 (N01)

LUT6:I5->O 1 0.205 0.579 Mxor_reduced_XOR_xo<0>14 (reduced_XOR_OBUF)

OBUF:I->O 2.571 reduced_XOR_OBUF (reduced_XOR)

Total 7.522ns (4.404ns logic, 3.118ns route)

(58.5% logic, 41.5% route)

=====

Cross Clock Domains Report:

=====

Total REAL time to Xst completion: 9.00 secs

Total CPU time to Xst completion: 9.15 secs

-->

Total memory usage is 4487516 kilobytes

Number of errors : 0 (0 filtered)

Number of warnings : 0 (0 filtered)

Number of infos : 0 (0 filtered)

64200112>fuse -incremental -o unary_vhdl93_tb_isim_beh.exe -prj

unary_vhdl93_tb.prj -top reduction_operators_tb

Running: C:\Xilinx\14.7\ISE_DS\ISE\bin\nt64\unwrapped\fuse.exe -incremental -o

unary_vhdl93_tb_isim_beh.exe -prj unary_vhdl93_tb.prj -top reduction_operators_tb

ISim P.20131013 (signature 0x7708f090)

Number of CPUs detected in this system: 8

Turning on mult-threading, number of parallel sub-compilation jobs: 16

Determining compilation order of HDL files

Parsing VHDL file "unary_operators_vhdl_93.vhd" into library work

Parsing VHDL file "unary_operators_vhdl93_IDEAL_tb.vhd" into library work

Starting static elaboration
Completed static elaboration
Compiling package standard
Compiling package std_logic_1164
Compiling package numeric_std
Compiling package textio
Compiling package std_logic_textio
Compiling architecture vhd1_93_process of entity reduction_operators
[\\reduction_operators(3)\\]
Compiling architecture test of entity reduction_operators_tb
Time Resolution for simulation is 1ps.
Waiting for 1 sub-compilation(s) to finish...
Compiled 8 VHDL Units
Built simulation executable unary_vhdl93_tb_isim_beh.exe
Fuse Memory Usage: 36788 KB
Fuse CPU Usage: 890 ms

64200112>if exist reduction_operators.csv del reduction_operators.csv

64200112>if exist reduction_operators_64200112.csv del
reduction_operators_64200112.csv

64200112>unary_vhdl93_tb_isim_beh.exe -tclbatch isim.tcl -wdb
unary_vhdl93_tb_isim_beh.wdb
ISim P.20131013 (signature 0x7708f090)
WARNING: A WEBPACK license was found.
WARNING: Please use Xilinx License Configuration Manager to check out a full ISim
license.
WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for
more information on the differences between the Lite and the Full version.
This is a Lite version of ISim.
Time resolution is 1 ps
Simulator is doing circuit initialization process.
Finished circuit initialization process.

64200112>rem ren reduction_operators.csv reduction_operators_64200112.csv

```
-- *****
-- **** STUDENT: 64200163
-- *****
-- KOMENTARJI K OCENI NALOGE
-- Matej Možek: Ni pripomb
-- *****
```

```
64200163>if not exist "xst" mkdir xst
```

```
64200163>cd XST
```

```
64200163\xst>if not exist "projnav.tmp" mkdir "projnav.tmp"
```

```
64200163\xst>cd ..
```

```
64200163>xst -ifn unary_tree.xst
Release 14.7 - xst P.20131013 (nt64)
Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.
--> Parameter TMPDIR set to xst/projnav.tmp
```

```
Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.23 secs
```

```
--> Parameter xsthdpdir set to xst
```

```
Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.24 secs
```

```
-->
```

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 - 8.4.3) Timing Summary
 - 8.4.4) Timing Details
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```
=====
*      Synthesis Options Summary      *
=====
```

---- Source Parameters

```
Input File Name      : "unary_tree.prj"
Ignore Synthesis Constraint File : NO
```

---- Target Parameters

```
Output File Name     : "Unary_Op_Bin_Tree"
```


Output Format : NGC
Target Device : xc6slx4-3-tqg144

----- Source Options

Top Module Name : Unary_Op_Bin_Tree
Automatic FSM Extraction : YES
FSM Encoding Algorithm : Auto
Safe Implementation : No
FSM Style : LUT
RAM Extraction : Yes
RAM Style : Auto
ROM Extraction : Yes
Shift Register Extraction : YES
ROM Style : Auto
Resource Sharing : YES
Asynchronous To Synchronous : NO
Shift Register Minimum Size : 2
Use DSP Block : Auto
Automatic Register Balancing : No

----- Target Options

LUT Combining : Auto
Reduce Control Sets : Auto
Add IO Buffers : YES
Global Maximum Fanout : 100000
Add Generic Clock Buffer(BUFG) : 16
Register Duplication : YES
Optimize Instantiated Primitives : NO
Use Clock Enable : Auto
Use Synchronous Set : Auto
Use Synchronous Reset : Auto
Pack IO Registers into IOBs : Auto
Equivalent register Removal : YES

----- General Options

Optimization Goal : Speed
Optimization Effort : 1
Power Reduction : NO
Keep Hierarchy : No
Netlist Hierarchy : As_Optimized
RTL Output : Yes
Global Optimization : AllClockNets
Read Cores : YES
Write Timing Constraints : NO
Cross Clock Analysis : NO
Hierarchy Separator : /
Bus Delimiter : <>
Case Specifier : Maintain
Slice Utilization Ratio : 100
BRAM Utilization Ratio : 100
DSP48 Utilization Ratio : 100
Auto BRAM Packing : NO
Slice Utilization Ratio Delta : 5

=====

=====

* HDL Parsing *

=====

Parsing VHDL file "64200163\unary_op_xor_tree_lut6.vhd" into library work
Parsing entity <XorTreeStage>.
Parsing architecture <tree_of_xor_lut6> of entity <xortreestage>.
Parsing VHDL file "64200163\unary_op_tree.vhd" into library work
Parsing entity <Unary_Op_Bin_Tree>.
Parsing architecture <t> of entity <unary_op_bin_tree>.

```
=====
*          HDL Elaboration          *
=====
```

Elaborating entity <Unary_Op_Bin_Tree> (architecture <t>) with generics from library <work>.

Elaborating entity <XorTreeStage> (architecture <tree_of_xor_lut6>) with generics from library <work>.

Elaborating entity <XorTreeStage> (architecture <tree_of_xor_lut6>) with generics from library <work>.

Elaborating entity <XorTreeStage> (architecture <tree_of_xor_lut6>) with generics from library <work>.

Elaborating entity <XorTreeStage> (architecture <tree_of_xor_lut6>) with generics from library <work>.

Elaborating entity <XorTreeStage> (architecture <tree_of_xor_lut6>) with generics from library <work>.

Elaborating entity <XorTreeStage> (architecture <tree_of_xor_lut6>) with generics from library <work>.

Elaborating entity <XorTreeStage> (architecture <tree_of_xor_lut6>) with generics from library <work>.

Elaborating entity <XorTreeStage> (architecture <tree_of_xor_lut6>) with generics from library <work>.

Elaborating entity <XorTreeStage> (architecture <tree_of_xor_lut6>) with generics from library <work>.

```
=====
*          HDL Synthesis            *
=====
```

Synthesizing Unit <Unary_Op_Bin_Tree>.
Related source file is "64200163\unary_op_tree.vhd".
N = 4096
Summary:
no macro.
Unit <Unary_Op_Bin_Tree> synthesized.

Synthesizing Unit <XorTreeStage_1>.
Related source file is "64200163\unary_op_xor_tree_lut6.vhd".
N = 4096
Summary:
no macro.
Unit <XorTreeStage_1> synthesized.

Synthesizing Unit <XorTreeStage_2>.
Related source file is "64200163\unary_op_xor_tree_lut6.vhd".
N = 683
Summary:
no macro.
Unit <XorTreeStage_2> synthesized.

Synthesizing Unit <XorTreeStage_3>.
Related source file is "64200163\unary_op_xor_tree_lut6.vhd".
N = 114
Summary:
no macro.
Unit <XorTreeStage_3> synthesized.

Synthesizing Unit <XorTreeStage_4>.
Related source file is "64200163\unary_op_xor_tree_lut6.vhd".
N = 19
Summary:
no macro.
Unit <XorTreeStage_4> synthesized.

Synthesizing Unit <XorTreeStage_5>.
Related source file is "64200163\unary_op_xor_tree_lut6.vhd".
N = 4
Summary:
no macro.
Unit <XorTreeStage_5> synthesized.

Synthesizing Unit <XorTreeStage_6>.
Related source file is "64200163\unary_op_xor_tree_lut6.vhd".
N = 3
Summary:
no macro.
Unit <XorTreeStage_6> synthesized.

Synthesizing Unit <XorTreeStage_7>.
Related source file is "64200163\unary_op_xor_tree_lut6.vhd".
N = 113
Summary:
no macro.
Unit <XorTreeStage_7> synthesized.

Synthesizing Unit <XorTreeStage_8>.
Related source file is "64200163\unary_op_xor_tree_lut6.vhd".
N = 18
Summary:
no macro.
Unit <XorTreeStage_8> synthesized.

Synthesizing Unit <XorTreeStage_9>.
Related source file is "64200163\unary_op_xor_tree_lut6.vhd".
N = 682
Summary:
no macro.
Unit <XorTreeStage_9> synthesized.

=====
HDL Synthesis Report

Found no macro

```
=====
*      Advanced HDL Synthesis      *
=====
```

```
=====
Advanced HDL Synthesis Report
=====
```

Found no macro

```
=====
*      Low Level Synthesis      *
=====
```

Optimizing unit <Unary_Op_Bin_Tree> ...

Mapping all equations...

Building and optimizing final netlist ...

Found area constraint ratio of 100 (+ 5) on block Unary_Op_Bin_Tree, actual ratio is 94.

Final Macro Processing ...

```
=====
Final Register Report
=====
```

Found no macro

```
=====
*      Partition Report      *
=====
```

Partition Implementation Status

No Partitions were found in this design.

```
=====
*      Design Summary      *
=====
```

Top Level Output File Name : Unary_Op_Bin_Tree.ngc

Primitive and Black Box Usage:

BELS : 1555
LUT3 : 1088
LUT4 : 208
LUT6 : 259
IO Buffers : 4097
IBUF : 4096
OBUF : 1

Device utilization summary:

Selected Device : 6slx4tqg144-3

Slice Logic Utilization:

Number of Slice LUTs: 1555 out of 2400 64%
Number used as Logic: 1555 out of 2400 64%

Slice Logic Distribution:

Number of LUT Flip Flop pairs used: 1555
Number with an unused Flip Flop: 1555 out of 1555 100%
Number with an unused LUT: 0 out of 1555 0%
Number of fully used LUT-FF pairs: 0 out of 1555 0%
Number of unique control sets: 0

IO Utilization:

Number of IOs: 4097
Number of bonded IOBs: 4097 out of 102 4016% (*)

Specific Feature Utilization:

WARNING:Xst:1336 - (*) More than 100% of Device resources are used

Partition Resource Summary:

No Partitions were found in this design.

=====

Timing Report

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.
FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT
GENERATED AFTER PLACE-and-ROUTE.

Clock Information:

No clock signals found in this design

Asynchronous Control Signals Information:

No asynchronous control signals found in this design

Timing Summary:

Speed Grade: -3

Minimum period: No path found
Minimum input arrival time before clock: No path found
Maximum output required time after clock: No path found
Maximum combinational path delay: 10.106ns

Timing Details:

All values displayed in nanoseconds (ns)

```

=====
Timing constraint: Default path analysis
Total number of paths / destination ports: 4096 / 1
-----
Delay:      10.106ns (Levels of Logic = 7)
Source:     I<4092> (PAD)
Destination: O_Xor (PAD)

Data Path: I<4092> to O_Xor
Gate Net
Cell:in->out fanout Delay Delay Logical Name (Net Name)
-----
IBUF:I->O      1 1.222 0.827 I_4092_IBUF (I_4092_IBUF)
LUT4:I0->O     1 0.320 0.944
U_Xor/Stages.Tree_1_6/Stages.Tree_1_6/Stages.Tree_1_6/Stages.Tree_1_6/Stage_xor_4.
XOR4_LUT (U_Xor/Stages.Tree_1_6/Stages.Tree_1_6/Stages.Tree_1_6/Stages.Xor_1_6)
LUT6:I0->O     1 0.203 0.944
U_Xor/Stages.Tree_1_6/Stages.Tree_1_6/Stages.Tree_1_6/Stages.XOR6_LUT
(U_Xor/Stages.Tree_1_6/Stages.Tree_1_6/Stages.Xor_1_6)
LUT6:I0->O     1 0.203 0.944 U_Xor/Stages.Tree_1_6/Stages.Tree_1_6/Stages.XOR6_LUT
(U_Xor/Stages.Tree_1_6/Stages.Xor_1_6)
LUT6:I0->O     1 0.203 0.944 U_Xor/Stages.Tree_1_6/Stages.XOR6_LUT
(U_Xor/Stages.Xor_1_6)
LUT6:I0->O     1 0.203 0.579 U_Xor/Stages.XOR6_LUT (O_Xor_OBUF)
OBUF:I->O      2.571 O_Xor_OBUF (O_Xor)
-----
Total      10.106ns (4.925ns logic, 5.181ns route)
          (48.7% logic, 51.3% route)
=====

```

Cross Clock Domains Report:

```

=====
Total REAL time to Xst completion: 16.00 secs
Total CPU time to Xst completion: 15.31 secs

```

-->

Total memory usage is 4538384 kilobytes

```

Number of errors : 0 ( 0 filtered)
Number of warnings : 1 ( 0 filtered)
Number of infos : 0 ( 0 filtered)

```

```

64200163>fuse -incremental -o unary_tree_tb_isim_beh.exe -prj unary_tree_tb.prj -
top Unary_Op_Bin_Tree_tb
Running: C:\Xilinx\14.7\ISE_DS\ISE\bin\nt64\unwrapped\fuse.exe -incremental -o
unary_tree_tb_isim_beh.exe -prj unary_tree_tb.prj -top Unary_Op_Bin_Tree_tb
ISim P.20131013 (signature 0x7708f090)
Number of CPUs detected in this system: 8
Turning on mult-threading, number of parallel sub-compilation jobs: 16
Determining compilation order of HDL files
Parsing VHDL file "slv_image_pkg.vhd" into library work
Parsing VHDL file "unary_op_xor_tree_lut6.vhd" into library work
Parsing VHDL file "unary_op_tree.vhd" into library work

```

```
Parsing VHDL file "unary_op_tree_IDEAL_tb.vhd" into library work
Starting static elaboration
Completed static elaboration
Compiling package standard
Compiling package std_logic_1164
Compiling package numeric_std
Compiling package textio
Compiling package std_logic_textio
Compiling package slv_image_pkg
Compiling package vcomponents
Compiling package vital_timing
Compiling package vital_primitives
Compiling package vpkg
Compiling architecture lut3_v of entity LUT3 [\LUT3("10010110")(0,7)\]
Compiling architecture tree_of_xor_lut6 of entity XorTreeStage [\XorTreeStage(3)\]
Compiling architecture tree_of_xor_lut6 of entity XorTreeStage [\XorTreeStage(2)\]
Compiling architecture lut6_v of entity LUT6 [\LUT6("0110100110010110100101100...")\]
Compiling architecture tree_of_xor_lut6 of entity XorTreeStage
[\XorTreeStage(16)\]
Compiling architecture t of entity Unary_Op_Bin_Tree [\Unary_Op_Bin_Tree(16)\]
Compiling architecture test of entity unary_op_bin_tree_tb
Time Resolution for simulation is 1ps.
Waiting for 1 sub-compilation(s) to finish...
Compiled 23 VHDL Units
Built simulation executable unary_tree_tb_isim_beh.exe
Fuse Memory Usage: 60072 KB
Fuse CPU Usage: 1468 ms
```

```
64200163>if exist Unary_Op_Bin_Tree.csv del Unary_Op_Bin_Tree.csv
```

```
64200163>if exist Unary_Op_Bin_Tree_64200163.csv del
Unary_Op_Bin_Tree_64200163.csv
```

```
64200163>unary_tree_tb_isim_beh.exe -tclbatch isim.tcl -wdb
unary_tree_tb_isim_beh.wdb
ISim P.20131013 (signature 0x7708f090)
WARNING: A WEBPACK license was found.
WARNING: Please use Xilinx License Configuration Manager to check out a full ISim
license.
WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for
more information on the differences between the Lite and the Full version.
This is a Lite version of ISim.
Time resolution is 1 ps
Simulator is doing circuit initialization process.
Finished circuit initialization process.
```

```
64200163>rem ren Unary_Op_Bin_Tree.csv Unary_Op_Bin_Tree_64200163.csv
```

```
64200163>xst -ifn unary_vhdl93.xst
Release 14.7 - xst P.20131013 (nt64)
Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.
--> Parameter TMPDIR set to xst/projnav.tmp
```

```
Total REAL time to Xst completion: 1.00 secs
Total CPU time to Xst completion: 0.23 secs
```

```
--> Parameter xsthdpdir set to xst
```

```
Total REAL time to Xst completion: 1.00 secs
```

Total CPU time to Xst completion: 0.23 secs

-->

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```
=====
*      Synthesis Options Summary      *
=====
```

---- Source Parameters

Input File Name : "./unary_vhd193.prj"
Ignore Synthesis Constraint File : NO

---- Target Parameters

Output File Name : "reduction_operators"
Output Format : NGC
Target Device : xc6slx4-3-tqg144

---- Source Options

Top Module Name : reduction_operators
Automatic FSM Extraction : YES
FSM Encoding Algorithm : Auto
Safe Implementation : No
FSM Style : LUT
RAM Extraction : Yes
RAM Style : Auto
ROM Extraction : Yes
Shift Register Extraction : YES
ROM Style : Auto
Resource Sharing : YES
Asynchronous To Synchronous : NO
Shift Register Minimum Size : 2
Use DSP Block : Auto
Automatic Register Balancing : No

---- Target Options

LUT Combining : Auto
Reduce Control Sets : Auto
Add IO Buffers : YES
Global Maximum Fanout : 100000
Add Generic Clock Buffer(BUFG) : 16

Register Duplication : YES
Optimize Instantiated Primitives : NO
Use Clock Enable : Auto
Use Synchronous Set : Auto
Use Synchronous Reset : Auto
Pack IO Registers into IOBs : Auto
Equivalent register Removal : YES

---- General Options

Optimization Goal : Speed
Optimization Effort : 1
Power Reduction : NO
Keep Hierarchy : No
Netlist Hierarchy : As_Optimized
RTL Output : Yes
Global Optimization : AllClockNets
Read Cores : YES
Write Timing Constraints : NO
Cross Clock Analysis : NO
Hierarchy Separator : /
Bus Delimiter : <>
Case Specifier : Maintain
Slice Utilization Ratio : 100
BRAM Utilization Ratio : 100
DSP48 Utilization Ratio : 100
Auto BRAM Packing : NO
Slice Utilization Ratio Delta : 5

=====

=====

* HDL Parsing *

=====

Parsing VHDL file "64200163\unary_operators_vhdl_93.vhd" into library work
Parsing entity <reduction_operators>.
Parsing architecture <vhdl_93_process> of entity <reduction_operators>.

=====

* HDL Elaboration *

=====

Elaborating entity <reduction_operators> (architecture <vhdl_93_process>) with
generics from library <work>.

=====

* HDL Synthesis *

=====

Synthesizing Unit <reduction_operators>.
Related source file is "64200163\unary_operators_vhdl_93.vhd".
N = 64
Summary:
inferred 128 Multiplexer(s).
Unit <reduction_operators> synthesized.

=====

HDL Synthesis Report

Macro Statistics

```
# Multiplexers          : 128
 1-bit 2-to-1 multiplexer : 128
# Xors                  : 1
 1-bit xor64           : 1
```

=====

=====

```
*      Advanced HDL Synthesis      *
```

=====

=====

Advanced HDL Synthesis Report

Macro Statistics

```
# Multiplexers          : 128
 1-bit 2-to-1 multiplexer : 128
# Xors                  : 1
 1-bit xor64           : 1
```

=====

=====

```
*      Low Level Synthesis      *
```

=====

Optimizing unit <reduction_operators> ...

Mapping all equations...

Building and optimizing final netlist ...

Found area constraint ratio of 100 (+ 5) on block reduction_operators, actual ratio is 1.

Final Macro Processing ...

=====

Final Register Report

Found no macro

=====

=====

```
*      Partition Report      *
```

=====

Partition Implementation Status

No Partitions were found in this design.

=====

```
*      Design Summary      *
```

=====

Top Level Output File Name : reduction_operators.ngc

Primitive and Black Box Usage:

```
-----  
# BELS      : 59  
# GND       : 1  
# LUT4      : 3  
# LUT6      : 32  
# MUXCY     : 22  
# VCC       : 1  
# IO Buffers : 67  
# IBUF      : 64  
# OBUF      : 3
```

Device utilization summary:

Selected Device : 6slx4tqg144-3

Slice Logic Utilization:

Number of Slice LUTs: 35 out of 2400 1%
Number used as Logic: 35 out of 2400 1%

Slice Logic Distribution:

Number of LUT Flip Flop pairs used: 35
Number with an unused Flip Flop: 35 out of 35 100%
Number with an unused LUT: 0 out of 35 0%
Number of fully used LUT-FF pairs: 0 out of 35 0%
Number of unique control sets: 0

IO Utilization:

Number of IOs: 67
Number of bonded IOBs: 67 out of 102 65%

Specific Feature Utilization:

Partition Resource Summary:

No Partitions were found in this design.

=====

Timing Report

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.
FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT
GENERATED AFTER PLACE-and-ROUTE.

Clock Information:

No clock signals found in this design

Asynchronous Control Signals Information:

No asynchronous control signals found in this design

Timing Summary:

Speed Grade: -3

Minimum period: No path found
Minimum input arrival time before clock: No path found
Maximum output required time after clock: No path found
Maximum combinational path delay: 7.522ns

Timing Details:

All values displayed in nanoseconds (ns)

=====

Timing constraint: Default path analysis

Total number of paths / destination ports: 192 / 3

Delay: 7.522ns (Levels of Logic = 5)

Source: A<22> (PAD)

Destination: reduced_XOR (PAD)

Data Path: A<22> to reduced_XOR

Gate Net

Cell:in->out fanout Delay Delay Logical Name (Net Name)

IBUF:I->O 3 1.222 1.015 A_22_IBUF (A_22_IBUF)

LUT6:I0->O 1 0.203 0.944 Mxor_reduced_XOR_xo<0>3 (Mxor_reduced_XOR_xo<0>2)

LUT6:I0->O 1 0.203 0.580 Mxor_reduced_XOR_xo<0>14_SW0 (N01)

LUT6:I5->O 1 0.205 0.579 Mxor_reduced_XOR_xo<0>14 (reduced_XOR_OBUF)

OBUF:I->O 2.571 reduced_XOR_OBUF (reduced_XOR)

Total 7.522ns (4.404ns logic, 3.118ns route)

(58.5% logic, 41.5% route)

=====

Cross Clock Domains Report:

=====

Total REAL time to Xst completion: 10.00 secs

Total CPU time to Xst completion: 9.99 secs

-->

Total memory usage is 4487516 kilobytes

Number of errors : 0 (0 filtered)

Number of warnings : 0 (0 filtered)

Number of infos : 0 (0 filtered)

64200163>fuse -incremental -o unary_vhdl93_tb_isim_beh.exe -prj

unary_vhdl93_tb.prj -top reduction_operators_tb

Running: C:\Xilinx\14.7\ISE_DS\ISE\bin\nt64\unwrapped\fuse.exe -incremental -o

unary_vhdl93_tb_isim_beh.exe -prj unary_vhdl93_tb.prj -top reduction_operators_tb

ISim P.20131013 (signature 0x7708f090)

Number of CPUs detected in this system: 8

Turning on mult-threading, number of parallel sub-compilation jobs: 16

Determining compilation order of HDL files

Parsing VHDL file "unary_operators_vhdl_93.vhd" into library work

Parsing VHDL file "unary_operators_vhdl93_IDEAL_tb.vhd" into library work

```
Starting static elaboration
Completed static elaboration
Compiling package standard
Compiling package std_logic_1164
Compiling package numeric_std
Compiling package textio
Compiling package std_logic_textio
Compiling architecture vhdl_93_process of entity reduction_operators
[\\reduction_operators(3)\\]
Compiling architecture test of entity reduction_operators_tb
Time Resolution for simulation is 1ps.
Waiting for 1 sub-compilation(s) to finish...
Compiled 8 VHDL Units
Built simulation executable unary_vhdl93_tb_isim_beh.exe
Fuse Memory Usage: 36884 KB
Fuse CPU Usage: 874 ms
```

```
64200163>if exist reduction_operators.csv del reduction_operators.csv
```

```
64200163>if exist reduction_operators_64200163.csv del
reduction_operators_64200163.csv
```

```
64200163>unary_vhdl93_tb_isim_beh.exe -tclbatch isim.tcl -wdb
unary_vhdl93_tb_isim_beh.wdb
ISim P.20131013 (signature 0x7708f090)
WARNING: A WEBPACK license was found.
WARNING: Please use Xilinx License Configuration Manager to check out a full ISim
license.
WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for
more information on the differences between the Lite and the Full version.
This is a Lite version of ISim.
Time resolution is 1 ps
Simulator is doing circuit initialization process.
Finished circuit initialization process.
```

```
64200163>rem ren reduction_operators.csv reduction_operators_64200163.csv
```

```
-- *****
-- **** STUDENT: 64200238
-- *****
-- KOMENTARJI K OCENI NALOGE
-- Matej Možek: Ni pripomb
-- *****
```

```
64200238>if not exist "xst" mkdir xst
```

```
64200238>cd XST
```

```
64200238\xst>if not exist "projnav.tmp" mkdir "projnav.tmp"
```

```
64200238\xst>cd ..
```

```
64200238>xst -ifn unary_tree.xst
Release 14.7 - xst P.20131013 (nt64)
Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.
--> Parameter TMPDIR set to xst/projnav.tmp
```

```
Total REAL time to Xst completion: 0.00 secs
```

```
Total CPU time to Xst completion: 0.24 secs
```

```
--> Parameter xsthdpdir set to xst
```

```
Total REAL time to Xst completion: 0.00 secs
```

```
Total CPU time to Xst completion: 0.24 secs
```

```
-->
```

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 - 8.4.5) Cross Clock Domains Report

```
=====
*      Synthesis Options Summary      *
=====
```

---- Source Parameters

```
Input File Name      : "unary_tree.prj"
Ignore Synthesis Constraint File : NO
```

---- Target Parameters

```
Output File Name     : "Unary_Op_Bin_Tree"
```

Output Format : NGC
Target Device : xc6slx4-3-tqg144

----- Source Options

Top Module Name : Unary_Op_Bin_Tree
Automatic FSM Extraction : YES
FSM Encoding Algorithm : Auto
Safe Implementation : No
FSM Style : LUT
RAM Extraction : Yes
RAM Style : Auto
ROM Extraction : Yes
Shift Register Extraction : YES
ROM Style : Auto
Resource Sharing : YES
Asynchronous To Synchronous : NO
Shift Register Minimum Size : 2
Use DSP Block : Auto
Automatic Register Balancing : No

----- Target Options

LUT Combining : Auto
Reduce Control Sets : Auto
Add IO Buffers : YES
Global Maximum Fanout : 100000
Add Generic Clock Buffer(BUFG) : 16
Register Duplication : YES
Optimize Instantiated Primitives : NO
Use Clock Enable : Auto
Use Synchronous Set : Auto
Use Synchronous Reset : Auto
Pack IO Registers into IOBs : Auto
Equivalent register Removal : YES

----- General Options

Optimization Goal : Speed
Optimization Effort : 1
Power Reduction : NO
Keep Hierarchy : No
Netlist Hierarchy : As_Optimized
RTL Output : Yes
Global Optimization : AllClockNets
Read Cores : YES
Write Timing Constraints : NO
Cross Clock Analysis : NO
Hierarchy Separator : /
Bus Delimiter : <>
Case Specifier : Maintain
Slice Utilization Ratio : 100
BRAM Utilization Ratio : 100
DSP48 Utilization Ratio : 100
Auto BRAM Packing : NO
Slice Utilization Ratio Delta : 5

=====

=====

* HDL Parsing *

=====

Parsing VHDL file "64200238\unary_op_xor_tree_lut6.vhd" into library work
Parsing entity <XorTreeStage>.
Parsing architecture <tree_of_xor_lut6> of entity <xortreestage>.
Parsing VHDL file "64200238\unary_op_tree.vhd" into library work
Parsing entity <Unary_Op_Bin_Tree>.
Parsing architecture <t> of entity <unary_op_bin_tree>.

```
=====
*          HDL Elaboration          *
=====
```

Elaborating entity <Unary_Op_Bin_Tree> (architecture <t>) with generics from library <work>.

Elaborating entity <XorTreeStage> (architecture <tree_of_xor_lut6>) with generics from library <work>.

Elaborating entity <XorTreeStage> (architecture <tree_of_xor_lut6>) with generics from library <work>.

Elaborating entity <XorTreeStage> (architecture <tree_of_xor_lut6>) with generics from library <work>.

Elaborating entity <XorTreeStage> (architecture <tree_of_xor_lut6>) with generics from library <work>.

Elaborating entity <XorTreeStage> (architecture <tree_of_xor_lut6>) with generics from library <work>.

Elaborating entity <XorTreeStage> (architecture <tree_of_xor_lut6>) with generics from library <work>.

Elaborating entity <XorTreeStage> (architecture <tree_of_xor_lut6>) with generics from library <work>.

Elaborating entity <XorTreeStage> (architecture <tree_of_xor_lut6>) with generics from library <work>.

Elaborating entity <XorTreeStage> (architecture <tree_of_xor_lut6>) with generics from library <work>.

```
=====
*          HDL Synthesis            *
=====
```

Synthesizing Unit <Unary_Op_Bin_Tree>.
Related source file is "64200238\unary_op_tree.vhd".
N = 4096
Summary:
no macro.
Unit <Unary_Op_Bin_Tree> synthesized.

Synthesizing Unit <XorTreeStage_1>.
Related source file is "64200238\unary_op_xor_tree_lut6.vhd".
N = 4096
Summary:
no macro.
Unit <XorTreeStage_1> synthesized.

Synthesizing Unit <XorTreeStage_2>.
Related source file is "64200238\unary_op_xor_tree_lut6.vhd".
N = 683
Summary:
no macro.
Unit <XorTreeStage_2> synthesized.

Synthesizing Unit <XorTreeStage_3>.
Related source file is "64200238\unary_op_xor_tree_lut6.vhd".
N = 114
Summary:
no macro.
Unit <XorTreeStage_3> synthesized.

Synthesizing Unit <XorTreeStage_4>.
Related source file is "64200238\unary_op_xor_tree_lut6.vhd".
N = 19
Summary:
no macro.
Unit <XorTreeStage_4> synthesized.

Synthesizing Unit <XorTreeStage_5>.
Related source file is "64200238\unary_op_xor_tree_lut6.vhd".
N = 4
Summary:
no macro.
Unit <XorTreeStage_5> synthesized.

Synthesizing Unit <XorTreeStage_6>.
Related source file is "64200238\unary_op_xor_tree_lut6.vhd".
N = 3
Summary:
no macro.
Unit <XorTreeStage_6> synthesized.

Synthesizing Unit <XorTreeStage_7>.
Related source file is "64200238\unary_op_xor_tree_lut6.vhd".
N = 113
Summary:
no macro.
Unit <XorTreeStage_7> synthesized.

Synthesizing Unit <XorTreeStage_8>.
Related source file is "64200238\unary_op_xor_tree_lut6.vhd".
N = 18
Summary:
no macro.
Unit <XorTreeStage_8> synthesized.

Synthesizing Unit <XorTreeStage_9>.
Related source file is "64200238\unary_op_xor_tree_lut6.vhd".
N = 682
Summary:
no macro.
Unit <XorTreeStage_9> synthesized.

=====
HDL Synthesis Report

Found no macro

```
=====
*      Advanced HDL Synthesis      *
=====
```

```
=====
Advanced HDL Synthesis Report
=====
```

Found no macro

```
=====
*      Low Level Synthesis      *
=====
```

Optimizing unit <Unary_Op_Bin_Tree> ...

Mapping all equations...

Building and optimizing final netlist ...

Found area constraint ratio of 100 (+ 5) on block Unary_Op_Bin_Tree, actual ratio is 94.

Final Macro Processing ...

```
=====
Final Register Report
=====
```

Found no macro

```
=====
*      Partition Report      *
=====
```

Partition Implementation Status

No Partitions were found in this design.

```
=====
*      Design Summary      *
=====
```

Top Level Output File Name : Unary_Op_Bin_Tree.ngc

Primitive and Black Box Usage:

# BELS	: 1555
# LUT3	: 1088
# LUT4	: 208
# LUT6	: 259
# IO Buffers	: 4097
# IBUF	: 4096
# OBUF	: 1

Device utilization summary:

Selected Device : 6slx4tqg144-3

Slice Logic Utilization:

Number of Slice LUTs: 1555 out of 2400 64%
Number used as Logic: 1555 out of 2400 64%

Slice Logic Distribution:

Number of LUT Flip Flop pairs used: 1555
Number with an unused Flip Flop: 1555 out of 1555 100%
Number with an unused LUT: 0 out of 1555 0%
Number of fully used LUT-FF pairs: 0 out of 1555 0%
Number of unique control sets: 0

IO Utilization:

Number of IOs: 4097
Number of bonded IOBs: 4097 out of 102 4016% (*)

Specific Feature Utilization:

WARNING:Xst:1336 - (*) More than 100% of Device resources are used

Partition Resource Summary:

No Partitions were found in this design.

=====

Timing Report

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.
FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT
GENERATED AFTER PLACE-and-ROUTE.

Clock Information:

No clock signals found in this design

Asynchronous Control Signals Information:

No asynchronous control signals found in this design

Timing Summary:

Speed Grade: -3

Minimum period: No path found
Minimum input arrival time before clock: No path found
Maximum output required time after clock: No path found
Maximum combinational path delay: 10.106ns

Timing Details:

All values displayed in nanoseconds (ns)

```

=====
Timing constraint: Default path analysis
Total number of paths / destination ports: 4096 / 1
-----
Delay:      10.106ns (Levels of Logic = 7)
Source:     I<4092> (PAD)
Destination: O_Xor (PAD)

Data Path: I<4092> to O_Xor
Gate Net
Cell:in->out fanout Delay Delay Logical Name (Net Name)
-----
IBUF:I->O      1 1.222 0.827 I_4092_IBUF (I_4092_IBUF)
LUT4:I0->O     1 0.320 0.944
U_Xor/Stages.Stage1/Stages.Stage1/Stages.Stage1/Stages.Stage1/Stage_xor_4.XOR_LUT4
(U_Xor/Stages.Stage1/Stages.Stage1/Stages.Stage1/Stages.ladja1)
LUT6:I0->O     1 0.203 0.944
U_Xor/Stages.Stage1/Stages.Stage1/Stages.Stage1/Stages.XOR6_LUT6
(U_Xor/Stages.Stage1/Stages.Stage1/Stages.ladja1)
LUT6:I0->O     1 0.203 0.944 U_Xor/Stages.Stage1/Stages.Stage1/Stages.XOR6_LUT6
(U_Xor/Stages.Stage1/Stages.ladja1)
LUT6:I0->O     1 0.203 0.944 U_Xor/Stages.Stage1/Stages.XOR6_LUT6
(U_Xor/Stages.ladja1)
LUT6:I0->O     1 0.203 0.579 U_Xor/Stages.XOR6_LUT6 (O_Xor_OBUF)
OBUF:I->O      2.571 O_Xor_OBUF (O_Xor)
-----
Total      10.106ns (4.925ns logic, 5.181ns route)
          (48.7% logic, 51.3% route)
=====

```

Cross Clock Domains Report:

```

=====
Total REAL time to Xst completion: 17.00 secs
Total CPU time to Xst completion: 16.45 secs

```

-->

Total memory usage is 4538344 kilobytes

```

Number of errors : 0 ( 0 filtered)
Number of warnings : 1 ( 0 filtered)
Number of infos : 0 ( 0 filtered)

```

```

64200238>fuse -incremental -o unary_tree_tb_isim_beh.exe -prj unary_tree_tb.prj -
top Unary_Op_Bin_Tree_tb
Running: C:\Xilinx\14.7\ISE_DS\ISE\bin\nt64\unwrapped\fuse.exe -incremental -o
unary_tree_tb_isim_beh.exe -prj unary_tree_tb.prj -top Unary_Op_Bin_Tree_tb
ISim P.20131013 (signature 0x7708f090)
Number of CPUs detected in this system: 8
Turning on mult-threading, number of parallel sub-compilation jobs: 16
Determining compilation order of HDL files
Parsing VHDL file "slv_image_pkg.vhd" into library work
Parsing VHDL file "unary_op_xor_tree_lut6.vhd" into library work
Parsing VHDL file "unary_op_tree.vhd" into library work

```

```

Parsing VHDL file "unary_op_tree_IDEAL_tb.vhd" into library work
Starting static elaboration
Completed static elaboration
Compiling package standard
Compiling package std_logic_1164
Compiling package numeric_std
Compiling package textio
Compiling package std_logic_textio
Compiling package slv_image_pkg
Compiling package vcomponents
Compiling package vital_timing
Compiling package vital_primitives
Compiling package vpkg
Compiling architecture lut3_v of entity LUT3 [\LUT3("10010110")(0,7)\]
Compiling architecture tree_of_xor_lut6 of entity XorTreeStage [\XorTreeStage(3)\]
Compiling architecture tree_of_xor_lut6 of entity XorTreeStage [\XorTreeStage(2)\]
Compiling architecture lut6_v of entity LUT6 [\LUT6("0110100110010110100101100...")
Compiling architecture tree_of_xor_lut6 of entity XorTreeStage
[\XorTreeStage(16)\]
Compiling architecture t of entity Unary_Op_Bin_Tree [\Unary_Op_Bin_Tree(16)\]
Compiling architecture test of entity unary_op_bin_tree_tb
Time Resolution for simulation is 1ps.
Compiled 23 VHDL Units
Built simulation executable unary_tree_tb_isim_beh.exe
Fuse Memory Usage: 59964 KB
Fuse CPU Usage: 1406 ms

```

```
64200238>if exist Unary_Op_Bin_Tree.csv del Unary_Op_Bin_Tree.csv
```

```
64200238>if exist Unary_Op_Bin_Tree_64200238.csv del
Unary_Op_Bin_Tree_64200238.csv
```

```

64200238>unary_tree_tb_isim_beh.exe -tclbatch isim.tcl -wdb
unary_tree_tb_isim_beh.wdb
ISim P.20131013 (signature 0x7708f090)
WARNING: A WEBPACK license was found.
WARNING: Please use Xilinx License Configuration Manager to check out a full ISim
license.
WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for
more information on the differences between the Lite and the Full version.
This is a Lite version of ISim.
Time resolution is 1 ps
Simulator is doing circuit initialization process.
Finished circuit initialization process.

```

```
64200238>rem ren Unary_Op_Bin_Tree.csv Unary_Op_Bin_Tree_64200238.csv
```

```

64200238>xst -ifn unary_vhdl93.xst
Release 14.7 - xst P.20131013 (nt64)
Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.
--> Parameter TMPDIR set to xst/projnav.tmp

```

```

Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.27 secs

```

```
--> Parameter xsthdpdir set to xst
```

```

Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.27 secs

```

-->

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 - 8.4.5) Cross Clock Domains Report

```
=====
*      Synthesis Options Summary      *
```

----- Source Parameters

Input File Name : `"./unary_vhd193.prj"`
Ignore Synthesis Constraint File : NO

----- Target Parameters

Output File Name : `"reduction_operators"`
Output Format : NGC
Target Device : xc6slx4-3-tqg144

----- Source Options

Top Module Name : reduction_operators
Automatic FSM Extraction : YES
FSM Encoding Algorithm : Auto
Safe Implementation : No
FSM Style : LUT
RAM Extraction : Yes
RAM Style : Auto
ROM Extraction : Yes
Shift Register Extraction : YES
ROM Style : Auto
Resource Sharing : YES
Asynchronous To Synchronous : NO
Shift Register Minimum Size : 2
Use DSP Block : Auto
Automatic Register Balancing : No

----- Target Options

LUT Combining : Auto
Reduce Control Sets : Auto
Add IO Buffers : YES
Global Maximum Fanout : 100000
Add Generic Clock Buffer(BUFG) : 16
Register Duplication : YES

Optimize Instantiated Primitives : NO
Use Clock Enable : Auto
Use Synchronous Set : Auto
Use Synchronous Reset : Auto
Pack IO Registers into IOBs : Auto
Equivalent register Removal : YES

---- General Options

Optimization Goal : Speed
Optimization Effort : 1
Power Reduction : NO
Keep Hierarchy : No
Netlist Hierarchy : As_Optimized
RTL Output : Yes
Global Optimization : AllClockNets
Read Cores : YES
Write Timing Constraints : NO
Cross Clock Analysis : NO
Hierarchy Separator : /
Bus Delimiter : <>
Case Specifier : Maintain
Slice Utilization Ratio : 100
BRAM Utilization Ratio : 100
DSP48 Utilization Ratio : 100
Auto BRAM Packing : NO
Slice Utilization Ratio Delta : 5

=====

=====

* HDL Parsing *

=====

Parsing VHDL file "64200238\unary_operators_vhdl_93.vhd" into library work
Parsing entity <reduction_operators>.
Parsing architecture <vhdl_93_process> of entity <reduction_operators>.

=====

* HDL Elaboration *

=====

Elaborating entity <reduction_operators> (architecture <vhdl_93_process>) with
generics from library <work>.

=====

* HDL Synthesis *

=====

Synthesizing Unit <reduction_operators>.
Related source file is "64200238\unary_operators_vhdl_93.vhd".
N = 64
Summary:
inferred 128 Multiplexer(s).
Unit <reduction_operators> synthesized.

=====

HDL Synthesis Report

Macro Statistics

Multiplexers : 128

```
1-bit 2-to-1 multiplexer      : 128
# Xors                        : 1
1-bit xor64                   : 1
```

```
=====
*      Advanced HDL Synthesis      *
```

```
=====
Advanced HDL Synthesis Report
```

```
Macro Statistics
# Multiplexers                : 128
1-bit 2-to-1 multiplexer      : 128
# Xors                        : 1
1-bit xor64                   : 1
```

```
=====
*      Low Level Synthesis      *
```

```
Optimizing unit <reduction_operators> ...
```

```
Mapping all equations...
```

```
Building and optimizing final netlist ...
```

```
Found area constraint ratio of 100 (+ 5) on block reduction_operators, actual
ratio is 1.
```

```
Final Macro Processing ...
```

```
=====
Final Register Report
```

```
Found no macro
```

```
=====
*      Partition Report      *
```

```
Partition Implementation Status
```

```
-----
No Partitions were found in this design.
```

```
=====
*      Design Summary      *
```

```
Top Level Output File Name : reduction_operators.ngc
```

```
Primitive and Black Box Usage:
```



```
# BELS      : 59
# GND       : 1
# LUT4      : 3
# LUT6      : 32
# MUXCY     : 22
# VCC       : 1
# IO Buffers : 67
# IBUF      : 64
# OBUF      : 3
```

Device utilization summary:

Selected Device : 6slx4tqg144-3

Slice Logic Utilization:

Number of Slice LUTs: 35 out of 2400 1%
Number used as Logic: 35 out of 2400 1%

Slice Logic Distribution:

Number of LUT Flip Flop pairs used: 35
Number with an unused Flip Flop: 35 out of 35 100%
Number with an unused LUT: 0 out of 35 0%
Number of fully used LUT-FF pairs: 0 out of 35 0%
Number of unique control sets: 0

IO Utilization:

Number of IOs: 67
Number of bonded IOBs: 67 out of 102 65%

Specific Feature Utilization:

Partition Resource Summary:

No Partitions were found in this design.

=====

Timing Report

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.
FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT
GENERATED AFTER PLACE-and-ROUTE.

Clock Information:

No clock signals found in this design

Asynchronous Control Signals Information:

No asynchronous control signals found in this design

Timing Summary:

Speed Grade: -3

Minimum period: No path found
Minimum input arrival time before clock: No path found
Maximum output required time after clock: No path found
Maximum combinational path delay: 7.522ns

Timing Details:

All values displayed in nanoseconds (ns)

=====

Timing constraint: Default path analysis
Total number of paths / destination ports: 192 / 3

Delay: 7.522ns (Levels of Logic = 5)
Source: A<22> (PAD)
Destination: reduced_XOR (PAD)

Data Path: A<22> to reduced_XOR
Gate Net

Cell:	in->out	fanout	Delay	Delay	Logical Name (Net Name)

IBUF:	I->O	3	1.222	1.015	A_22_IBUF (A_22_IBUF)
LUT6:	I0->O	1	0.203	0.944	Mxor_reduced_XOR_xo<0>3 (Mxor_reduced_XOR_xo<0>2)
LUT6:	I0->O	1	0.203	0.580	Mxor_reduced_XOR_xo<0>14_SW0 (N01)
LUT6:	I5->O	1	0.205	0.579	Mxor_reduced_XOR_xo<0>14 (reduced_XOR_OBUF)
OBUF:	I->O		2.571		reduced_XOR_OBUF (reduced_XOR)

Total			7.522ns	(4.404ns logic, 3.118ns route)	(58.5% logic, 41.5% route)

=====

Cross Clock Domains Report:

=====

Total REAL time to Xst completion: 10.00 secs
Total CPU time to Xst completion: 10.01 secs

-->

Total memory usage is 4487516 kilobytes

Number of errors : 0 (0 filtered)
Number of warnings : 0 (0 filtered)
Number of infos : 0 (0 filtered)

64200238>fuse -incremental -o unary_vhdl93_tb_isim_beh.exe -prj
unary_vhdl93_tb.prj -top reduction_operators_tb
Running: C:\Xilinx\14.7\ISE_DS\ISE\bin\nt64\unwrapped\fuse.exe -incremental -o
unary_vhdl93_tb_isim_beh.exe -prj unary_vhdl93_tb.prj -top reduction_operators_tb
ISim P.20131013 (signature 0x7708f090)
Number of CPUs detected in this system: 8
Turning on mult-threading, number of parallel sub-compilation jobs: 16
Determining compilation order of HDL files
Parsing VHDL file "unary_operators_vhdl_93.vhd" into library work
Parsing VHDL file "unary_operators_vhdl93_IDEAL_tb.vhd" into library work
Starting static elaboration

```
Completed static elaboration
Compiling package standard
Compiling package std_logic_1164
Compiling package numeric_std
Compiling package textio
Compiling package std_logic_textio
Compiling architecture vhdl_93_process of entity reduction_operators
[\\reduction_operators(3)\\]
Compiling architecture test of entity reduction_operators_tb
Time Resolution for simulation is 1ps.
Waiting for 1 sub-compilation(s) to finish...
Compiled 8 VHDL Units
Built simulation executable unary_vhdl93_tb_isim_beh.exe
Fuse Memory Usage: 36820 KB
Fuse CPU Usage: 859 ms
```

```
64200238>if exist reduction_operators.csv del reduction_operators.csv
```

```
64200238>if exist reduction_operators_64200238.csv del
reduction_operators_64200238.csv
```

```
64200238>unary_vhdl93_tb_isim_beh.exe -tclbatch isim.tcl -wdb
unary_vhdl93_tb_isim_beh.wdb
ISim P.20131013 (signature 0x7708f090)
WARNING: A WEBPACK license was found.
WARNING: Please use Xilinx License Configuration Manager to check out a full ISim
license.
WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for
more information on the differences between the Lite and the Full version.
This is a Lite version of ISim.
Time resolution is 1 ps
Simulator is doing circuit initialization process.
Finished circuit initialization process.
```

```
64200238>rem ren reduction_operators.csv reduction_operators_64200238.csv
```

```
-- *****
-- **** STUDENT: 64200288
-- *****
-- KOMENTARJI K OCENI NALOGE
-- Matej Možek: Ni pripomb
-- *****
```

```
64200288>if not exist "xst" mkdir xst
```

```
64200288>cd XST
```

```
64200288\xst>if not exist "projnav.tmp" mkdir "projnav.tmp"
```

```
64200288\xst>cd ..
```

```
64200288>xst -ifn unary_tree.xst
Release 14.7 - xst P.20131013 (nt64)
Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.
--> Parameter TMPDIR set to xst/projnav.tmp
```

```
Total REAL time to Xst completion: 1.00 secs
```

```
Total CPU time to Xst completion: 0.24 secs
```

```
--> Parameter xsthdpdir set to xst
```

```
Total REAL time to Xst completion: 1.00 secs
```

```
Total CPU time to Xst completion: 0.24 secs
```

```
-->
```

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```
=====
*      Synthesis Options Summary      *
=====
```

---- Source Parameters

```
Input File Name      : "unary_tree.prj"
Ignore Synthesis Constraint File : NO
```

---- Target Parameters

```
Output File Name     : "Unary_Op_Bin_Tree"
```

Output Format : NGC
Target Device : xc6slx4-3-tqg144

----- Source Options

Top Module Name : Unary_Op_Bin_Tree
Automatic FSM Extraction : YES
FSM Encoding Algorithm : Auto
Safe Implementation : No
FSM Style : LUT
RAM Extraction : Yes
RAM Style : Auto
ROM Extraction : Yes
Shift Register Extraction : YES
ROM Style : Auto
Resource Sharing : YES
Asynchronous To Synchronous : NO
Shift Register Minimum Size : 2
Use DSP Block : Auto
Automatic Register Balancing : No

----- Target Options

LUT Combining : Auto
Reduce Control Sets : Auto
Add IO Buffers : YES
Global Maximum Fanout : 100000
Add Generic Clock Buffer(BUFG) : 16
Register Duplication : YES
Optimize Instantiated Primitives : NO
Use Clock Enable : Auto
Use Synchronous Set : Auto
Use Synchronous Reset : Auto
Pack IO Registers into IOBs : Auto
Equivalent register Removal : YES

----- General Options

Optimization Goal : Speed
Optimization Effort : 1
Power Reduction : NO
Keep Hierarchy : No
Netlist Hierarchy : As_Optimized
RTL Output : Yes
Global Optimization : AllClockNets
Read Cores : YES
Write Timing Constraints : NO
Cross Clock Analysis : NO
Hierarchy Separator : /
Bus Delimiter : <>
Case Specifier : Maintain
Slice Utilization Ratio : 100
BRAM Utilization Ratio : 100
DSP48 Utilization Ratio : 100
Auto BRAM Packing : NO
Slice Utilization Ratio Delta : 5

=====

=====

* HDL Parsing *

=====

Parsing VHDL file "64200288\unary_op_xor_tree_lut6.vhd" into library work
Parsing entity <XorTreeStage>.
Parsing architecture <tree_of_xor_lut6> of entity <xortreestage>.
Parsing VHDL file "64200288\unary_op_tree.vhd" into library work
Parsing entity <Unary_Op_Bin_Tree>.
Parsing architecture <t> of entity <unary_op_bin_tree>.

```
=====
*          HDL Elaboration          *
=====
```

Elaborating entity <Unary_Op_Bin_Tree> (architecture <t>) with generics from library <work>.

Elaborating entity <XorTreeStage> (architecture <tree_of_xor_lut6>) with generics from library <work>.

Elaborating entity <XorTreeStage> (architecture <tree_of_xor_lut6>) with generics from library <work>.

Elaborating entity <XorTreeStage> (architecture <tree_of_xor_lut6>) with generics from library <work>.

Elaborating entity <XorTreeStage> (architecture <tree_of_xor_lut6>) with generics from library <work>.

Elaborating entity <XorTreeStage> (architecture <tree_of_xor_lut6>) with generics from library <work>.

Elaborating entity <XorTreeStage> (architecture <tree_of_xor_lut6>) with generics from library <work>.

Elaborating entity <XorTreeStage> (architecture <tree_of_xor_lut6>) with generics from library <work>.

Elaborating entity <XorTreeStage> (architecture <tree_of_xor_lut6>) with generics from library <work>.

Elaborating entity <XorTreeStage> (architecture <tree_of_xor_lut6>) with generics from library <work>.

```
=====
*          HDL Synthesis            *
=====
```

Synthesizing Unit <Unary_Op_Bin_Tree>.
Related source file is "64200288\unary_op_tree.vhd".
N = 4096
Summary:
no macro.
Unit <Unary_Op_Bin_Tree> synthesized.

Synthesizing Unit <XorTreeStage_1>.
Related source file is "64200288\unary_op_xor_tree_lut6.vhd".
N = 4096
Summary:
no macro.
Unit <XorTreeStage_1> synthesized.

Synthesizing Unit <XorTreeStage_2>.
Related source file is "64200288\unary_op_xor_tree_lut6.vhd".
N = 683
Summary:
no macro.
Unit <XorTreeStage_2> synthesized.

Synthesizing Unit <XorTreeStage_3>.
Related source file is "64200288\unary_op_xor_tree_lut6.vhd".
N = 114
Summary:
no macro.
Unit <XorTreeStage_3> synthesized.

Synthesizing Unit <XorTreeStage_4>.
Related source file is "64200288\unary_op_xor_tree_lut6.vhd".
N = 19
Summary:
no macro.
Unit <XorTreeStage_4> synthesized.

Synthesizing Unit <XorTreeStage_5>.
Related source file is "64200288\unary_op_xor_tree_lut6.vhd".
N = 4
Summary:
no macro.
Unit <XorTreeStage_5> synthesized.

Synthesizing Unit <XorTreeStage_6>.
Related source file is "64200288\unary_op_xor_tree_lut6.vhd".
N = 3
Summary:
no macro.
Unit <XorTreeStage_6> synthesized.

Synthesizing Unit <XorTreeStage_7>.
Related source file is "64200288\unary_op_xor_tree_lut6.vhd".
N = 113
Summary:
no macro.
Unit <XorTreeStage_7> synthesized.

Synthesizing Unit <XorTreeStage_8>.
Related source file is "64200288\unary_op_xor_tree_lut6.vhd".
N = 18
Summary:
no macro.
Unit <XorTreeStage_8> synthesized.

Synthesizing Unit <XorTreeStage_9>.
Related source file is "64200288\unary_op_xor_tree_lut6.vhd".
N = 682
Summary:
no macro.
Unit <XorTreeStage_9> synthesized.

=====
HDL Synthesis Report

Found no macro

```
=====
*      Advanced HDL Synthesis      *
=====
```

```
=====
Advanced HDL Synthesis Report
=====
```

Found no macro

```
=====
*      Low Level Synthesis      *
=====
```

Optimizing unit <Unary_Op_Bin_Tree> ...

Mapping all equations...

Building and optimizing final netlist ...

Found area constraint ratio of 100 (+ 5) on block Unary_Op_Bin_Tree, actual ratio is 94.

Final Macro Processing ...

```
=====
Final Register Report
=====
```

Found no macro

```
=====
*      Partition Report      *
=====
```

Partition Implementation Status

No Partitions were found in this design.

```
=====
*      Design Summary      *
=====
```

Top Level Output File Name : Unary_Op_Bin_Tree.ngc

Primitive and Black Box Usage:

# BELS	: 1555
# LUT3	: 1088
# LUT4	: 208
# LUT6	: 259
# IO Buffers	: 4097
# IBUF	: 4096
# OBUF	: 1

Device utilization summary:

Selected Device : 6slx4tqg144-3

Slice Logic Utilization:

Number of Slice LUTs: 1555 out of 2400 64%
Number used as Logic: 1555 out of 2400 64%

Slice Logic Distribution:

Number of LUT Flip Flop pairs used: 1555
Number with an unused Flip Flop: 1555 out of 1555 100%
Number with an unused LUT: 0 out of 1555 0%
Number of fully used LUT-FF pairs: 0 out of 1555 0%
Number of unique control sets: 0

IO Utilization:

Number of IOs: 4097
Number of bonded IOBs: 4097 out of 102 4016% (*)

Specific Feature Utilization:

WARNING:Xst:1336 - (*) More than 100% of Device resources are used

Partition Resource Summary:

No Partitions were found in this design.

=====

Timing Report

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.
FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT
GENERATED AFTER PLACE-and-ROUTE.

Clock Information:

No clock signals found in this design

Asynchronous Control Signals Information:

No asynchronous control signals found in this design

Timing Summary:

Speed Grade: -3

Minimum period: No path found
Minimum input arrival time before clock: No path found
Maximum output required time after clock: No path found
Maximum combinational path delay: 10.106ns

Timing Details:

All values displayed in nanoseconds (ns)

```

=====
Timing constraint: Default path analysis
Total number of paths / destination ports: 4096 / 1
-----
Delay:      10.106ns (Levels of Logic = 7)
Source:     I<4092> (PAD)
Destination: O_Xor (PAD)

Data Path: I<4092> to O_Xor
Gate Net
Cell:in->out fanout Delay Delay Logical Name (Net Name)
-----
IBUF:I->O      1 1.222 0.827 I_4092_IBUF (I_4092_IBUF)
LUT4:I0->O     1 0.320 0.944
U_Xor/Stages.Stage1/Stages.Stage1/Stages.Stage1/Stages.Stage1/Stage_xor_4.XOR_LUT4
(U_Xor/Stages.Stage1/Stages.Stage1/Stages.Stage1/Stages.testVar1)
LUT6:I0->O     1 0.203 0.944
U_Xor/Stages.Stage1/Stages.Stage1/Stages.Stage1/Stages.XOR6_LUT6
(U_Xor/Stages.Stage1/Stages.Stage1/Stages.testVar1)
LUT6:I0->O     1 0.203 0.944 U_Xor/Stages.Stage1/Stages.Stage1/Stages.XOR6_LUT6
(U_Xor/Stages.Stage1/Stages.testVar1)
LUT6:I0->O     1 0.203 0.944 U_Xor/Stages.Stage1/Stages.XOR6_LUT6
(U_Xor/Stages.testVar1)
LUT6:I0->O     1 0.203 0.579 U_Xor/Stages.XOR6_LUT6 (O_Xor_OBUF)
OBUF:I->O      2.571 O_Xor_OBUF (O_Xor)
-----
Total      10.106ns (4.925ns logic, 5.181ns route)
           (48.7% logic, 51.3% route)
=====

```

Cross Clock Domains Report:

```

=====
Total REAL time to Xst completion: 17.00 secs
Total CPU time to Xst completion: 16.86 secs

```

-->

Total memory usage is 4538368 kilobytes

```

Number of errors : 0 ( 0 filtered)
Number of warnings : 1 ( 0 filtered)
Number of infos : 0 ( 0 filtered)

```

```

64200288>fuse -incremental -o unary_tree_tb_isim_beh.exe -prj unary_tree_tb.prj -
top Unary_Op_Bin_Tree_tb
Running: C:\Xilinx\14.7\ISE_DS\ISE\bin\nt64\unwrapped\fuse.exe -incremental -o
unary_tree_tb_isim_beh.exe -prj unary_tree_tb.prj -top Unary_Op_Bin_Tree_tb
ISim P.20131013 (signature 0x7708f090)
Number of CPUs detected in this system: 8
Turning on mult-threading, number of parallel sub-compilation jobs: 16
Determining compilation order of HDL files
Parsing VHDL file "slv_image_pkg.vhd" into library work
Parsing VHDL file "unary_op_xor_tree_lut6.vhd" into library work
Parsing VHDL file "unary_op_tree.vhd" into library work

```

```

Parsing VHDL file "unary_op_tree_IDEAL_tb.vhd" into library work
Starting static elaboration
Completed static elaboration
Compiling package standard
Compiling package std_logic_1164
Compiling package numeric_std
Compiling package textio
Compiling package std_logic_textio
Compiling package slv_image_pkg
Compiling package vcomponents
Compiling package vital_timing
Compiling package vital_primitives
Compiling package vpkg
Compiling architecture lut3_v of entity LUT3 [\LUT3("10010110")(0,7)\]
Compiling architecture tree_of_xor_lut6 of entity XorTreeStage [\XorTreeStage(3)\]
Compiling architecture tree_of_xor_lut6 of entity XorTreeStage [\XorTreeStage(2)\]
Compiling architecture lut6_v of entity LUT6 [\LUT6("0110100110010110100101100...")
Compiling architecture tree_of_xor_lut6 of entity XorTreeStage
[\XorTreeStage(16)\]
Compiling architecture t of entity Unary_Op_Bin_Tree [\Unary_Op_Bin_Tree(16)\]
Compiling architecture test of entity unary_op_bin_tree_tb
Time Resolution for simulation is 1ps.
Compiled 23 VHDL Units
Built simulation executable unary_tree_tb_isim_beh.exe
Fuse Memory Usage: 60120 KB
Fuse CPU Usage: 1436 ms

```

```
64200288>if exist Unary_Op_Bin_Tree.csv del Unary_Op_Bin_Tree.csv
```

```
64200288>if exist Unary_Op_Bin_Tree_64200288.csv del
Unary_Op_Bin_Tree_64200288.csv
```

```

64200288>unary_tree_tb_isim_beh.exe -tclbatch isim.tcl -wdb
unary_tree_tb_isim_beh.wdb
ISim P.20131013 (signature 0x7708f090)
WARNING: A WEBPACK license was found.
WARNING: Please use Xilinx License Configuration Manager to check out a full ISim
license.
WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for
more information on the differences between the Lite and the Full version.
This is a Lite version of ISim.
Time resolution is 1 ps
Simulator is doing circuit initialization process.
Finished circuit initialization process.

```

```
64200288>rem ren Unary_Op_Bin_Tree.csv Unary_Op_Bin_Tree_64200288.csv
```

```

64200288>xst -ifn unary_vhdl93.xst
Release 14.7 - xst P.20131013 (nt64)
Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.
--> Parameter TMPDIR set to xst/projnav.tmp

```

```

Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.24 secs

```

```
--> Parameter xsthdpdir set to xst
```

```

Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.24 secs

```

-->

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 - 8.4.5) Cross Clock Domains Report

```
=====
*      Synthesis Options Summary      *
=====
```

---- Source Parameters

Input File Name : **"/unary_vhd193.prj"**
Ignore Synthesis Constraint File : NO

---- Target Parameters

Output File Name : **"reduction_operators"**
Output Format : NGC
Target Device : xc6slx4-3-tqg144

---- Source Options

Top Module Name : reduction_operators
Automatic FSM Extraction : YES
FSM Encoding Algorithm : Auto
Safe Implementation : No
FSM Style : LUT
RAM Extraction : Yes
RAM Style : Auto
ROM Extraction : Yes
Shift Register Extraction : YES
ROM Style : Auto
Resource Sharing : YES
Asynchronous To Synchronous : NO
Shift Register Minimum Size : **2**
Use DSP Block : Auto
Automatic Register Balancing : No

---- Target Options

LUT Combining : Auto
Reduce Control Sets : Auto
Add IO Buffers : YES
Global Maximum Fanout : **100000**
Add Generic Clock Buffer(BUFG) : **16**
Register Duplication : YES

Optimize Instantiated Primitives : NO
Use Clock Enable : Auto
Use Synchronous Set : Auto
Use Synchronous Reset : Auto
Pack IO Registers into IOBs : Auto
Equivalent register Removal : YES

---- General Options

Optimization Goal : Speed
Optimization Effort : 1
Power Reduction : NO
Keep Hierarchy : No
Netlist Hierarchy : As_Optimized
RTL Output : Yes
Global Optimization : AllClockNets
Read Cores : YES
Write Timing Constraints : NO
Cross Clock Analysis : NO
Hierarchy Separator : /
Bus Delimiter : <>
Case Specifier : Maintain
Slice Utilization Ratio : 100
BRAM Utilization Ratio : 100
DSP48 Utilization Ratio : 100
Auto BRAM Packing : NO
Slice Utilization Ratio Delta : 5

=====

=====

* HDL Parsing *

=====

Parsing VHDL file "64200288\unary_operators_vhdl_93.vhd" into library work
Parsing entity <reduction_operators>.
Parsing architecture <vhdl_93_process> of entity <reduction_operators>.

=====

* HDL Elaboration *

=====

Elaborating entity <reduction_operators> (architecture <vhdl_93_process>) with
generics from library <work>.

=====

* HDL Synthesis *

=====

Synthesizing Unit <reduction_operators>.
Related source file is "64200288\unary_operators_vhdl_93.vhd".
N = 64
Summary:
inferred 128 Multiplexer(s).
Unit <reduction_operators> synthesized.

=====

HDL Synthesis Report

Macro Statistics

Multiplexers : 128

```
1-bit 2-to-1 multiplexer      : 128
# Xors                        : 1
1-bit xor64                   : 1
```

```
=====
*      Advanced HDL Synthesis      *
```

```
=====
Advanced HDL Synthesis Report
```

```
Macro Statistics
# Multiplexers              : 128
1-bit 2-to-1 multiplexer    : 128
# Xors                      : 1
1-bit xor64                 : 1
```

```
=====
*      Low Level Synthesis      *
```

```
Optimizing unit <reduction_operators> ...
```

```
Mapping all equations...
```

```
Building and optimizing final netlist ...
```

```
Found area constraint ratio of 100 (+ 5) on block reduction_operators, actual
ratio is 1.
```

```
Final Macro Processing ...
```

```
=====
Final Register Report
```

```
Found no macro
```

```
=====
*      Partition Report      *
```

```
Partition Implementation Status
```

```
-----
No Partitions were found in this design.
```

```
=====
*      Design Summary      *
```

```
Top Level Output File Name : reduction_operators.ngc
```

```
Primitive and Black Box Usage:
```

```
# BELS      : 59
# GND       : 1
# LUT4      : 3
# LUT6      : 32
# MUXCY     : 22
# VCC       : 1
# IO Buffers : 67
# IBUF      : 64
# OBUF      : 3
```

Device utilization summary:

Selected Device : 6slx4tqg144-3

Slice Logic Utilization:

Number of Slice LUTs: 35 out of 2400 1%
Number used as Logic: 35 out of 2400 1%

Slice Logic Distribution:

Number of LUT Flip Flop pairs used: 35
Number with an unused Flip Flop: 35 out of 35 100%
Number with an unused LUT: 0 out of 35 0%
Number of fully used LUT-FF pairs: 0 out of 35 0%
Number of unique control sets: 0

IO Utilization:

Number of IOs: 67
Number of bonded IOBs: 67 out of 102 65%

Specific Feature Utilization:

Partition Resource Summary:

No Partitions were found in this design.

=====

Timing Report

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.
FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT
GENERATED AFTER PLACE-and-ROUTE.

Clock Information:

No clock signals found in this design

Asynchronous Control Signals Information:

No asynchronous control signals found in this design

Timing Summary:

Speed Grade: -3

Minimum period: No path found
Minimum input arrival time before clock: No path found
Maximum output required time after clock: No path found
Maximum combinational path delay: 7.522ns

Timing Details:

All values displayed in nanoseconds (ns)

Timing constraint: Default path analysis

Total number of paths / destination ports: 192 / 3

Delay: 7.522ns (Levels of Logic = 5)

Source: A<22> (PAD)

Destination: reduced_XOR (PAD)

Data Path: A<22> to reduced_XOR

Gate Net

Cell:in->out fanout Delay Delay Logical Name (Net Name)

IBUF:I->O	3	1.222	1.015	A_22_IBUF	(A_22_IBUF)
LUT6:I0->O	1	0.203	0.944	Mxor_reduced_XOR_xo<0>3	(Mxor_reduced_XOR_xo<0>2)
LUT6:I0->O	1	0.203	0.580	Mxor_reduced_XOR_xo<0>14_SW0	(N01)
LUT6:I5->O	1	0.205	0.579	Mxor_reduced_XOR_xo<0>14	(reduced_XOR_OBUF)
OBUF:I->O	2	2.571		reduced_XOR_OBUF	(reduced_XOR)

Total 7.522ns (4.404ns logic, 3.118ns route)
(58.5% logic, 41.5% route)

Cross Clock Domains Report:

Total REAL time to Xst completion: 11.00 secs

Total CPU time to Xst completion: 10.57 secs

-->

Total memory usage is 4487516 kilobytes

Number of errors : 0 (0 filtered)

Number of warnings : 0 (0 filtered)

Number of infos : 0 (0 filtered)

64200288>fuse -incremental -o unary_vhdl93_tb_isim_beh.exe -prj

unary_vhdl93_tb.prj -top reduction_operators_tb

Running: C:\Xilinx\14.7\ISE_DS\ISE\bin\nt64\unwrapped\fuse.exe -incremental -o unary_vhdl93_tb_isim_beh.exe -prj unary_vhdl93_tb.prj -top reduction_operators_tb
ISim P.20131013 (signature 0x7708f090)

Number of CPUs detected in this system: 8

Turning on mult-threading, number of parallel sub-compilation jobs: 16

Determining compilation order of HDL files

Parsing VHDL file "unary_operators_vhdl_93.vhd" into library work

Parsing VHDL file "unary_operators_vhdl93_IDEAL_tb.vhd" into library work

Starting static elaboration

Completed static elaboration
Compiling package standard
Compiling package std_logic_1164
Compiling package numeric_std
Compiling package textio
Compiling package std_logic_textio
Compiling architecture vhdl_93_process of entity reduction_operators
[\\reduction_operators(3)\\]
Compiling architecture test of entity reduction_operators_tb
Time Resolution for simulation is 1ps.
Waiting for 1 sub-compilation(s) to finish...
Compiled 8 VHDL Units
Built simulation executable unary_vhdl93_tb_isim_beh.exe
Fuse Memory Usage: 36880 KB
Fuse CPU Usage: 921 ms

64200288>if exist reduction_operators.csv del reduction_operators.csv

64200288>if exist reduction_operators_64200288.csv del
reduction_operators_64200288.csv

64200288>unary_vhdl93_tb_isim_beh.exe -tclbatch isim.tcl -wdb
unary_vhdl93_tb_isim_beh.wdb
ISim P.20131013 (signature 0x7708f090)
WARNING: A WEBPACK license was found.
WARNING: Please use Xilinx License Configuration Manager to check out a full ISim
license.
WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for
more information on the differences between the Lite and the Full version.
This is a Lite version of ISim.
Time resolution is 1 ps
Simulator is doing circuit initialization process.
Finished circuit initialization process.

64200288>ren reduction_operators.csv reduction_operators_64200288.csv

```
-- *****
-- **** STUDENT: 64200296
-- *****
-- KOMENTARJI K OCENI NALOGE
-- Matej Možek: Ni pripomb
-- *****
```

```
64200296>if not exist "xst" mkdir xst
```

```
64200296>cd XST
```

```
64200296\xst>if not exist "projnav.tmp" mkdir "projnav.tmp"
```

```
64200296\xst>cd ..
```

```
64200296>xst -ifn unary_tree.xst
Release 14.7 - xst P.20131013 (nt64)
Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.
--> Parameter TMPDIR set to xst/projnav.tmp
```

```
Total REAL time to Xst completion: 1.00 secs
Total CPU time to Xst completion: 0.24 secs
```

```
--> Parameter xsthdpdir set to xst
```

```
Total REAL time to Xst completion: 1.00 secs
Total CPU time to Xst completion: 0.24 secs
```

```
-->
```

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 - 8.4.5) Cross Clock Domains Report

```
=====
*      Synthesis Options Summary      *
=====
```

---- Source Parameters

```
Input File Name      : "unary_tree.prj"
Ignore Synthesis Constraint File : NO
```

---- Target Parameters

```
Output File Name     : "Unary_Op_Bin_Tree"
```

Output Format : NGC
Target Device : xc6slx4-3-tqg144

----- Source Options

Top Module Name : Unary_Op_Bin_Tree
Automatic FSM Extraction : YES
FSM Encoding Algorithm : Auto
Safe Implementation : No
FSM Style : LUT
RAM Extraction : Yes
RAM Style : Auto
ROM Extraction : Yes
Shift Register Extraction : YES
ROM Style : Auto
Resource Sharing : YES
Asynchronous To Synchronous : NO
Shift Register Minimum Size : 2
Use DSP Block : Auto
Automatic Register Balancing : No

----- Target Options

LUT Combining : Auto
Reduce Control Sets : Auto
Add IO Buffers : YES
Global Maximum Fanout : 100000
Add Generic Clock Buffer(BUFG) : 16
Register Duplication : YES
Optimize Instantiated Primitives : NO
Use Clock Enable : Auto
Use Synchronous Set : Auto
Use Synchronous Reset : Auto
Pack IO Registers into IOBs : Auto
Equivalent register Removal : YES

----- General Options

Optimization Goal : Speed
Optimization Effort : 1
Power Reduction : NO
Keep Hierarchy : No
Netlist Hierarchy : As_Optimized
RTL Output : Yes
Global Optimization : AllClockNets
Read Cores : YES
Write Timing Constraints : NO
Cross Clock Analysis : NO
Hierarchy Separator : /
Bus Delimiter : <>
Case Specifier : Maintain
Slice Utilization Ratio : 100
BRAM Utilization Ratio : 100
DSP48 Utilization Ratio : 100
Auto BRAM Packing : NO
Slice Utilization Ratio Delta : 5

=====

=====

* HDL Parsing *

=====

Parsing VHDL file "64200296\unary_op_xor_tree_lut6.vhd" into library work
Parsing entity <XorTreeStage>.
Parsing architecture <tree_of_xor_lut6> of entity <xortreestage>.
Parsing VHDL file "64200296\unary_op_tree.vhd" into library work
Parsing entity <Unary_Op_Bin_Tree>.
Parsing architecture <t> of entity <unary_op_bin_tree>.

```
=====
*          HDL Elaboration          *
=====
```

Elaborating entity <Unary_Op_Bin_Tree> (architecture <t>) with generics from library <work>.

Elaborating entity <XorTreeStage> (architecture <tree_of_xor_lut6>) with generics from library <work>.

Elaborating entity <XorTreeStage> (architecture <tree_of_xor_lut6>) with generics from library <work>.

Elaborating entity <XorTreeStage> (architecture <tree_of_xor_lut6>) with generics from library <work>.

Elaborating entity <XorTreeStage> (architecture <tree_of_xor_lut6>) with generics from library <work>.

Elaborating entity <XorTreeStage> (architecture <tree_of_xor_lut6>) with generics from library <work>.

Elaborating entity <XorTreeStage> (architecture <tree_of_xor_lut6>) with generics from library <work>.

Elaborating entity <XorTreeStage> (architecture <tree_of_xor_lut6>) with generics from library <work>.

Elaborating entity <XorTreeStage> (architecture <tree_of_xor_lut6>) with generics from library <work>.

Elaborating entity <XorTreeStage> (architecture <tree_of_xor_lut6>) with generics from library <work>.

```
=====
*          HDL Synthesis            *
=====
```

Synthesizing Unit <Unary_Op_Bin_Tree>.
Related source file is "64200296\unary_op_tree.vhd".
N = 4096
Summary:
no macro.
Unit <Unary_Op_Bin_Tree> synthesized.

Synthesizing Unit <XorTreeStage_1>.
Related source file is "64200296\unary_op_xor_tree_lut6.vhd".
N = 4096
Summary:
no macro.
Unit <XorTreeStage_1> synthesized.

Synthesizing Unit <XorTreeStage_2>.
Related source file is "64200296\unary_op_xor_tree_lut6.vhd".
N = 682
Summary:
no macro.
Unit <XorTreeStage_2> synthesized.

Synthesizing Unit <XorTreeStage_3>.
Related source file is "64200296\unary_op_xor_tree_lut6.vhd".
N = 113
Summary:
no macro.
Unit <XorTreeStage_3> synthesized.

Synthesizing Unit <XorTreeStage_4>.
Related source file is "64200296\unary_op_xor_tree_lut6.vhd".
N = 18
Summary:
no macro.
Unit <XorTreeStage_4> synthesized.

Synthesizing Unit <XorTreeStage_5>.
Related source file is "64200296\unary_op_xor_tree_lut6.vhd".
N = 3
Summary:
no macro.
Unit <XorTreeStage_5> synthesized.

Synthesizing Unit <XorTreeStage_6>.
Related source file is "64200296\unary_op_xor_tree_lut6.vhd".
N = 19
Summary:
no macro.
Unit <XorTreeStage_6> synthesized.

Synthesizing Unit <XorTreeStage_7>.
Related source file is "64200296\unary_op_xor_tree_lut6.vhd".
N = 4
Summary:
no macro.
Unit <XorTreeStage_7> synthesized.

Synthesizing Unit <XorTreeStage_8>.
Related source file is "64200296\unary_op_xor_tree_lut6.vhd".
N = 114
Summary:
no macro.
Unit <XorTreeStage_8> synthesized.

Synthesizing Unit <XorTreeStage_9>.
Related source file is "64200296\unary_op_xor_tree_lut6.vhd".
N = 683
Summary:
no macro.
Unit <XorTreeStage_9> synthesized.

=====
HDL Synthesis Report

Found no macro

```
=====
*      Advanced HDL Synthesis      *
=====
```

```
=====
Advanced HDL Synthesis Report
=====
```

Found no macro

```
=====
*      Low Level Synthesis      *
=====
```

Optimizing unit <Unary_Op_Bin_Tree> ...

Mapping all equations...

Building and optimizing final netlist ...

Found area constraint ratio of 100 (+ 5) on block Unary_Op_Bin_Tree, actual ratio is 94.

Final Macro Processing ...

```
=====
Final Register Report
=====
```

Found no macro

```
=====
*      Partition Report      *
=====
```

Partition Implementation Status

No Partitions were found in this design.

```
=====
*      Design Summary      *
=====
```

Top Level Output File Name : Unary_Op_Bin_Tree.ngc

Primitive and Black Box Usage:

# BELS	: 1555
# LUT3	: 1088
# LUT4	: 208
# LUT6	: 259
# IO Buffers	: 4097
# IBUF	: 4096
# OBUF	: 1

Device utilization summary:

Selected Device : 6slx4tqg144-3

Slice Logic Utilization:

Number of Slice LUTs: 1555 out of 2400 64%
Number used as Logic: 1555 out of 2400 64%

Slice Logic Distribution:

Number of LUT Flip Flop pairs used: 1555
Number with an unused Flip Flop: 1555 out of 1555 100%
Number with an unused LUT: 0 out of 1555 0%
Number of fully used LUT-FF pairs: 0 out of 1555 0%
Number of unique control sets: 0

IO Utilization:

Number of IOs: 4097
Number of bonded IOBs: 4097 out of 102 4016% (*)

Specific Feature Utilization:

WARNING:Xst:1336 - (*) More than 100% of Device resources are used

Partition Resource Summary:

No Partitions were found in this design.

=====

Timing Report

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.
FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT
GENERATED AFTER PLACE-and-ROUTE.

Clock Information:

No clock signals found in this design

Asynchronous Control Signals Information:

No asynchronous control signals found in this design

Timing Summary:

Speed Grade: -3

Minimum period: No path found
Minimum input arrival time before clock: No path found
Maximum output required time after clock: No path found
Maximum combinational path delay: 10.106ns

Timing Details:

All values displayed in nanoseconds (ns)

```

=====
Timing constraint: Default path analysis
Total number of paths / destination ports: 4096 / 1
-----
Delay: 10.106ns (Levels of Logic = 7)
Source: I<0> (PAD)
Destination: O_Xor (PAD)

Data Path: I<0> to O_Xor
Gate Net
Cell:in->out fanout Delay Delay Logical Name (Net Name)
-----
IBUF:I->O 1 1.222 0.808 I_0_IBUF (I_0_IBUF)
LUT3:I0->O 1 0.339 0.944
U_Xor/Stages.Sixth1_tree/Stages.Sixth1_tree/Stages.Sixth1_tree/Stages.Sixth1_tree/
Stage_xor_3.XOR3_LUT
(U_Xor/Stages.Sixth1_tree/Stages.Sixth1_tree/Stages.Sixth1_tree/Stages.Sixth1)
LUT6:I0->O 1 0.203 0.944
U_Xor/Stages.Sixth1_tree/Stages.Sixth1_tree/Stages.Sixth1_tree/Stages.XOR6_LUT
(U_Xor/Stages.Sixth1_tree/Stages.Sixth1_tree/Stages.Sixth1)
LUT6:I0->O 1 0.203 0.944
U_Xor/Stages.Sixth1_tree/Stages.Sixth1_tree/Stages.XOR6_LUT
(U_Xor/Stages.Sixth1_tree/Stages.Sixth1)
LUT6:I0->O 1 0.203 0.944 U_Xor/Stages.Sixth1_tree/Stages.XOR6_LUT
(U_Xor/Stages.Sixth1)
LUT6:I0->O 1 0.203 0.579 U_Xor/Stages.XOR6_LUT (O_Xor_OBUF)
OBUF:I->O 2.571 O_Xor_OBUF (O_Xor)
-----
Total 10.106ns (4.944ns logic, 5.162ns route)
(48.9% logic, 51.1% route)
=====

```

Cross Clock Domains Report:

```

-----
Total REAL time to Xst completion: 17.00 secs
Total CPU time to Xst completion: 16.72 secs

```

-->

Total memory usage is 4538352 kilobytes

```

Number of errors : 0 ( 0 filtered)
Number of warnings : 1 ( 0 filtered)
Number of infos : 0 ( 0 filtered)

```

```

64200296>fuse -incremental -o unary_tree_tb_isim_beh.exe -prj unary_tree_tb.prj -
top Unary_Op_Bin_Tree_tb
Running: C:\Xilinx\14.7\ISE_DS\ISE\bin\nt64\unwrapped\fuse.exe -incremental -o
unary_tree_tb_isim_beh.exe -prj unary_tree_tb.prj -top Unary_Op_Bin_Tree_tb
ISim P.20131013 (signature 0x7708f090)
Number of CPUs detected in this system: 8
Turning on mult-threading, number of parallel sub-compilation jobs: 16
Determining compilation order of HDL files
Parsing VHDL file "slv_image_pkg.vhd" into library work

```



```

Parsing VHDL file "unary_op_xor_tree_lut6.vhd" into library work
Parsing VHDL file "unary_op_tree.vhd" into library work
Parsing VHDL file "unary_op_tree_IDEAL_tb.vhd" into library work
Starting static elaboration
Completed static elaboration
Compiling package standard
Compiling package std_logic_1164
Compiling package numeric_std
Compiling package textio
Compiling package std_logic_textio
Compiling package slv_image_pkg
Compiling package vcomponents
Compiling package vital_timing
Compiling package vital_primitives
Compiling package vpkg
Compiling architecture tree_of_xor_lut6 of entity XorTreeStage [\XorTreeStage(2)\]
Compiling architecture lut3_v of entity LUT3 [\LUT3("10010110")(0,7)\]
Compiling architecture tree_of_xor_lut6 of entity XorTreeStage [\XorTreeStage(3)\]
Compiling architecture lut6_v of entity LUT6 [\LUT6("0110100110010110100101100...)]
Compiling architecture tree_of_xor_lut6 of entity XorTreeStage
[\XorTreeStage(16)\]
Compiling architecture t of entity Unary_Op_Bin_Tree [\Unary_Op_Bin_Tree(16)\]
Compiling architecture test of entity unary_op_bin_tree_tb
Time Resolution for simulation is 1ps.
Waiting for 1 sub-compilation(s) to finish...
Compiled 23 VHDL Units
Built simulation executable unary_tree_tb_isim_beh.exe
Fuse Memory Usage: 59804 KB
Fuse CPU Usage: 1390 ms

```

```
64200296>if exist Unary_Op_Bin_Tree.csv del Unary_Op_Bin_Tree.csv
```

```
64200296>if exist Unary_Op_Bin_Tree_64200296.csv del
Unary_Op_Bin_Tree_64200296.csv
```

```

64200296>unary_tree_tb_isim_beh.exe -tclbatch isim.tcl -wdb
unary_tree_tb_isim_beh.wdb
ISim P.20131013 (signature 0x7708f090)
WARNING: A WEBPACK license was found.
WARNING: Please use Xilinx License Configuration Manager to check out a full ISim
license.
WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for
more information on the differences between the Lite and the Full version.
This is a Lite version of ISim.
Time resolution is 1 ps
Simulator is doing circuit initialization process.
Finished circuit initialization process.

```

```
64200296>rem ren Unary_Op_Bin_Tree.csv Unary_Op_Bin_Tree_64200296.csv
```

```

64200296>xst -ifn unary_vhdl93.xst
Release 14.7 - xst P.20131013 (nt64)
Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.
--> Parameter TMPDIR set to xst/projnav.tmp

```

```

Total REAL time to Xst completion: 1.00 secs
Total CPU time to Xst completion: 0.31 secs

```

```
--> Parameter xsthdpdir set to xst
```

Total REAL time to Xst completion: 1.00 secs
Total CPU time to Xst completion: 0.31 secs

-->

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 - 8.4.5) Cross Clock Domains Report

```
=====
*      Synthesis Options Summary      *
=====
```

---- Source Parameters

Input File Name : "./unary_vhdl93.prj"
Ignore Synthesis Constraint File : NO

---- Target Parameters

Output File Name : "reduction_operators"
Output Format : NGC
Target Device : xc6slx4-3-tqg144

---- Source Options

Top Module Name : reduction_operators
Automatic FSM Extraction : YES
FSM Encoding Algorithm : Auto
Safe Implementation : No
FSM Style : LUT
RAM Extraction : Yes
RAM Style : Auto
ROM Extraction : Yes
Shift Register Extraction : YES
ROM Style : Auto
Resource Sharing : YES
Asynchronous To Synchronous : NO
Shift Register Minimum Size : 2
Use DSP Block : Auto
Automatic Register Balancing : No

---- Target Options

LUT Combining : Auto
Reduce Control Sets : Auto
Add IO Buffers : YES

Global Maximum Fanout : 100000
Add Generic Clock Buffer(BUFG) : 16
Register Duplication : YES
Optimize Instantiated Primitives : NO
Use Clock Enable : Auto
Use Synchronous Set : Auto
Use Synchronous Reset : Auto
Pack IO Registers into IOBs : Auto
Equivalent register Removal : YES

---- General Options

Optimization Goal : Speed
Optimization Effort : 1
Power Reduction : NO
Keep Hierarchy : No
Netlist Hierarchy : As_Optimized
RTL Output : Yes
Global Optimization : AllClockNets
Read Cores : YES
Write Timing Constraints : NO
Cross Clock Analysis : NO
Hierarchy Separator : /
Bus Delimiter : <>
Case Specifier : Maintain
Slice Utilization Ratio : 100
BRAM Utilization Ratio : 100
DSP48 Utilization Ratio : 100
Auto BRAM Packing : NO
Slice Utilization Ratio Delta : 5

=====

=====

* HDL Parsing *

=====

Parsing VHDL file "64200296\unary_operators_vhdl_93.vhd" into library work
Parsing entity <reduction_operators>.
Parsing architecture <vhdl_93_process> of entity <reduction_operators>.

=====

* HDL Elaboration *

=====

Elaborating entity <reduction_operators> (architecture <vhdl_93_process>) with
generics from library <work>.

=====

* HDL Synthesis *

=====

Synthesizing Unit <reduction_operators>.
Related source file is "64200296\unary_operators_vhdl_93.vhd".
N = 64
Summary:
inferred 128 Multiplexer(s).
Unit <reduction_operators> synthesized.

=====

HDL Synthesis Report

Macro Statistics

Multiplexers : 128
1-bit 2-to-1 multiplexer : 128
Xors : 1
1-bit xor64 : 1

=====

=====

* Advanced HDL Synthesis *

=====

=====

Advanced HDL Synthesis Report

Macro Statistics

Multiplexers : 128
1-bit 2-to-1 multiplexer : 128
Xors : 1
1-bit xor64 : 1

=====

=====

* Low Level Synthesis *

=====

Optimizing unit <reduction_operators> ...

Mapping all equations...

Building and optimizing final netlist ...

Found area constraint ratio of 100 (+ 5) on block reduction_operators, actual ratio is 1.

Final Macro Processing ...

=====

Final Register Report

Found no macro

=====

=====

* Partition Report *

=====

Partition Implementation Status

No Partitions were found in this design.

=====

* Design Summary *

=====

Top Level Output File Name : reduction_operators.ngc

Primitive and Black Box Usage:

```
-----  
# BELS           : 59  
# GND            : 1  
# LUT4           : 3  
# LUT6           : 32  
# MUXCY          : 22  
# VCC            : 1  
# IO Buffers     : 67  
# IBUF           : 64  
# OBUF           : 3
```

Device utilization summary:

Selected Device : 6slx4tqg144-3

Slice Logic Utilization:

Number of Slice LUTs: 35 out of 2400 1%
Number used as Logic: 35 out of 2400 1%

Slice Logic Distribution:

Number of LUT Flip Flop pairs used: 35
Number with an unused Flip Flop: 35 out of 35 100%
Number with an unused LUT: 0 out of 35 0%
Number of fully used LUT-FF pairs: 0 out of 35 0%
Number of unique control sets: 0

IO Utilization:

Number of IOs: 67
Number of bonded IOBs: 67 out of 102 65%

Specific Feature Utilization:

----- Partition Resource Summary:

No Partitions were found in this design.

=====

Timing Report

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.

FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT
GENERATED AFTER PLACE-and-ROUTE.

Clock Information:

No clock signals found in this design

Asynchronous Control Signals Information:

No asynchronous control signals found in this design

Timing Summary:

Speed Grade: -3

Minimum period: No path found
Minimum input arrival time before clock: No path found
Maximum output required time after clock: No path found
Maximum combinational path delay: 7.522ns

Timing Details:

All values displayed in nanoseconds (ns)

=====
Timing constraint: Default path analysis
Total number of paths / destination ports: 192 / 3

Delay: 7.522ns (Levels of Logic = 5)
Source: A<22> (PAD)
Destination: reduced_XOR (PAD)

Data Path: A<22> to reduced_XOR

Gate Net
Cell:in->out fanout Delay Delay Logical Name (Net Name)

IBUF:I->O 3 1.222 1.015 A_22_IBUF (A_22_IBUF)
LUT6:I0->O 1 0.203 0.944 Mxor_reduced_XOR_xo<0>3 (Mxor_reduced_XOR_xo<0>2)
LUT6:I0->O 1 0.203 0.580 Mxor_reduced_XOR_xo<0>14_SW0 (N01)
LUT6:I5->O 1 0.205 0.579 Mxor_reduced_XOR_xo<0>14 (reduced_XOR_OBUF)
OBUF:I->O 2.571 reduced_XOR_OBUF (reduced_XOR)

Total 7.522ns (4.404ns logic, 3.118ns route)
(58.5% logic, 41.5% route)

=====
Cross Clock Domains Report:

=====
Total REAL time to Xst completion: 10.00 secs
Total CPU time to Xst completion: 10.13 secs

-->

Total memory usage is 4487516 kilobytes

Number of errors : 0 (0 filtered)
Number of warnings : 0 (0 filtered)
Number of infos : 0 (0 filtered)

64200296>fuse -incremental -o unary_vhdl93_tb_isim_beh.exe -prj
unary_vhdl93_tb.prj -top reduction_operators_tb
Running: C:\Xilinx\14.7\ISE_DS\ISE\bin\nt64\unwrapped\fuse.exe -incremental -o
unary_vhdl93_tb_isim_beh.exe -prj unary_vhdl93_tb.prj -top reduction_operators_tb
ISim P.20131013 (signature 0x7708f090)
Number of CPUs detected in this system: 8
Turning on mult-threading, number of parallel sub-compilation jobs: 16
Determining compilation order of HDL files

```
Parsing VHDL file "unary_operators_vhdl_93.vhd" into library work
Parsing VHDL file "unary_operators_vhdl93_IDEAL_tb.vhd" into library work
Starting static elaboration
Completed static elaboration
Compiling package standard
Compiling package std_logic_1164
Compiling package numeric_std
Compiling package textio
Compiling package std_logic_textio
Compiling architecture vhdl_93_process of entity reduction_operators
[\\reduction_operators(3)\\]
Compiling architecture test of entity reduction_operators_tb
Time Resolution for simulation is 1ps.
Compiled 8 VHDL Units
Built simulation executable unary_vhdl93_tb_isim_beh.exe
Fuse Memory Usage: 37368 KB
Fuse CPU Usage: 843 ms
```

```
64200296>if exist reduction_operators.csv del reduction_operators.csv
```

```
64200296>if exist reduction_operators_64200296.csv del
reduction_operators_64200296.csv
```

```
64200296>unary_vhdl93_tb_isim_beh.exe -tclbatch isim.tcl -wdb
unary_vhdl93_tb_isim_beh.wdb
ISim P.20131013 (signature 0x7708f090)
WARNING: A WEBPACK license was found.
WARNING: Please use Xilinx License Configuration Manager to check out a full ISim
license.
WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for
more information on the differences between the Lite and the Full version.
This is a Lite version of ISim.
Time resolution is 1 ps
Simulator is doing circuit initialization process.
Finished circuit initialization process.
```

```
64200296>rem ren reduction_operators.csv reduction_operators_64200296.csv
```

```
-- *****
-- **** STUDENT: 64200385
-- *****
-- KOMENTARJI K OCENI NALOGE
-- Matej Možek: Ni pripomb
-- *****
```

```
64200385>if not exist "xst" mkdir xst
```

```
64200385>cd XST
```

```
64200385\xst>if not exist "projnav.tmp" mkdir "projnav.tmp"
```

```
64200385\xst>cd ..
```

```
64200385>xst -ifn unary_tree.xst
Release 14.7 - xst P.20131013 (nt64)
Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.
--> Parameter TMPDIR set to xst/projnav.tmp
```

```
Total REAL time to Xst completion: 0.00 secs
```

```
Total CPU time to Xst completion: 0.24 secs
```

```
--> Parameter xsthdpdir set to xst
```

```
Total REAL time to Xst completion: 0.00 secs
```

```
Total CPU time to Xst completion: 0.24 secs
```

```
-->
```

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```
=====
*      Synthesis Options Summary      *
=====
```

---- Source Parameters

```
Input File Name      : "unary_tree.prj"
Ignore Synthesis Constraint File : NO
```

---- Target Parameters

```
Output File Name     : "Unary_Op_Bin_Tree"
```


Output Format : NGC
Target Device : xc6slx4-3-tqg144

----- Source Options

Top Module Name : Unary_Op_Bin_Tree
Automatic FSM Extraction : YES
FSM Encoding Algorithm : Auto
Safe Implementation : No
FSM Style : LUT
RAM Extraction : Yes
RAM Style : Auto
ROM Extraction : Yes
Shift Register Extraction : YES
ROM Style : Auto
Resource Sharing : YES
Asynchronous To Synchronous : NO
Shift Register Minimum Size : 2
Use DSP Block : Auto
Automatic Register Balancing : No

----- Target Options

LUT Combining : Auto
Reduce Control Sets : Auto
Add IO Buffers : YES
Global Maximum Fanout : 100000
Add Generic Clock Buffer(BUFG) : 16
Register Duplication : YES
Optimize Instantiated Primitives : NO
Use Clock Enable : Auto
Use Synchronous Set : Auto
Use Synchronous Reset : Auto
Pack IO Registers into IOBs : Auto
Equivalent register Removal : YES

----- General Options

Optimization Goal : Speed
Optimization Effort : 1
Power Reduction : NO
Keep Hierarchy : No
Netlist Hierarchy : As_Optimized
RTL Output : Yes
Global Optimization : AllClockNets
Read Cores : YES
Write Timing Constraints : NO
Cross Clock Analysis : NO
Hierarchy Separator : /
Bus Delimiter : <>
Case Specifier : Maintain
Slice Utilization Ratio : 100
BRAM Utilization Ratio : 100
DSP48 Utilization Ratio : 100
Auto BRAM Packing : NO
Slice Utilization Ratio Delta : 5

=====

=====

* HDL Parsing *

=====

Parsing VHDL file "64200385\unary_op_xor_tree_lut6.vhd" into library work
Parsing entity <XorTreeStage>.
Parsing architecture <tree_of_xor_lut6> of entity <xortreestage>.
Parsing VHDL file "64200385\unary_op_tree.vhd" into library work
Parsing entity <Unary_Op_Bin_Tree>.
Parsing architecture <t> of entity <unary_op_bin_tree>.

```
=====
*          HDL Elaboration          *
=====
```

Elaborating entity <Unary_Op_Bin_Tree> (architecture <t>) with generics from library <work>.

Elaborating entity <XorTreeStage> (architecture <tree_of_xor_lut6>) with generics from library <work>.

Elaborating entity <XorTreeStage> (architecture <tree_of_xor_lut6>) with generics from library <work>.

Elaborating entity <XorTreeStage> (architecture <tree_of_xor_lut6>) with generics from library <work>.

Elaborating entity <XorTreeStage> (architecture <tree_of_xor_lut6>) with generics from library <work>.

Elaborating entity <XorTreeStage> (architecture <tree_of_xor_lut6>) with generics from library <work>.

Elaborating entity <XorTreeStage> (architecture <tree_of_xor_lut6>) with generics from library <work>.

Elaborating entity <XorTreeStage> (architecture <tree_of_xor_lut6>) with generics from library <work>.

Elaborating entity <XorTreeStage> (architecture <tree_of_xor_lut6>) with generics from library <work>.

Elaborating entity <XorTreeStage> (architecture <tree_of_xor_lut6>) with generics from library <work>.

```
=====
*          HDL Synthesis            *
=====
```

Synthesizing Unit <Unary_Op_Bin_Tree>.
Related source file is "64200385\unary_op_tree.vhd".
N = 4096
Summary:
no macro.
Unit <Unary_Op_Bin_Tree> synthesized.

Synthesizing Unit <XorTreeStage_1>.
Related source file is "64200385\unary_op_xor_tree_lut6.vhd".
N = 4096
Summary:
no macro.
Unit <XorTreeStage_1> synthesized.

Synthesizing Unit <XorTreeStage_2>.
Related source file is "64200385\unary_op_xor_tree_lut6.vhd".
N = 682
Summary:
no macro.
Unit <XorTreeStage_2> synthesized.

Synthesizing Unit <XorTreeStage_3>.
Related source file is "64200385\unary_op_xor_tree_lut6.vhd".
N = 113
Summary:
no macro.
Unit <XorTreeStage_3> synthesized.

Synthesizing Unit <XorTreeStage_4>.
Related source file is "64200385\unary_op_xor_tree_lut6.vhd".
N = 18
Summary:
no macro.
Unit <XorTreeStage_4> synthesized.

Synthesizing Unit <XorTreeStage_5>.
Related source file is "64200385\unary_op_xor_tree_lut6.vhd".
N = 3
Summary:
no macro.
Unit <XorTreeStage_5> synthesized.

Synthesizing Unit <XorTreeStage_6>.
Related source file is "64200385\unary_op_xor_tree_lut6.vhd".
N = 19
Summary:
no macro.
Unit <XorTreeStage_6> synthesized.

Synthesizing Unit <XorTreeStage_7>.
Related source file is "64200385\unary_op_xor_tree_lut6.vhd".
N = 4
Summary:
no macro.
Unit <XorTreeStage_7> synthesized.

Synthesizing Unit <XorTreeStage_8>.
Related source file is "64200385\unary_op_xor_tree_lut6.vhd".
N = 114
Summary:
no macro.
Unit <XorTreeStage_8> synthesized.

Synthesizing Unit <XorTreeStage_9>.
Related source file is "64200385\unary_op_xor_tree_lut6.vhd".
N = 683
Summary:
no macro.
Unit <XorTreeStage_9> synthesized.

=====
HDL Synthesis Report

Found no macro

```
=====
*      Advanced HDL Synthesis      *
=====
```

```
=====
Advanced HDL Synthesis Report
=====
```

Found no macro

```
=====
*      Low Level Synthesis      *
=====
```

Optimizing unit <Unary_Op_Bin_Tree> ...

Mapping all equations...

Building and optimizing final netlist ...

Found area constraint ratio of 100 (+ 5) on block Unary_Op_Bin_Tree, actual ratio is 94.

Final Macro Processing ...

```
=====
Final Register Report
=====
```

Found no macro

```
=====
*      Partition Report      *
=====
```

Partition Implementation Status

No Partitions were found in this design.

```
=====
*      Design Summary      *
=====
```

Top Level Output File Name : Unary_Op_Bin_Tree.ngc

Primitive and Black Box Usage:

# BELS	: 1555
# LUT3	: 1088
# LUT4	: 208
# LUT6	: 259
# IO Buffers	: 4097
# IBUF	: 4096
# OBUF	: 1

Device utilization summary:

Selected Device : 6slx4tqg144-3

Slice Logic Utilization:

Number of Slice LUTs: 1555 out of 2400 64%
Number used as Logic: 1555 out of 2400 64%

Slice Logic Distribution:

Number of LUT Flip Flop pairs used: 1555
Number with an unused Flip Flop: 1555 out of 1555 100%
Number with an unused LUT: 0 out of 1555 0%
Number of fully used LUT-FF pairs: 0 out of 1555 0%
Number of unique control sets: 0

IO Utilization:

Number of IOs: 4097
Number of bonded IOBs: 4097 out of 102 4016% (*)

Specific Feature Utilization:

WARNING:Xst:1336 - (*) More than 100% of Device resources are used

Partition Resource Summary:

No Partitions were found in this design.

=====

Timing Report

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.
FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT
GENERATED AFTER PLACE-and-ROUTE.

Clock Information:

No clock signals found in this design

Asynchronous Control Signals Information:

No asynchronous control signals found in this design

Timing Summary:

Speed Grade: -3

Minimum period: No path found
Minimum input arrival time before clock: No path found
Maximum output required time after clock: No path found
Maximum combinational path delay: 10.106ns

Timing Details:

All values displayed in nanoseconds (ns)

```

=====
Timing constraint: Default path analysis
Total number of paths / destination ports: 4096 / 1
-----
Delay: 10.106ns (Levels of Logic = 7)
Source: I<0> (PAD)
Destination: O_Xor (PAD)

Data Path: I<0> to O_Xor
Gate Net
Cell:in->out fanout Delay Delay Logical Name (Net Name)
-----
IBUF:I->O 1 1.222 0.808 I_0_IBUF (I_0_IBUF)
LUT3:I0->O 1 0.339 0.944
U_Xor/Stages.XTree1/Stages.XTree1/Stages.XTree1/Stages.XTree1/Stage_xor_3.XOR3_LUT
(U_Xor/Stages.XTree1/Stages.XTree1/Stages.XTree1/Stages.Sixth1_0)
LUT6:I0->O 1 0.203 0.944
U_Xor/Stages.XTree1/Stages.XTree1/Stages.XOR6_LUT
(U_Xor/Stages.XTree1/Stages.XTree1/Stages.Sixth1_0)
LUT6:I0->O 1 0.203 0.944 U_Xor/Stages.XTree1/Stages.XTree1/Stages.XOR6_LUT
(U_Xor/Stages.XTree1/Stages.Sixth1_0)
LUT6:I0->O 1 0.203 0.944 U_Xor/Stages.XTree1/Stages.XOR6_LUT
(U_Xor/Stages.Sixth1_0)
LUT6:I0->O 1 0.203 0.579 U_Xor/Stages.XOR6_LUT (O_Xor_OBUF)
OBUF:I->O 2.571 O_Xor_OBUF (O_Xor)
-----
Total 10.106ns (4.944ns logic, 5.162ns route)
(48.9% logic, 51.1% route)
=====

```

Cross Clock Domains Report:

```

=====
Total REAL time to Xst completion: 17.00 secs
Total CPU time to Xst completion: 17.37 secs

```

-->

Total memory usage is 4538336 kilobytes

```

Number of errors : 0 ( 0 filtered)
Number of warnings : 1 ( 0 filtered)
Number of infos : 0 ( 0 filtered)

```

```

64200385>fuse -incremental -o unary_tree_tb_isim_beh.exe -prj unary_tree_tb.prj -
top Unary_Op_Bin_Tree_tb
Running: C:\Xilinx\14.7\ISE_DS\ISE\bin\nt64\unwrapped\fuse.exe -incremental -o
unary_tree_tb_isim_beh.exe -prj unary_tree_tb.prj -top Unary_Op_Bin_Tree_tb
ISim P.20131013 (signature 0x7708f090)
Number of CPUs detected in this system: 8
Turning on mult-threading, number of parallel sub-compilation jobs: 16
Determining compilation order of HDL files
Parsing VHDL file "slv_image_pkg.vhd" into library work
Parsing VHDL file "unary_op_xor_tree_lut6.vhd" into library work
Parsing VHDL file "unary_op_tree.vhd" into library work

```

```

Parsing VHDL file "unary_op_tree_IDEAL_tb.vhd" into library work
Starting static elaboration
Completed static elaboration
Compiling package standard
Compiling package std_logic_1164
Compiling package numeric_std
Compiling package textio
Compiling package std_logic_textio
Compiling package slv_image_pkg
Compiling package vcomponents
Compiling package vital_timing
Compiling package vital_primitives
Compiling package vpkg
Compiling architecture tree_of_xor_lut6 of entity XorTreeStage [\XorTreeStage(2)\]
Compiling architecture lut3_v of entity LUT3 [\LUT3("10010110")(0,7)\]
Compiling architecture tree_of_xor_lut6 of entity XorTreeStage [\XorTreeStage(3)\]
Compiling architecture lut6_v of entity LUT6 [\LUT6("0110100110010110100101100...)]
Compiling architecture tree_of_xor_lut6 of entity XorTreeStage
[\XorTreeStage(16)\]
Compiling architecture t of entity Unary_Op_Bin_Tree [\Unary_Op_Bin_Tree(16)\]
Compiling architecture test of entity unary_op_bin_tree_tb
Time Resolution for simulation is 1ps.
Waiting for 1 sub-compilation(s) to finish...
Compiled 23 VHDL Units
Built simulation executable unary_tree_tb_isim_beh.exe
Fuse Memory Usage: 60084 KB
Fuse CPU Usage: 1374 ms

```

```
64200385>if exist Unary_Op_Bin_Tree.csv del Unary_Op_Bin_Tree.csv
```

```
64200385>if exist Unary_Op_Bin_Tree_64200385.csv del
Unary_Op_Bin_Tree_64200385.csv
```

```

64200385>unary_tree_tb_isim_beh.exe -tclbatch isim.tcl -wdb
unary_tree_tb_isim_beh.wdb
ISim P.20131013 (signature 0x7708f090)
WARNING: A WEBPACK license was found.
WARNING: Please use Xilinx License Configuration Manager to check out a full ISim
license.
WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for
more information on the differences between the Lite and the Full version.
This is a Lite version of ISim.
Time resolution is 1 ps
Simulator is doing circuit initialization process.
Finished circuit initialization process.

```

```
64200385>rem ren Unary_Op_Bin_Tree.csv Unary_Op_Bin_Tree_64200385.csv
```

```

64200385>xst -ifn unary_vhdl93.xst
Release 14.7 - xst P.20131013 (nt64)
Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.
--> Parameter TMPDIR set to xst/projnav.tmp

```

```

Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.24 secs

```

```
--> Parameter xsthdpdir set to xst
```

```
Total REAL time to Xst completion: 0.00 secs
```

Total CPU time to Xst completion: 0.24 secs

-->

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```
=====
*      Synthesis Options Summary      *
=====
```

---- Source Parameters

Input File Name : "./unary_vhd193.prj"
Ignore Synthesis Constraint File : NO

---- Target Parameters

Output File Name : "reduction_operators"
Output Format : NGC
Target Device : xc6slx4-3-tqg144

---- Source Options

Top Module Name : reduction_operators
Automatic FSM Extraction : YES
FSM Encoding Algorithm : Auto
Safe Implementation : No
FSM Style : LUT
RAM Extraction : Yes
RAM Style : Auto
ROM Extraction : Yes
Shift Register Extraction : YES
ROM Style : Auto
Resource Sharing : YES
Asynchronous To Synchronous : NO
Shift Register Minimum Size : 2
Use DSP Block : Auto
Automatic Register Balancing : No

---- Target Options

LUT Combining : Auto
Reduce Control Sets : Auto
Add IO Buffers : YES
Global Maximum Fanout : 100000
Add Generic Clock Buffer(BUFG) : 16

Register Duplication : YES
Optimize Instantiated Primitives : NO
Use Clock Enable : Auto
Use Synchronous Set : Auto
Use Synchronous Reset : Auto
Pack IO Registers into IOBs : Auto
Equivalent register Removal : YES

---- General Options

Optimization Goal : Speed
Optimization Effort : 1
Power Reduction : NO
Keep Hierarchy : No
Netlist Hierarchy : As_Optimized
RTL Output : Yes
Global Optimization : AllClockNets
Read Cores : YES
Write Timing Constraints : NO
Cross Clock Analysis : NO
Hierarchy Separator : /
Bus Delimiter : <>
Case Specifier : Maintain
Slice Utilization Ratio : 100
BRAM Utilization Ratio : 100
DSP48 Utilization Ratio : 100
Auto BRAM Packing : NO
Slice Utilization Ratio Delta : 5

=====

=====

* HDL Parsing *

=====

Parsing VHDL file "64200385\unary_operators_vhdl_93.vhd" into library work
Parsing entity <reduction_operators>.
Parsing architecture <vhdl_93_process> of entity <reduction_operators>.

=====

* HDL Elaboration *

=====

Elaborating entity <reduction_operators> (architecture <vhdl_93_process>) with
generics from library <work>.

=====

* HDL Synthesis *

=====

Synthesizing Unit <reduction_operators>.
Related source file is "64200385\unary_operators_vhdl_93.vhd".
N = 10
Summary:
inferred 20 Multiplexer(s).
Unit <reduction_operators> synthesized.

=====

HDL Synthesis Report

Macro Statistics

```
# Multiplexers          : 20
 1-bit 2-to-1 multiplexer : 20
# Xors                  : 1
 1-bit xor10           : 1
```

=====

=====

```
*      Advanced HDL Synthesis      *
```

=====

=====

Advanced HDL Synthesis Report

Macro Statistics

```
# Multiplexers          : 20
 1-bit 2-to-1 multiplexer : 20
# Xors                  : 1
 1-bit xor10           : 1
```

=====

=====

```
*      Low Level Synthesis      *
```

=====

Optimizing unit <reduction_operators> ...

Mapping all equations...

Building and optimizing final netlist ...

Found area constraint ratio of 100 (+ 5) on block reduction_operators, actual ratio is 0.

Final Macro Processing ...

=====

Final Register Report

Found no macro

=====

=====

```
*      Partition Report      *
```

=====

Partition Implementation Status

No Partitions were found in this design.

=====

```
*      Design Summary      *
```

=====

Top Level Output File Name : reduction_operators.ngc

Primitive and Black Box Usage:

```
-----
# BELS      : 6
# LUT5      : 3
# LUT6      : 3
# IO Buffers : 13
# IBUF      : 10
# OBUF      : 3
```

Device utilization summary:

```
-----
Selected Device : 6slx4tqg144-3
```

Slice Logic Utilization:

```
Number of Slice LUTs:    6 out of 2400  0%
Number used as Logic:    6 out of 2400  0%
```

Slice Logic Distribution:

```
Number of LUT Flip Flop pairs used:  6
Number with an unused Flip Flop:  6 out of 6 100%
Number with an unused LUT:          0 out of 6  0%
Number of fully used LUT-FF pairs:  0 out of 6  0%
Number of unique control sets:      0
```

IO Utilization:

```
Number of IOs:          13
Number of bonded IOBs:   13 out of 102 12%
```

Specific Feature Utilization:

```
-----
Partition Resource Summary:
-----
```

No Partitions were found in this design.

```
=====
Timing Report
```

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.
FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT
GENERATED AFTER PLACE-and-ROUTE.

Clock Information:

```
-----
No clock signals found in this design
```

Asynchronous Control Signals Information:

```
-----
No asynchronous control signals found in this design
```

Timing Summary:

```
-----
Speed Grade: -3
```

Minimum period: No path found
Minimum input arrival time before clock: No path found

Maximum output required time after clock: No path found
Maximum combinational path delay: 6.355ns

Timing Details:

All values displayed in nanoseconds (ns)

Timing constraint: Default path analysis

Total number of paths / destination ports: 30 / 3

Delay: 6.355ns (Levels of Logic = 4)

Source: A<4> (PAD)

Destination: reduced_OR (PAD)

Data Path: A<4> to reduced_OR

Gate Net

Cell:in->out fanout Delay Delay Logical Name (Net Name)

IBUF:I->O 3 1.222 0.995 A_4_IBUF (A_4_IBUF)

LUT5:I0->O 1 0.203 0.580 Mxor_reduced_XOR_xo<0>_SW0 (N01)

LUT6:I5->O 1 0.205 0.579 Mxor_reduced_XOR_xo<0> (reduced_XOR_OBUF)

OBUF:I->O 2.571 reduced_XOR_OBUF (reduced_XOR)

Total 6.355ns (4.201ns logic, 2.154ns route)
(66.1% logic, 33.9% route)

Cross Clock Domains Report:

Total REAL time to Xst completion: 9.00 secs

Total CPU time to Xst completion: 9.08 secs

-->

Total memory usage is 4487516 kilobytes

Number of errors : 0 (0 filtered)

Number of warnings : 0 (0 filtered)

Number of infos : 0 (0 filtered)

64200385>fuse -incremental -o unary_vhdl93_tb_isim_beh.exe -prj

unary_vhdl93_tb.prj -top reduction_operators_tb

Running: C:\Xilinx\14.7\ISE_DS\ISE\bin\nt64\unwrapped\fuse.exe -incremental -o
unary_vhdl93_tb_isim_beh.exe -prj unary_vhdl93_tb.prj -top reduction_operators_tb
ISim P.20131013 (signature 0x7708f090)

Number of CPUs detected in this system: 8

Turning on mult-threading, number of parallel sub-compilation jobs: 16

Determining compilation order of HDL files

Parsing VHDL file "unary_operators_vhdl_93.vhd" into library work

Parsing VHDL file "unary_operators_vhdl93_IDEAL_tb.vhd" into library work

Starting static elaboration

Completed static elaboration

Compiling package standard

Compiling package std_logic_1164

```
Compiling package numeric_std
Compiling package textio
Compiling package std_logic_textio
Compiling architecture vhd1_93_process of entity reduction_operators
[\reduction_operators(3)\]
Compiling architecture test of entity reduction_operators_tb
Time Resolution for simulation is 1ps.
Compiled 8 VHDL Units
Built simulation executable unary_vhdl93_tb_isim_beh.exe
Fuse Memory Usage: 36820 KB
Fuse CPU Usage: 811 ms
```

```
64200385>if exist reduction_operators.csv del reduction_operators.csv
```

```
64200385>if exist reduction_operators_64200385.csv del
reduction_operators_64200385.csv
```

```
64200385>unary_vhdl93_tb_isim_beh.exe -tclbatch isim.tcl -wdb
unary_vhdl93_tb_isim_beh.wdb
ISim P.20131013 (signature 0x7708f090)
WARNING: A WEBPACK license was found.
WARNING: Please use Xilinx License Configuration Manager to check out a full ISim
license.
WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for
more information on the differences between the Lite and the Full version.
This is a Lite version of ISim.
Time resolution is 1 ps
Simulator is doing circuit initialization process.
Finished circuit initialization process.
```

```
64200385>ren reduction_operators.csv reduction_operators_64200385.csv
```

```
-- *****
-- **** STUDENT: 64210132
-- *****
-- KOMENTARJI K OCENI NALOGE
-- Matej Možek: Ni pripomb
-- *****
```

```
64210132>if not exist "xst" mkdir xst
```

```
64210132>cd XST
```

```
64210132\xst>if not exist "projnav.tmp" mkdir "projnav.tmp"
```

```
64210132\xst>cd ..
```

```
64210132>xst -ifn unary_tree.xst
Release 14.7 - xst P.20131013 (nt64)
Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.
--> Parameter TMPDIR set to xst/projnav.tmp
```

```
Total REAL time to Xst completion: 0.00 secs
```

```
Total CPU time to Xst completion: 0.24 secs
```

```
--> Parameter xsthdpdir set to xst
```

```
Total REAL time to Xst completion: 0.00 secs
```

```
Total CPU time to Xst completion: 0.24 secs
```

```
-->
```

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```
=====
*      Synthesis Options Summary      *
```

----- Source Parameters

```
Input File Name      : "unary_tree.prj"
Ignore Synthesis Constraint File : NO
```

----- Target Parameters

```
Output File Name     : "Unary_Op_Bin_Tree"
```

Output Format : NGC
Target Device : xc6slx4-3-tqg144

----- Source Options

Top Module Name : Unary_Op_Bin_Tree
Automatic FSM Extraction : YES
FSM Encoding Algorithm : Auto
Safe Implementation : No
FSM Style : LUT
RAM Extraction : Yes
RAM Style : Auto
ROM Extraction : Yes
Shift Register Extraction : YES
ROM Style : Auto
Resource Sharing : YES
Asynchronous To Synchronous : NO
Shift Register Minimum Size : 2
Use DSP Block : Auto
Automatic Register Balancing : No

----- Target Options

LUT Combining : Auto
Reduce Control Sets : Auto
Add IO Buffers : YES
Global Maximum Fanout : 100000
Add Generic Clock Buffer(BUFG) : 16
Register Duplication : YES
Optimize Instantiated Primitives : NO
Use Clock Enable : Auto
Use Synchronous Set : Auto
Use Synchronous Reset : Auto
Pack IO Registers into IOBs : Auto
Equivalent register Removal : YES

----- General Options

Optimization Goal : Speed
Optimization Effort : 1
Power Reduction : NO
Keep Hierarchy : No
Netlist Hierarchy : As_Optimized
RTL Output : Yes
Global Optimization : AllClockNets
Read Cores : YES
Write Timing Constraints : NO
Cross Clock Analysis : NO
Hierarchy Separator : /
Bus Delimiter : <>
Case Specifier : Maintain
Slice Utilization Ratio : 100
BRAM Utilization Ratio : 100
DSP48 Utilization Ratio : 100
Auto BRAM Packing : NO
Slice Utilization Ratio Delta : 5

=====

=====

* HDL Parsing *

=====

Parsing VHDL file "64210132\unary_op_xor_tree_lut6.vhd" into library work
Parsing entity <XorTreeStage>.
Parsing architecture <tree_of_xor_lut6> of entity <xortreestage>.
Parsing VHDL file "64210132\unary_op_tree.vhd" into library work
Parsing entity <Unary_Op_Bin_Tree>.
Parsing architecture <t> of entity <unary_op_bin_tree>.

```
=====
*          HDL Elaboration          *
=====
```

Elaborating entity <Unary_Op_Bin_Tree> (architecture <t>) with generics from library <work>.

Elaborating entity <XorTreeStage> (architecture <tree_of_xor_lut6>) with generics from library <work>.

Elaborating entity <XorTreeStage> (architecture <tree_of_xor_lut6>) with generics from library <work>.

Elaborating entity <XorTreeStage> (architecture <tree_of_xor_lut6>) with generics from library <work>.

Elaborating entity <XorTreeStage> (architecture <tree_of_xor_lut6>) with generics from library <work>.

Elaborating entity <XorTreeStage> (architecture <tree_of_xor_lut6>) with generics from library <work>.

Elaborating entity <XorTreeStage> (architecture <tree_of_xor_lut6>) with generics from library <work>.

Elaborating entity <XorTreeStage> (architecture <tree_of_xor_lut6>) with generics from library <work>.

Elaborating entity <XorTreeStage> (architecture <tree_of_xor_lut6>) with generics from library <work>.

Elaborating entity <XorTreeStage> (architecture <tree_of_xor_lut6>) with generics from library <work>.

```
=====
*          HDL Synthesis            *
=====
```

Synthesizing Unit <Unary_Op_Bin_Tree>.
Related source file is "64210132\unary_op_tree.vhd".
N = 4096
Summary:
no macro.
Unit <Unary_Op_Bin_Tree> synthesized.

Synthesizing Unit <XorTreeStage_1>.
Related source file is "64210132\unary_op_xor_tree_lut6.vhd".
N = 4096
Summary:
no macro.
Unit <XorTreeStage_1> synthesized.

Synthesizing Unit <XorTreeStage_2>.
Related source file is "64210132\unary_op_xor_tree_lut6.vhd".
N = 682
Summary:
no macro.
Unit <XorTreeStage_2> synthesized.

Synthesizing Unit <XorTreeStage_3>.
Related source file is "64210132\unary_op_xor_tree_lut6.vhd".
N = 113
Summary:
no macro.
Unit <XorTreeStage_3> synthesized.

Synthesizing Unit <XorTreeStage_4>.
Related source file is "64210132\unary_op_xor_tree_lut6.vhd".
N = 18
Summary:
no macro.
Unit <XorTreeStage_4> synthesized.

Synthesizing Unit <XorTreeStage_5>.
Related source file is "64210132\unary_op_xor_tree_lut6.vhd".
N = 3
Summary:
no macro.
Unit <XorTreeStage_5> synthesized.

Synthesizing Unit <XorTreeStage_6>.
Related source file is "64210132\unary_op_xor_tree_lut6.vhd".
N = 19
Summary:
no macro.
Unit <XorTreeStage_6> synthesized.

Synthesizing Unit <XorTreeStage_7>.
Related source file is "64210132\unary_op_xor_tree_lut6.vhd".
N = 4
Summary:
no macro.
Unit <XorTreeStage_7> synthesized.

Synthesizing Unit <XorTreeStage_8>.
Related source file is "64210132\unary_op_xor_tree_lut6.vhd".
N = 114
Summary:
no macro.
Unit <XorTreeStage_8> synthesized.

Synthesizing Unit <XorTreeStage_9>.
Related source file is "64210132\unary_op_xor_tree_lut6.vhd".
N = 683
Summary:
no macro.
Unit <XorTreeStage_9> synthesized.

=====
HDL Synthesis Report

Found no macro

```
=====
*      Advanced HDL Synthesis      *
=====
```

```
=====
Advanced HDL Synthesis Report
=====
```

Found no macro

```
=====
*      Low Level Synthesis      *
=====
```

Optimizing unit <Unary_Op_Bin_Tree> ...

Mapping all equations...

Building and optimizing final netlist ...

Found area constraint ratio of 100 (+ 5) on block Unary_Op_Bin_Tree, actual ratio is 94.

Final Macro Processing ...

```
=====
Final Register Report
=====
```

Found no macro

```
=====
*      Partition Report      *
=====
```

Partition Implementation Status

No Partitions were found in this design.

```
=====
*      Design Summary      *
=====
```

Top Level Output File Name : Unary_Op_Bin_Tree.ngc

Primitive and Black Box Usage:

# BELS	: 1555
# LUT3	: 1088
# LUT4	: 208
# LUT6	: 259
# IO Buffers	: 4097
# IBUF	: 4096
# OBUF	: 1

Device utilization summary:

Selected Device : 6slx4tqg144-3

Slice Logic Utilization:

Number of Slice LUTs: 1555 out of 2400 64%
Number used as Logic: 1555 out of 2400 64%

Slice Logic Distribution:

Number of LUT Flip Flop pairs used: 1555
Number with an unused Flip Flop: 1555 out of 1555 100%
Number with an unused LUT: 0 out of 1555 0%
Number of fully used LUT-FF pairs: 0 out of 1555 0%
Number of unique control sets: 0

IO Utilization:

Number of IOs: 4097
Number of bonded IOBs: 4097 out of 102 4016% (*)

Specific Feature Utilization:

WARNING:Xst:1336 - (*) More than 100% of Device resources are used

Partition Resource Summary:

No Partitions were found in this design.

=====

Timing Report

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.
FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT
GENERATED AFTER PLACE-and-ROUTE.

Clock Information:

No clock signals found in this design

Asynchronous Control Signals Information:

No asynchronous control signals found in this design

Timing Summary:

Speed Grade: -3

Minimum period: No path found
Minimum input arrival time before clock: No path found
Maximum output required time after clock: No path found
Maximum combinational path delay: 10.106ns

Timing Details:

All values displayed in nanoseconds (ns)

```

=====
Timing constraint: Default path analysis
Total number of paths / destination ports: 4096 / 1
-----
Delay: 10.106ns (Levels of Logic = 7)
Source: I<0> (PAD)
Destination: O_Xor (PAD)

Data Path: I<0> to O_Xor
Gate Net
Cell:in->out fanout Delay Delay Logical Name (Net Name)
-----
IBUF:I->O 1 1.222 0.808 I_0_IBUF (I_0_IBUF)
LUT3:I0->O 1 0.339 0.944
U_Xor/Stages.Sixth1_Tree/Stages.Sixth1_Tree/Stages.Sixth1_Tree/Stages.Sixth1_Tree/
Stage_xor_3.LUT3_inst
(U_Xor/Stages.Sixth1_Tree/Stages.Sixth1_Tree/Stages.Sixth1_Tree/Stages.Sixth1_Xor)
LUT6:I0->O 1 0.203 0.944
U_Xor/Stages.Sixth1_Tree/Stages.Sixth1_Tree/Stages.Sixth1_Tree/Stages.LUT6_inst
(U_Xor/Stages.Sixth1_Tree/Stages.Sixth1_Tree/Stages.Sixth1_Xor)
LUT6:I0->O 1 0.203 0.944
U_Xor/Stages.Sixth1_Tree/Stages.Sixth1_Tree/Stages.LUT6_inst
(U_Xor/Stages.Sixth1_Tree/Stages.Sixth1_Xor)
LUT6:I0->O 1 0.203 0.944 U_Xor/Stages.Sixth1_Tree/Stages.LUT6_inst
(U_Xor/Stages.Sixth1_Xor)
LUT6:I0->O 1 0.203 0.579 U_Xor/Stages.LUT6_inst (O_Xor_OBUF)
OBUF:I->O 2.571 O_Xor_OBUF (O_Xor)
-----
Total 10.106ns (4.944ns logic, 5.162ns route)
(48.9% logic, 51.1% route)
=====

```

Cross Clock Domains Report:

```

-----
Total REAL time to Xst completion: 18.00 secs
Total CPU time to Xst completion: 17.88 secs

```

-->

Total memory usage is 4538404 kilobytes

```

Number of errors : 0 ( 0 filtered)
Number of warnings : 1 ( 0 filtered)
Number of infos : 0 ( 0 filtered)

```

```

64210132>fuse -incremental -o unary_tree_tb_isim_beh.exe -prj unary_tree_tb.prj -
top Unary_Op_Bin_Tree_tb
Running: C:\Xilinx\14.7\ISE_DS\ISE\bin\nt64\unwrapped\fuse.exe -incremental -o
unary_tree_tb_isim_beh.exe -prj unary_tree_tb.prj -top Unary_Op_Bin_Tree_tb
ISim P.20131013 (signature 0x7708f090)
Number of CPUs detected in this system: 8
Turning on mult-threading, number of parallel sub-compilation jobs: 16
Determining compilation order of HDL files
Parsing VHDL file "slv_image_pkg.vhd" into library work

```

```
Parsing VHDL file "unary_op_xor_tree_lut6.vhd" into library work
Parsing VHDL file "unary_op_tree.vhd" into library work
Parsing VHDL file "unary_op_tree_IDEAL_tb.vhd" into library work
Starting static elaboration
Completed static elaboration
Compiling package standard
Compiling package std_logic_1164
Compiling package numeric_std
Compiling package textio
Compiling package std_logic_textio
Compiling package slv_image_pkg
Compiling package vcomponents
Compiling package vital_timing
Compiling package vital_primitives
Compiling package vpkg
Compiling architecture tree_of_xor_lut6 of entity XorTreeStage [\XorTreeStage(2)\]
Compiling architecture lut3_v of entity LUT3 [\LUT3("01101001")(0,7)\]
Compiling architecture tree_of_xor_lut6 of entity XorTreeStage [\XorTreeStage(3)\]
Compiling architecture lut6_v of entity LUT6 [\LUT6("0110100110010110100101100...)]
Compiling architecture tree_of_xor_lut6 of entity XorTreeStage
[\XorTreeStage(16)\]
Compiling architecture t of entity Unary_Op_Bin_Tree [\Unary_Op_Bin_Tree(16)\]
Compiling architecture test of entity unary_op_bin_tree_tb
Time Resolution for simulation is 1ps.
Waiting for 1 sub-compilation(s) to finish...
Compiled 23 VHDL Units
Built simulation executable unary_tree_tb_isim_beh.exe
Fuse Memory Usage: 59328 KB
Fuse CPU Usage: 1296 ms
```

```
64210132>if exist Unary_Op_Bin_Tree.csv del Unary_Op_Bin_Tree.csv
```

```
64210132>if exist Unary_Op_Bin_Tree_64210132.csv del
Unary_Op_Bin_Tree_64210132.csv
```

```
64210132>unary_tree_tb_isim_beh.exe -tclbatch isim.tcl -wdb
unary_tree_tb_isim_beh.wdb
ISim P.20131013 (signature 0x7708f090)
WARNING: A WEBPACK license was found.
WARNING: Please use Xilinx License Configuration Manager to check out a full ISim
license.
WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for
more information on the differences between the Lite and the Full version.
This is a Lite version of ISim.
Time resolution is 1 ps
Simulator is doing circuit initialization process.
Finished circuit initialization process.
```

```
64210132>rem ren Unary_Op_Bin_Tree.csv Unary_Op_Bin_Tree_64210132.csv
```

```
64210132>xst -ifn unary_vhdl93.xst
Release 14.7 - xst P.20131013 (nt64)
Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.
--> Parameter TMPDIR set to xst/projnav.tmp
```

```
Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.26 secs
```

```
--> Parameter xsthdpdir set to xst
```

Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.26 secs

-->

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 - 8.4.5) Cross Clock Domains Report

```
=====
*      Synthesis Options Summary      *
=====
```

---- Source Parameters

Input File Name : "./unary_vhdl93.prj"
Ignore Synthesis Constraint File : NO

---- Target Parameters

Output File Name : "reduction_operators"
Output Format : NGC
Target Device : xc6slx4-3-tqg144

---- Source Options

Top Module Name : reduction_operators
Automatic FSM Extraction : YES
FSM Encoding Algorithm : Auto
Safe Implementation : No
FSM Style : LUT
RAM Extraction : Yes
RAM Style : Auto
ROM Extraction : Yes
Shift Register Extraction : YES
ROM Style : Auto
Resource Sharing : YES
Asynchronous To Synchronous : NO
Shift Register Minimum Size : 2
Use DSP Block : Auto
Automatic Register Balancing : No

---- Target Options

LUT Combining : Auto
Reduce Control Sets : Auto
Add IO Buffers : YES

Global Maximum Fanout : 100000
Add Generic Clock Buffer(BUFG) : 16
Register Duplication : YES
Optimize Instantiated Primitives : NO
Use Clock Enable : Auto
Use Synchronous Set : Auto
Use Synchronous Reset : Auto
Pack IO Registers into IOBs : Auto
Equivalent register Removal : YES

---- General Options

Optimization Goal : Speed
Optimization Effort : 1
Power Reduction : NO
Keep Hierarchy : No
Netlist Hierarchy : As_Optimized
RTL Output : Yes
Global Optimization : AllClockNets
Read Cores : YES
Write Timing Constraints : NO
Cross Clock Analysis : NO
Hierarchy Separator : /
Bus Delimiter : <>
Case Specifier : Maintain
Slice Utilization Ratio : 100
BRAM Utilization Ratio : 100
DSP48 Utilization Ratio : 100
Auto BRAM Packing : NO
Slice Utilization Ratio Delta : 5

=====

=====

* HDL Parsing *

=====

Parsing VHDL file "64210132\unary_operators_vhdl_93.vhd" into library work
Parsing entity <reduction_operators>.
Parsing architecture <vhdl_93_process> of entity <reduction_operators>.

=====

* HDL Elaboration *

=====

Elaborating entity <reduction_operators> (architecture <vhdl_93_process>) with
generics from library <work>.

=====

* HDL Synthesis *

=====

Synthesizing Unit <reduction_operators>.

Related source file is "64210132\unary_operators_vhdl_93.vhd".

N = 64

Summary:

inferred 128 Multiplexer(s).

Unit <reduction_operators> synthesized.

=====

HDL Synthesis Report

Macro Statistics

Multiplexers : 128
1-bit 2-to-1 multiplexer : 128
Xors : 1
1-bit xor64 : 1

=====

=====

* Advanced HDL Synthesis *

=====

=====

Advanced HDL Synthesis Report

Macro Statistics

Multiplexers : 128
1-bit 2-to-1 multiplexer : 128
Xors : 1
1-bit xor64 : 1

=====

=====

* Low Level Synthesis *

=====

Optimizing unit <reduction_operators> ...

Mapping all equations...

Building and optimizing final netlist ...

Found area constraint ratio of 100 (+ 5) on block reduction_operators, actual ratio is 1.

Final Macro Processing ...

=====

Final Register Report

Found no macro

=====

=====

* Partition Report *

=====

Partition Implementation Status

No Partitions were found in this design.

=====

* Design Summary *

=====

Top Level Output File Name : reduction_operators.ngc

Primitive and Black Box Usage:

```
-----  
# BELS           : 59  
# GND            : 1  
# LUT4           : 3  
# LUT6           : 32  
# MUXCY          : 22  
# VCC            : 1  
# IO Buffers     : 67  
# IBUF           : 64  
# OBUF           : 3
```

Device utilization summary:

Selected Device : 6slx4tqg144-3

Slice Logic Utilization:

Number of Slice LUTs: 35 out of 2400 1%
Number used as Logic: 35 out of 2400 1%

Slice Logic Distribution:

Number of LUT Flip Flop pairs used: 35
Number with an unused Flip Flop: 35 out of 35 100%
Number with an unused LUT: 0 out of 35 0%
Number of fully used LUT-FF pairs: 0 out of 35 0%
Number of unique control sets: 0

IO Utilization:

Number of IOs: 67
Number of bonded IOBs: 67 out of 102 65%

Specific Feature Utilization:

----- Partition Resource Summary: -----

No Partitions were found in this design.

=====

Timing Report

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.

FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT
GENERATED AFTER PLACE-and-ROUTE.

Clock Information:

No clock signals found in this design

Asynchronous Control Signals Information:

No asynchronous control signals found in this design

Timing Summary:

Speed Grade: -3

Minimum period: No path found
Minimum input arrival time before clock: No path found
Maximum output required time after clock: No path found
Maximum combinational path delay: 7.522ns

Timing Details:

All values displayed in nanoseconds (ns)

=====
Timing constraint: Default path analysis
Total number of paths / destination ports: 192 / 3

Delay: 7.522ns (Levels of Logic = 5)
Source: A<22> (PAD)
Destination: reduced_XOR (PAD)

Data Path: A<22> to reduced_XOR

	Gate	Net				
Cell:	in->out	fanout	Delay	Delay	Logical Name	(Net Name)

IBUF:I->O	3	1.222	1.015	A_22_IBUF	(A_22_IBUF)
LUT6:I0->O	1	0.203	0.944	Mxor_reduced_XOR_xo<0>3	(Mxor_reduced_XOR_xo<0>2)
LUT6:I0->O	1	0.203	0.580	Mxor_reduced_XOR_xo<0>14_SW0	(N01)
LUT6:I5->O	1	0.205	0.579	Mxor_reduced_XOR_xo<0>14	(reduced_XOR_OBUF)
OBUF:I->O		2.571		reduced_XOR_OBUF	(reduced_XOR)

Total 7.522ns (4.404ns logic, 3.118ns route)
(58.5% logic, 41.5% route)
=====

Cross Clock Domains Report:

=====
Total REAL time to Xst completion: 10.00 secs
Total CPU time to Xst completion: 9.89 secs

-->

Total memory usage is 4487516 kilobytes

Number of errors : 0 (0 filtered)
Number of warnings : 0 (0 filtered)
Number of infos : 0 (0 filtered)

64210132>fuse -incremental -o unary_vhdl93_tb_isim_beh.exe -prj
unary_vhdl93_tb.prj -top reduction_operators_tb
Running: C:\Xilinx\14.7\ISE_DS\ISE\bin\nt64\unwrapped\fuse.exe -incremental -o
unary_vhdl93_tb_isim_beh.exe -prj unary_vhdl93_tb.prj -top reduction_operators_tb
ISim P.20131013 (signature 0x7708f090)
Number of CPUs detected in this system: 8
Turning on mult-threading, number of parallel sub-compilation jobs: 16
Determining compilation order of HDL files

```
Parsing VHDL file "unary_operators_vhdl_93.vhd" into library work
Parsing VHDL file "unary_operators_vhdl93_IDEAL_tb.vhd" into library work
Starting static elaboration
Completed static elaboration
Compiling package standard
Compiling package std_logic_1164
Compiling package numeric_std
Compiling package textio
Compiling package std_logic_textio
Compiling architecture vhdl_93_process of entity reduction_operators
[\\reduction_operators(3)\\]
Compiling architecture test of entity reduction_operators_tb
Time Resolution for simulation is 1ps.
Waiting for 1 sub-compilation(s) to finish...
Compiled 8 VHDL Units
Built simulation executable unary_vhdl93_tb_isim_beh.exe
Fuse Memory Usage: 36724 KB
Fuse CPU Usage: 859 ms
```

```
64210132>if exist reduction_operators.csv del reduction_operators.csv
```

```
64210132>if exist reduction_operators_64210132.csv del
reduction_operators_64210132.csv
```

```
64210132>unary_vhdl93_tb_isim_beh.exe -tclbatch isim.tcl -wdb
unary_vhdl93_tb_isim_beh.wdb
ISim P.20131013 (signature 0x7708f090)
WARNING: A WEBPACK license was found.
WARNING: Please use Xilinx License Configuration Manager to check out a full ISim
license.
WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for
more information on the differences between the Lite and the Full version.
This is a Lite version of ISim.
Time resolution is 1 ps
Simulator is doing circuit initialization process.
Finished circuit initialization process.
```

```
64210132>rem ren reduction_operators.csv reduction_operators_64210132.csv
```

```
-- *****
-- **** STUDENT: 64210290
-- *****
-- KOMENTARJI K OCENI NALOGE
-- Matej Možek: Ni pripomb
-- *****
```

```
64210290>if not exist "xst" mkdir xst
```

```
64210290>cd XST
```

```
64210290\xst>if not exist "projnav.tmp" mkdir "projnav.tmp"
```

```
64210290\xst>cd ..
```

```
64210290>xst -ifn unary_tree.xst
Release 14.7 - xst P.20131013 (nt64)
Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.
--> Parameter TMPDIR set to xst/projnav.tmp
```

```
Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.24 secs
```

```
--> Parameter xsthdpdir set to xst
```

```
Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.24 secs
```

```
-->
```

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 - 8.4.5) Cross Clock Domains Report

```
=====
*      Synthesis Options Summary      *
=====
```

---- Source Parameters

```
Input File Name      : "unary_tree.prj"
Ignore Synthesis Constraint File : NO
```

---- Target Parameters

```
Output File Name     : "Unary_Op_Bin_Tree"
```

Output Format : NGC
Target Device : xc6slx4-3-tqg144

----- Source Options

Top Module Name : Unary_Op_Bin_Tree
Automatic FSM Extraction : YES
FSM Encoding Algorithm : Auto
Safe Implementation : No
FSM Style : LUT
RAM Extraction : Yes
RAM Style : Auto
ROM Extraction : Yes
Shift Register Extraction : YES
ROM Style : Auto
Resource Sharing : YES
Asynchronous To Synchronous : NO
Shift Register Minimum Size : 2
Use DSP Block : Auto
Automatic Register Balancing : No

----- Target Options

LUT Combining : Auto
Reduce Control Sets : Auto
Add IO Buffers : YES
Global Maximum Fanout : 100000
Add Generic Clock Buffer(BUFG) : 16
Register Duplication : YES
Optimize Instantiated Primitives : NO
Use Clock Enable : Auto
Use Synchronous Set : Auto
Use Synchronous Reset : Auto
Pack IO Registers into IOBs : Auto
Equivalent register Removal : YES

----- General Options

Optimization Goal : Speed
Optimization Effort : 1
Power Reduction : NO
Keep Hierarchy : No
Netlist Hierarchy : As_Optimized
RTL Output : Yes
Global Optimization : AllClockNets
Read Cores : YES
Write Timing Constraints : NO
Cross Clock Analysis : NO
Hierarchy Separator : /
Bus Delimiter : <>
Case Specifier : Maintain
Slice Utilization Ratio : 100
BRAM Utilization Ratio : 100
DSP48 Utilization Ratio : 100
Auto BRAM Packing : NO
Slice Utilization Ratio Delta : 5

=====

=====

* HDL Parsing *

=====

Parsing VHDL file "64210290\unary_op_xor_tree_lut6.vhd" into library work
Parsing entity <XorTreeStage>.
Parsing architecture <tree_of_xor_lut6> of entity <xortreestage>.
Parsing VHDL file "64210290\unary_op_tree.vhd" into library work
Parsing entity <Unary_Op_Bin_Tree>.
Parsing architecture <t> of entity <unary_op_bin_tree>.

```
=====
*          HDL Elaboration          *
=====
```

Elaborating entity <Unary_Op_Bin_Tree> (architecture <t>) with generics from library <work>.

Elaborating entity <XorTreeStage> (architecture <tree_of_xor_lut6>) with generics from library <work>.

Elaborating entity <XorTreeStage> (architecture <tree_of_xor_lut6>) with generics from library <work>.

Elaborating entity <XorTreeStage> (architecture <tree_of_xor_lut6>) with generics from library <work>.

Elaborating entity <XorTreeStage> (architecture <tree_of_xor_lut6>) with generics from library <work>.

Elaborating entity <XorTreeStage> (architecture <tree_of_xor_lut6>) with generics from library <work>.

Elaborating entity <XorTreeStage> (architecture <tree_of_xor_lut6>) with generics from library <work>.

Elaborating entity <XorTreeStage> (architecture <tree_of_xor_lut6>) with generics from library <work>.

Elaborating entity <XorTreeStage> (architecture <tree_of_xor_lut6>) with generics from library <work>.

Elaborating entity <XorTreeStage> (architecture <tree_of_xor_lut6>) with generics from library <work>.

```
=====
*          HDL Synthesis            *
=====
```

Synthesizing Unit <Unary_Op_Bin_Tree>.
Related source file is "64210290\unary_op_tree.vhd".
N = 4096
Summary:
no macro.
Unit <Unary_Op_Bin_Tree> synthesized.

Synthesizing Unit <XorTreeStage_1>.
Related source file is "64210290\unary_op_xor_tree_lut6.vhd".
N = 4096
Summary:
no macro.
Unit <XorTreeStage_1> synthesized.

Synthesizing Unit <XorTreeStage_2>.
Related source file is "64210290\unary_op_xor_tree_lut6.vhd".
N = 682
Summary:
no macro.
Unit <XorTreeStage_2> synthesized.

Synthesizing Unit <XorTreeStage_3>.
Related source file is "64210290\unary_op_xor_tree_lut6.vhd".
N = 113
Summary:
no macro.
Unit <XorTreeStage_3> synthesized.

Synthesizing Unit <XorTreeStage_4>.
Related source file is "64210290\unary_op_xor_tree_lut6.vhd".
N = 18
Summary:
no macro.
Unit <XorTreeStage_4> synthesized.

Synthesizing Unit <XorTreeStage_5>.
Related source file is "64210290\unary_op_xor_tree_lut6.vhd".
N = 3
Summary:
no macro.
Unit <XorTreeStage_5> synthesized.

Synthesizing Unit <XorTreeStage_6>.
Related source file is "64210290\unary_op_xor_tree_lut6.vhd".
N = 19
Summary:
no macro.
Unit <XorTreeStage_6> synthesized.

Synthesizing Unit <XorTreeStage_7>.
Related source file is "64210290\unary_op_xor_tree_lut6.vhd".
N = 4
Summary:
no macro.
Unit <XorTreeStage_7> synthesized.

Synthesizing Unit <XorTreeStage_8>.
Related source file is "64210290\unary_op_xor_tree_lut6.vhd".
N = 114
Summary:
no macro.
Unit <XorTreeStage_8> synthesized.

Synthesizing Unit <XorTreeStage_9>.
Related source file is "64210290\unary_op_xor_tree_lut6.vhd".
N = 683
Summary:
no macro.
Unit <XorTreeStage_9> synthesized.

=====
HDL Synthesis Report

Found no macro

```
=====
*      Advanced HDL Synthesis      *
=====
```

```
=====
Advanced HDL Synthesis Report
=====
```

Found no macro

```
=====
*      Low Level Synthesis      *
=====
```

Optimizing unit <Unary_Op_Bin_Tree> ...

Mapping all equations...

Building and optimizing final netlist ...

Found area constraint ratio of 100 (+ 5) on block Unary_Op_Bin_Tree, actual ratio is 94.

Final Macro Processing ...

```
=====
Final Register Report
=====
```

Found no macro

```
=====
*      Partition Report      *
=====
```

Partition Implementation Status

No Partitions were found in this design.

```
=====
*      Design Summary      *
=====
```

Top Level Output File Name : Unary_Op_Bin_Tree.ngc

Primitive and Black Box Usage:

# BELS	: 1555
# LUT3	: 1088
# LUT4	: 208
# LUT6	: 259
# IO Buffers	: 4097
# IBUF	: 4096
# OBUF	: 1

Device utilization summary:

Selected Device : 6slx4tqg144-3

Slice Logic Utilization:

Number of Slice LUTs: 1555 out of 2400 64%
Number used as Logic: 1555 out of 2400 64%

Slice Logic Distribution:

Number of LUT Flip Flop pairs used: 1555
Number with an unused Flip Flop: 1555 out of 1555 100%
Number with an unused LUT: 0 out of 1555 0%
Number of fully used LUT-FF pairs: 0 out of 1555 0%
Number of unique control sets: 0

IO Utilization:

Number of IOs: 4097
Number of bonded IOBs: 4097 out of 102 4016% (*)

Specific Feature Utilization:

WARNING:Xst:1336 - (*) More than 100% of Device resources are used

Partition Resource Summary:

No Partitions were found in this design.

=====

Timing Report

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.
FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT
GENERATED AFTER PLACE-and-ROUTE.

Clock Information:

No clock signals found in this design

Asynchronous Control Signals Information:

No asynchronous control signals found in this design

Timing Summary:

Speed Grade: -3

Minimum period: No path found
Minimum input arrival time before clock: No path found
Maximum output required time after clock: No path found
Maximum combinational path delay: 10.106ns

Timing Details:

All values displayed in nanoseconds (ns)

```

=====
Timing constraint: Default path analysis
Total number of paths / destination ports: 4096 / 1
-----
Delay: 10.106ns (Levels of Logic = 7)
Source: I<0> (PAD)
Destination: O_Xor (PAD)

Data Path: I<0> to O_Xor
Gate Net
Cell:in->out fanout Delay Delay Logical Name (Net Name)
-----
IBUF:I->O 1 1.222 0.808 I_0_IBUF (I_0_IBUF)
LUT3:I0->O 1 0.339 0.944
U_Xor/Stages.piece0_tree/Stages.piece0_tree/Stages.piece0_tree/Stages.piece0_tree/
Stage_xor_3.XOR3_LUT
(U_Xor/Stages.piece0_tree/Stages.piece0_tree/Stages.piece0_tree/Stages.piece0_xor)
LUT6:I0->O 1 0.203 0.944
U_Xor/Stages.piece0_tree/Stages.piece0_tree/Stages.piece0_tree/Stages.XOR6_LUT
(U_Xor/Stages.piece0_tree/Stages.piece0_tree/Stages.piece0_xor)
LUT6:I0->O 1 0.203 0.944
U_Xor/Stages.piece0_tree/Stages.piece0_tree/Stages.XOR6_LUT
(U_Xor/Stages.piece0_tree/Stages.piece0_xor)
LUT6:I0->O 1 0.203 0.944 U_Xor/Stages.piece0_tree/Stages.XOR6_LUT
(U_Xor/Stages.piece0_xor)
LUT6:I0->O 1 0.203 0.579 U_Xor/Stages.XOR6_LUT (O_Xor_OBUF)
OBUF:I->O 2.571 O_Xor_OBUF (O_Xor)
-----
Total 10.106ns (4.944ns logic, 5.162ns route)
(48.9% logic, 51.1% route)
=====

```

Cross Clock Domains Report:

```

-----
Total REAL time to Xst completion: 18.00 secs
Total CPU time to Xst completion: 17.88 secs

```

-->

Total memory usage is 4538304 kilobytes

```

Number of errors : 0 ( 0 filtered)
Number of warnings : 1 ( 0 filtered)
Number of infos : 0 ( 0 filtered)

```

```

64210290>fuse -incremental -o unary_tree_tb_isim_beh.exe -prj unary_tree_tb.prj -
top Unary_Op_Bin_Tree_tb
Running: C:\Xilinx\14.7\ISE_DS\ISE\bin\nt64\unwrapped\fuse.exe -incremental -o
unary_tree_tb_isim_beh.exe -prj unary_tree_tb.prj -top Unary_Op_Bin_Tree_tb
ISim P.20131013 (signature 0x7708f090)
Number of CPUs detected in this system: 8
Turning on mult-threading, number of parallel sub-compilation jobs: 16
Determining compilation order of HDL files
Parsing VHDL file "slv_image_pkg.vhd" into library work

```

```
Parsing VHDL file "unary_op_xor_tree_lut6.vhd" into library work
Parsing VHDL file "unary_op_tree.vhd" into library work
Parsing VHDL file "unary_op_tree_IDEAL_tb.vhd" into library work
Starting static elaboration
Completed static elaboration
Compiling package standard
Compiling package std_logic_1164
Compiling package numeric_std
Compiling package textio
Compiling package std_logic_textio
Compiling package slv_image_pkg
Compiling package vcomponents
Compiling package vital_timing
Compiling package vital_primitives
Compiling package vpkg
Compiling architecture tree_of_xor_lut6 of entity XorTreeStage [\XorTreeStage(2)\]
Compiling architecture lut3_v of entity LUT3 [\LUT3("10010110")(0,7)\]
Compiling architecture tree_of_xor_lut6 of entity XorTreeStage [\XorTreeStage(3)\]
Compiling architecture lut6_v of entity LUT6 [\LUT6("0110100110010110100101100...")
Compiling architecture tree_of_xor_lut6 of entity XorTreeStage
[\XorTreeStage(16)\]
Compiling architecture t of entity Unary_Op_Bin_Tree [\Unary_Op_Bin_Tree(16)\]
Compiling architecture test of entity unary_op_bin_tree_tb
Time Resolution for simulation is 1ps.
Waiting for 1 sub-compilation(s) to finish...
Compiled 23 VHDL Units
Built simulation executable unary_tree_tb_isim_beh.exe
Fuse Memory Usage: 59288 KB
Fuse CPU Usage: 1296 ms
```

```
64210290>if exist Unary_Op_Bin_Tree.csv del Unary_Op_Bin_Tree.csv
```

```
64210290>if exist Unary_Op_Bin_Tree_64210290.csv del
Unary_Op_Bin_Tree_64210290.csv
```

```
64210290>unary_tree_tb_isim_beh.exe -tclbatch isim.tcl -wdb
unary_tree_tb_isim_beh.wdb
ISim P.20131013 (signature 0x7708f090)
WARNING: A WEBPACK license was found.
WARNING: Please use Xilinx License Configuration Manager to check out a full ISim
license.
WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for
more information on the differences between the Lite and the Full version.
This is a Lite version of ISim.
Time resolution is 1 ps
Simulator is doing circuit initialization process.
Finished circuit initialization process.
```

```
64210290>rem ren Unary_Op_Bin_Tree.csv Unary_Op_Bin_Tree_64210290.csv
```

```
64210290>xst -ifn unary_vhdl93.xst
Release 14.7 - xst P.20131013 (nt64)
Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.
--> Parameter TMPDIR set to xst/projnav.tmp
```

```
Total REAL time to Xst completion: 1.00 secs
Total CPU time to Xst completion: 0.23 secs
```

```
--> Parameter xsthdpdir set to xst
```

Total REAL time to Xst completion: 1.00 secs
Total CPU time to Xst completion: 0.24 secs

-->

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 - 8.4.5) Cross Clock Domains Report

```
=====
*      Synthesis Options Summary      *
=====
```

---- Source Parameters

Input File Name : "./unary_vhdl93.prj"
Ignore Synthesis Constraint File : NO

---- Target Parameters

Output File Name : "reduction_operators"
Output Format : NGC
Target Device : xc6slx4-3-tqg144

---- Source Options

Top Module Name : reduction_operators
Automatic FSM Extraction : YES
FSM Encoding Algorithm : Auto
Safe Implementation : No
FSM Style : LUT
RAM Extraction : Yes
RAM Style : Auto
ROM Extraction : Yes
Shift Register Extraction : YES
ROM Style : Auto
Resource Sharing : YES
Asynchronous To Synchronous : NO
Shift Register Minimum Size : 2
Use DSP Block : Auto
Automatic Register Balancing : No

---- Target Options

LUT Combining : Auto
Reduce Control Sets : Auto
Add IO Buffers : YES

Global Maximum Fanout : 100000
Add Generic Clock Buffer(BUFG) : 16
Register Duplication : YES
Optimize Instantiated Primitives : NO
Use Clock Enable : Auto
Use Synchronous Set : Auto
Use Synchronous Reset : Auto
Pack IO Registers into IOBs : Auto
Equivalent register Removal : YES

---- General Options

Optimization Goal : Speed
Optimization Effort : 1
Power Reduction : NO
Keep Hierarchy : No
Netlist Hierarchy : As_Optimized
RTL Output : Yes
Global Optimization : AllClockNets
Read Cores : YES
Write Timing Constraints : NO
Cross Clock Analysis : NO
Hierarchy Separator : /
Bus Delimiter : <>
Case Specifier : Maintain
Slice Utilization Ratio : 100
BRAM Utilization Ratio : 100
DSP48 Utilization Ratio : 100
Auto BRAM Packing : NO
Slice Utilization Ratio Delta : 5

=====

=====

* HDL Parsing *

=====

Parsing VHDL file "64210290\unary_operators_vhdl_93.vhd" into library work
Parsing entity <reduction_operators>.
Parsing architecture <vhdl_93_process> of entity <reduction_operators>.

=====

* HDL Elaboration *

=====

Elaborating entity <reduction_operators> (architecture <vhdl_93_process>) with
generics from library <work>.

=====

* HDL Synthesis *

=====

Synthesizing Unit <reduction_operators>.

Related source file is "64210290\unary_operators_vhdl_93.vhd".

N = 64

Summary:

inferred 128 Multiplexer(s).

Unit <reduction_operators> synthesized.

=====

HDL Synthesis Report

Macro Statistics

Multiplexers : 128
1-bit 2-to-1 multiplexer : 128
Xors : 1
1-bit xor64 : 1

=====

=====

* Advanced HDL Synthesis *

=====

=====

Advanced HDL Synthesis Report

Macro Statistics

Multiplexers : 128
1-bit 2-to-1 multiplexer : 128
Xors : 1
1-bit xor64 : 1

=====

=====

* Low Level Synthesis *

=====

Optimizing unit <reduction_operators> ...

Mapping all equations...

Building and optimizing final netlist ...

Found area constraint ratio of 100 (+ 5) on block reduction_operators, actual ratio is 1.

Final Macro Processing ...

=====

Final Register Report

Found no macro

=====

=====

* Partition Report *

=====

Partition Implementation Status

No Partitions were found in this design.

=====

* Design Summary *

=====

Top Level Output File Name : reduction_operators.ngc

Primitive and Black Box Usage:

```
-----  
# BELS      : 59  
# GND       : 1  
# LUT4      : 3  
# LUT6      : 32  
# MUXCY     : 22  
# VCC       : 1  
# IO Buffers : 67  
# IBUF      : 64  
# OBUF      : 3
```

Device utilization summary:

Selected Device : 6slx4tqg144-3

Slice Logic Utilization:

Number of Slice LUTs: 35 out of 2400 1%
Number used as Logic: 35 out of 2400 1%

Slice Logic Distribution:

Number of LUT Flip Flop pairs used: 35
Number with an unused Flip Flop: 35 out of 35 100%
Number with an unused LUT: 0 out of 35 0%
Number of fully used LUT-FF pairs: 0 out of 35 0%
Number of unique control sets: 0

IO Utilization:

Number of IOs: 67
Number of bonded IOBs: 67 out of 102 65%

Specific Feature Utilization:

----- Partition Resource Summary: -----

No Partitions were found in this design.

=====

Timing Report

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.

FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT
GENERATED AFTER PLACE-and-ROUTE.

Clock Information:

No clock signals found in this design

Asynchronous Control Signals Information:

No asynchronous control signals found in this design

Timing Summary:

Speed Grade: -3

Minimum period: No path found
Minimum input arrival time before clock: No path found
Maximum output required time after clock: No path found
Maximum combinational path delay: 7.522ns

Timing Details:

All values displayed in nanoseconds (ns)

=====
Timing constraint: Default path analysis
Total number of paths / destination ports: 192 / 3

Delay: 7.522ns (Levels of Logic = 5)
Source: A<22> (PAD)
Destination: reduced_XOR (PAD)

Data Path: A<22> to reduced_XOR

	Gate	Net				
Cell:	in->out	fanout	Delay	Delay	Logical Name	(Net Name)

IBUF:I->O	3	1.222	1.015	A_22_IBUF	(A_22_IBUF)
LUT6:I0->O	1	0.203	0.944	Mxor_reduced_XOR_xo<0>3	(Mxor_reduced_XOR_xo<0>2)
LUT6:I0->O	1	0.203	0.580	Mxor_reduced_XOR_xo<0>14_SW0	(N01)
LUT6:I5->O	1	0.205	0.579	Mxor_reduced_XOR_xo<0>14	(reduced_XOR_OBUF)
OBUF:I->O		2.571		reduced_XOR_OBUF	(reduced_XOR)

Total 7.522ns (4.404ns logic, 3.118ns route)
(58.5% logic, 41.5% route)
=====

Cross Clock Domains Report:

=====
Total REAL time to Xst completion: 11.00 secs
Total CPU time to Xst completion: 10.77 secs

-->

Total memory usage is 4487516 kilobytes

Number of errors : 0 (0 filtered)
Number of warnings : 0 (0 filtered)
Number of infos : 0 (0 filtered)

64210290>fuse -incremental -o unary_vhdl93_tb_isim_beh.exe -prj
unary_vhdl93_tb.prj -top reduction_operators_tb
Running: C:\Xilinx\14.7\ISE_DS\ISE\bin\nt64\unwrapped\fuse.exe -incremental -o
unary_vhdl93_tb_isim_beh.exe -prj unary_vhdl93_tb.prj -top reduction_operators_tb
ISim P.20131013 (signature 0x7708f090)
Number of CPUs detected in this system: 8
Turning on mult-threading, number of parallel sub-compilation jobs: 16
Determining compilation order of HDL files


```
Parsing VHDL file "unary_operators_vhdl_93.vhd" into library work
Parsing VHDL file "unary_operators_vhdl93_IDEAL_tb.vhd" into library work
Starting static elaboration
Completed static elaboration
Compiling package standard
Compiling package std_logic_1164
Compiling package numeric_std
Compiling package textio
Compiling package std_logic_textio
Compiling architecture vhdl_93_process of entity reduction_operators
[\\reduction_operators(3)\\]
Compiling architecture test of entity reduction_operators_tb
Time Resolution for simulation is 1ps.
Compiled 8 VHDL Units
Built simulation executable unary_vhdl93_tb_isim_beh.exe
Fuse Memory Usage: 36828 KB
Fuse CPU Usage: 796 ms
```

```
64210290>if exist reduction_operators.csv del reduction_operators.csv
```

```
64210290>if exist reduction_operators_64210290.csv del
reduction_operators_64210290.csv
```

```
64210290>unary_vhdl93_tb_isim_beh.exe -tclbatch isim.tcl -wdb
unary_vhdl93_tb_isim_beh.wdb
ISim P.20131013 (signature 0x7708f090)
WARNING: A WEBPACK license was found.
WARNING: Please use Xilinx License Configuration Manager to check out a full ISim
license.
WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for
more information on the differences between the Lite and the Full version.
This is a Lite version of ISim.
Time resolution is 1 ps
Simulator is doing circuit initialization process.
Finished circuit initialization process.
```

```
64210290>rem ren reduction_operators.csv reduction_operators_64210290.csv
```

```
-- *****
-- **** STUDENT: 64210382
-- *****
-- KOMENTARJI K OCENI NALOGE
-- Matej Možek: Ni pripomb
-- *****
```

```
64210382>if not exist "xst" mkdir xst
```

```
64210382>cd XST
```

```
64210382\xst>if not exist "projnav.tmp" mkdir "projnav.tmp"
```

```
64210382\xst>cd ..
```

```
64210382>xst -ifn unary_tree.xst
Release 14.7 - xst P.20131013 (nt64)
Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.
--> Parameter TMPDIR set to xst/projnav.tmp
```

```
Total REAL time to Xst completion: 0.00 secs
```

```
Total CPU time to Xst completion: 0.23 secs
```

```
--> Parameter xsthdpdir set to xst
```

```
Total REAL time to Xst completion: 0.00 secs
```

```
Total CPU time to Xst completion: 0.23 secs
```

```
-->
```

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 - 8.4.5) Cross Clock Domains Report

```
=====
*      Synthesis Options Summary      *
=====
```

---- Source Parameters

```
Input File Name      : "unary_tree.prj"
Ignore Synthesis Constraint File : NO
```

---- Target Parameters

```
Output File Name     : "Unary_Op_Bin_Tree"
```

Output Format : NGC
Target Device : xc6slx4-3-tqg144

----- Source Options

Top Module Name : Unary_Op_Bin_Tree
Automatic FSM Extraction : YES
FSM Encoding Algorithm : Auto
Safe Implementation : No
FSM Style : LUT
RAM Extraction : Yes
RAM Style : Auto
ROM Extraction : Yes
Shift Register Extraction : YES
ROM Style : Auto
Resource Sharing : YES
Asynchronous To Synchronous : NO
Shift Register Minimum Size : 2
Use DSP Block : Auto
Automatic Register Balancing : No

----- Target Options

LUT Combining : Auto
Reduce Control Sets : Auto
Add IO Buffers : YES
Global Maximum Fanout : 100000
Add Generic Clock Buffer(BUFG) : 16
Register Duplication : YES
Optimize Instantiated Primitives : NO
Use Clock Enable : Auto
Use Synchronous Set : Auto
Use Synchronous Reset : Auto
Pack IO Registers into IOBs : Auto
Equivalent register Removal : YES

----- General Options

Optimization Goal : Speed
Optimization Effort : 1
Power Reduction : NO
Keep Hierarchy : No
Netlist Hierarchy : As_Optimized
RTL Output : Yes
Global Optimization : AllClockNets
Read Cores : YES
Write Timing Constraints : NO
Cross Clock Analysis : NO
Hierarchy Separator : /
Bus Delimiter : <>
Case Specifier : Maintain
Slice Utilization Ratio : 100
BRAM Utilization Ratio : 100
DSP48 Utilization Ratio : 100
Auto BRAM Packing : NO
Slice Utilization Ratio Delta : 5

=====

=====

* HDL Parsing *

=====

Parsing VHDL file "64210382\unary_op_xor_tree_lut6.vhd" into library work
Parsing entity <XorTreeStage>.
Parsing architecture <tree_of_xor_lut6> of entity <xortreestage>.
Parsing VHDL file "64210382\unary_op_tree.vhd" into library work
Parsing entity <Unary_Op_Bin_Tree>.
Parsing architecture <t> of entity <unary_op_bin_tree>.

```
=====
*          HDL Elaboration          *
=====
```

Elaborating entity <Unary_Op_Bin_Tree> (architecture <t>) with generics from library <work>.

Elaborating entity <XorTreeStage> (architecture <tree_of_xor_lut6>) with generics from library <work>.

Elaborating entity <XorTreeStage> (architecture <tree_of_xor_lut6>) with generics from library <work>.

Elaborating entity <XorTreeStage> (architecture <tree_of_xor_lut6>) with generics from library <work>.

Elaborating entity <XorTreeStage> (architecture <tree_of_xor_lut6>) with generics from library <work>.

Elaborating entity <XorTreeStage> (architecture <tree_of_xor_lut6>) with generics from library <work>.

Elaborating entity <XorTreeStage> (architecture <tree_of_xor_lut6>) with generics from library <work>.

Elaborating entity <XorTreeStage> (architecture <tree_of_xor_lut6>) with generics from library <work>.

Elaborating entity <XorTreeStage> (architecture <tree_of_xor_lut6>) with generics from library <work>.

Elaborating entity <XorTreeStage> (architecture <tree_of_xor_lut6>) with generics from library <work>.

```
=====
*          HDL Synthesis            *
=====
```

Synthesizing Unit <Unary_Op_Bin_Tree>.
Related source file is "64210382\unary_op_tree.vhd".
N = 4096
Summary:
no macro.
Unit <Unary_Op_Bin_Tree> synthesized.

Synthesizing Unit <XorTreeStage_1>.
Related source file is "64210382\unary_op_xor_tree_lut6.vhd".
N = 4096
Summary:
no macro.
Unit <XorTreeStage_1> synthesized.

Synthesizing Unit <XorTreeStage_2>.
Related source file is "64210382\unary_op_xor_tree_lut6.vhd".
N = 683
Summary:
no macro.
Unit <XorTreeStage_2> synthesized.

Synthesizing Unit <XorTreeStage_3>.
Related source file is "64210382\unary_op_xor_tree_lut6.vhd".
N = 114
Summary:
no macro.
Unit <XorTreeStage_3> synthesized.

Synthesizing Unit <XorTreeStage_4>.
Related source file is "64210382\unary_op_xor_tree_lut6.vhd".
N = 19
Summary:
no macro.
Unit <XorTreeStage_4> synthesized.

Synthesizing Unit <XorTreeStage_5>.
Related source file is "64210382\unary_op_xor_tree_lut6.vhd".
N = 4
Summary:
no macro.
Unit <XorTreeStage_5> synthesized.

Synthesizing Unit <XorTreeStage_6>.
Related source file is "64210382\unary_op_xor_tree_lut6.vhd".
N = 3
Summary:
no macro.
Unit <XorTreeStage_6> synthesized.

Synthesizing Unit <XorTreeStage_7>.
Related source file is "64210382\unary_op_xor_tree_lut6.vhd".
N = 113
Summary:
no macro.
Unit <XorTreeStage_7> synthesized.

Synthesizing Unit <XorTreeStage_8>.
Related source file is "64210382\unary_op_xor_tree_lut6.vhd".
N = 18
Summary:
no macro.
Unit <XorTreeStage_8> synthesized.

Synthesizing Unit <XorTreeStage_9>.
Related source file is "64210382\unary_op_xor_tree_lut6.vhd".
N = 682
Summary:
no macro.
Unit <XorTreeStage_9> synthesized.

=====
HDL Synthesis Report

Found no macro

```
=====
*      Advanced HDL Synthesis      *
=====
```

```
=====
Advanced HDL Synthesis Report
=====
```

Found no macro

```
=====
*      Low Level Synthesis      *
=====
```

Optimizing unit <Unary_Op_Bin_Tree> ...

Mapping all equations...

Building and optimizing final netlist ...

Found area constraint ratio of 100 (+ 5) on block Unary_Op_Bin_Tree, actual ratio is 94.

Final Macro Processing ...

```
=====
Final Register Report
=====
```

Found no macro

```
=====
*      Partition Report      *
=====
```

Partition Implementation Status

No Partitions were found in this design.

```
=====
*      Design Summary      *
=====
```

Top Level Output File Name : Unary_Op_Bin_Tree.ngc

Primitive and Black Box Usage:

# BELS	: 1555
# LUT3	: 1088
# LUT4	: 208
# LUT6	: 259
# IO Buffers	: 4097
# IBUF	: 4096
# OBUF	: 1

Device utilization summary:

Selected Device : 6slx4tqg144-3

Slice Logic Utilization:

Number of Slice LUTs: 1555 out of 2400 64%
Number used as Logic: 1555 out of 2400 64%

Slice Logic Distribution:

Number of LUT Flip Flop pairs used: 1555
Number with an unused Flip Flop: 1555 out of 1555 100%
Number with an unused LUT: 0 out of 1555 0%
Number of fully used LUT-FF pairs: 0 out of 1555 0%
Number of unique control sets: 0

IO Utilization:

Number of IOs: 4097
Number of bonded IOBs: 4097 out of 102 4016% (*)

Specific Feature Utilization:

WARNING:Xst:1336 - (*) More than 100% of Device resources are used

----- Partition Resource Summary: -----

No Partitions were found in this design.

=====

Timing Report

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.
FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT
GENERATED AFTER PLACE-and-ROUTE.

Clock Information:

No clock signals found in this design

Asynchronous Control Signals Information:

No asynchronous control signals found in this design

Timing Summary:

Speed Grade: -3

Minimum period: No path found
Minimum input arrival time before clock: No path found
Maximum output required time after clock: No path found
Maximum combinational path delay: 10.106ns

Timing Details:

All values displayed in nanoseconds (ns)

```

=====
Timing constraint: Default path analysis
Total number of paths / destination ports: 4096 / 1
-----
Delay:      10.106ns (Levels of Logic = 7)
Source:     I<4092> (PAD)
Destination: O_Xor (PAD)

Data Path: I<4092> to O_Xor
Gate Net
Cell:in->out fanout Delay Delay Logical Name (Net Name)
-----
IBUF:I->O      1 1.222 0.827 I_4092_IBUF (I_4092_IBUF)
LUT4:I0->O     1 0.320 0.944
U_Xor/Stages.Tree1/Stages.Tree1/Stages.Tree1/Stages.Tree1/Stage_Xor_4.XOR4_LUT4
(U_Xor/Stages.Tree1/Stages.Tree1/Stages.Tree1/Stages.Xor_1)
LUT6:I0->O     1 0.203 0.944
U_Xor/Stages.Tree1/Stages.Tree1/Stages.Tree1/Stages.XOR6_LUT6
(U_Xor/Stages.Tree1/Stages.Tree1/Stages.Xor_1)
LUT6:I0->O     1 0.203 0.944 U_Xor/Stages.Tree1/Stages.Tree1/Stages.XOR6_LUT6
(U_Xor/Stages.Tree1/Stages.Xor_1)
LUT6:I0->O     1 0.203 0.944 U_Xor/Stages.Tree1/Stages.XOR6_LUT6
(U_Xor/Stages.Xor_1)
LUT6:I0->O     1 0.203 0.579 U_Xor/Stages.XOR6_LUT6 (O_Xor_OBUF)
OBUF:I->O      2.571 O_Xor_OBUF (O_Xor)
-----
Total      10.106ns (4.925ns logic, 5.181ns route)
          (48.7% logic, 51.3% route)
=====

```

Cross Clock Domains Report:

```

=====
Total REAL time to Xst completion: 17.00 secs
Total CPU time to Xst completion: 16.99 secs

```

-->

Total memory usage is 4538348 kilobytes

```

Number of errors : 0 ( 0 filtered)
Number of warnings : 1 ( 0 filtered)
Number of infos : 0 ( 0 filtered)

```

```

64210382>fuse -incremental -o unary_tree_tb_isim_beh.exe -prj unary_tree_tb.prj -
top Unary_Op_Bin_Tree_tb
Running: C:\Xilinx\14.7\ISE_DS\ISE\bin\nt64\unwrapped\fuse.exe -incremental -o
unary_tree_tb_isim_beh.exe -prj unary_tree_tb.prj -top Unary_Op_Bin_Tree_tb
ISim P.20131013 (signature 0x7708f090)
Number of CPUs detected in this system: 8
Turning on mult-threading, number of parallel sub-compilation jobs: 16
Determining compilation order of HDL files
Parsing VHDL file "slv_image_pkg.vhd" into library work
Parsing VHDL file "unary_op_xor_tree_lut6.vhd" into library work
Parsing VHDL file "unary_op_tree.vhd" into library work

```



```
Parsing VHDL file "unary_op_tree_IDEAL_tb.vhd" into library work
Starting static elaboration
Completed static elaboration
Compiling package standard
Compiling package std_logic_1164
Compiling package numeric_std
Compiling package textio
Compiling package std_logic_textio
Compiling package slv_image_pkg
Compiling package vcomponents
Compiling package vital_timing
Compiling package vital_primitives
Compiling package vpkg
Compiling architecture lut3_v of entity LUT3 [\LUT3("10010110")(0,7)\]
Compiling architecture tree_of_xor_lut6 of entity XorTreeStage [\XorTreeStage(3)\]
Compiling architecture tree_of_xor_lut6 of entity XorTreeStage [\XorTreeStage(2)\]
Compiling architecture lut6_v of entity LUT6 [\LUT6("0110100110010110100101100...")
Compiling architecture tree_of_xor_lut6 of entity XorTreeStage
[\XorTreeStage(16)\]
Compiling architecture t of entity Unary_Op_Bin_Tree [\Unary_Op_Bin_Tree(16)\]
Compiling architecture test of entity unary_op_bin_tree_tb
Time Resolution for simulation is 1ps.
Waiting for 1 sub-compilation(s) to finish...
Compiled 23 VHDL Units
Built simulation executable unary_tree_tb_isim_beh.exe
Fuse Memory Usage: 60032 KB
Fuse CPU Usage: 1296 ms
```

```
64210382>if exist Unary_Op_Bin_Tree.csv del Unary_Op_Bin_Tree.csv
```

```
64210382>if exist Unary_Op_Bin_Tree_64210382.csv del
Unary_Op_Bin_Tree_64210382.csv
```

```
64210382>unary_tree_tb_isim_beh.exe -tclbatch isim.tcl -wdb
unary_tree_tb_isim_beh.wdb
ISim P.20131013 (signature 0x7708f090)
WARNING: A WEBPACK license was found.
WARNING: Please use Xilinx License Configuration Manager to check out a full ISim
license.
WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for
more information on the differences between the Lite and the Full version.
This is a Lite version of ISim.
Time resolution is 1 ps
Simulator is doing circuit initialization process.
Finished circuit initialization process.
```

```
64210382>rem ren Unary_Op_Bin_Tree.csv Unary_Op_Bin_Tree_64210382.csv
```

```
64210382>xst -ifn unary_vhdl93.xst
Release 14.7 - xst P.20131013 (nt64)
Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.
--> Parameter TMPDIR set to xst/projnav.tmp
```

```
Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.23 secs
```

```
--> Parameter xsthdpdir set to xst
```

```
Total REAL time to Xst completion: 0.00 secs
```

Total CPU time to Xst completion: 0.23 secs

-->

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 - 8.4.5) Cross Clock Domains Report

```
=====
*      Synthesis Options Summary      *
=====
```

---- Source Parameters

Input File Name : "./unary_vhd193.prj"
Ignore Synthesis Constraint File : NO

---- Target Parameters

Output File Name : "reduction_operators"
Output Format : NGC
Target Device : xc6slx4-3-tqg144

---- Source Options

Top Module Name : reduction_operators
Automatic FSM Extraction : YES
FSM Encoding Algorithm : Auto
Safe Implementation : No
FSM Style : LUT
RAM Extraction : Yes
RAM Style : Auto
ROM Extraction : Yes
Shift Register Extraction : YES
ROM Style : Auto
Resource Sharing : YES
Asynchronous To Synchronous : NO
Shift Register Minimum Size : 2
Use DSP Block : Auto
Automatic Register Balancing : No

---- Target Options

LUT Combining : Auto
Reduce Control Sets : Auto
Add IO Buffers : YES
Global Maximum Fanout : 100000
Add Generic Clock Buffer(BUFG) : 16

Register Duplication : YES
Optimize Instantiated Primitives : NO
Use Clock Enable : Auto
Use Synchronous Set : Auto
Use Synchronous Reset : Auto
Pack IO Registers into IOBs : Auto
Equivalent register Removal : YES

---- General Options

Optimization Goal : Speed
Optimization Effort : 1
Power Reduction : NO
Keep Hierarchy : No
Netlist Hierarchy : As_Optimized
RTL Output : Yes
Global Optimization : AllClockNets
Read Cores : YES
Write Timing Constraints : NO
Cross Clock Analysis : NO
Hierarchy Separator : /
Bus Delimiter : <>
Case Specifier : Maintain
Slice Utilization Ratio : 100
BRAM Utilization Ratio : 100
DSP48 Utilization Ratio : 100
Auto BRAM Packing : NO
Slice Utilization Ratio Delta : 5

=====

=====

* HDL Parsing *

=====

Parsing VHDL file "64210382\unary_operators_vhdl_93.vhd" into library work
Parsing entity <reduction_operators>.
Parsing architecture <vhdl_93_process> of entity <reduction_operators>.

=====

* HDL Elaboration *

=====

Elaborating entity <reduction_operators> (architecture <vhdl_93_process>) with
generics from library <work>.

=====

* HDL Synthesis *

=====

Synthesizing Unit <reduction_operators>.
Related source file is "64210382\unary_operators_vhdl_93.vhd".
N = 64
Summary:
inferred 128 Multiplexer(s).
Unit <reduction_operators> synthesized.

=====

HDL Synthesis Report

Macro Statistics

```
# Multiplexers          : 128
 1-bit 2-to-1 multiplexer : 128
# Xors                  : 1
 1-bit xor64            : 1
```

=====

=====

```
*      Advanced HDL Synthesis      *
```

=====

=====

Advanced HDL Synthesis Report

Macro Statistics

```
# Multiplexers          : 128
 1-bit 2-to-1 multiplexer : 128
# Xors                  : 1
 1-bit xor64            : 1
```

=====

=====

```
*      Low Level Synthesis      *
```

=====

Optimizing unit <reduction_operators> ...

Mapping all equations...

Building and optimizing final netlist ...

Found area constraint ratio of 100 (+ 5) on block reduction_operators, actual ratio is 1.

Final Macro Processing ...

=====

Final Register Report

Found no macro

=====

=====

```
*      Partition Report      *
```

=====

Partition Implementation Status

No Partitions were found in this design.

=====

```
*      Design Summary      *
```

=====

Top Level Output File Name : reduction_operators.ngc

Primitive and Black Box Usage:

```
-----  
# BELS      : 59  
# GND       : 1  
# LUT4      : 3  
# LUT6      : 32  
# MUXCY     : 22  
# VCC       : 1  
# IO Buffers : 67  
# IBUF      : 64  
# OBUF      : 3
```

Device utilization summary:

Selected Device : 6slx4tqg144-3

Slice Logic Utilization:

Number of Slice LUTs: 35 out of 2400 1%
Number used as Logic: 35 out of 2400 1%

Slice Logic Distribution:

Number of LUT Flip Flop pairs used: 35
Number with an unused Flip Flop: 35 out of 35 100%
Number with an unused LUT: 0 out of 35 0%
Number of fully used LUT-FF pairs: 0 out of 35 0%
Number of unique control sets: 0

IO Utilization:

Number of IOs: 67
Number of bonded IOBs: 67 out of 102 65%

Specific Feature Utilization:

Partition Resource Summary:

No Partitions were found in this design.

=====

Timing Report

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.
FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT
GENERATED AFTER PLACE-and-ROUTE.

Clock Information:

No clock signals found in this design

Asynchronous Control Signals Information:

No asynchronous control signals found in this design

Timing Summary:

Speed Grade: -3

Minimum period: No path found
Minimum input arrival time before clock: No path found
Maximum output required time after clock: No path found
Maximum combinational path delay: 7.522ns

Timing Details:

All values displayed in nanoseconds (ns)

=====

Timing constraint: Default path analysis
Total number of paths / destination ports: 192 / 3

Delay: 7.522ns (Levels of Logic = 5)
Source: A<22> (PAD)
Destination: reduced_XOR (PAD)

Data Path: A<22> to reduced_XOR
Gate Net

Cell:in->out fanout Delay Delay Logical Name (Net Name)

IBUF:I->O 3 1.222 1.015 A_22_IBUF (A_22_IBUF)
LUT6:I0->O 1 0.203 0.944 Mxor_reduced_XOR_xo<0>3 (Mxor_reduced_XOR_xo<0>2)
LUT6:I0->O 1 0.203 0.580 Mxor_reduced_XOR_xo<0>14_SW0 (N01)
LUT6:I5->O 1 0.205 0.579 Mxor_reduced_XOR_xo<0>14 (reduced_XOR_OBUF)
OBUF:I->O 2.571 reduced_XOR_OBUF (reduced_XOR)

Total 7.522ns (4.404ns logic, 3.118ns route)
(58.5% logic, 41.5% route)

Cross Clock Domains Report:

=====

Total REAL time to Xst completion: 11.00 secs
Total CPU time to Xst completion: 10.99 secs

-->

Total memory usage is 4487516 kilobytes

Number of errors : 0 (0 filtered)
Number of warnings : 0 (0 filtered)
Number of infos : 0 (0 filtered)

64210382>fuse -incremental -o unary_vhdl93_tb_isim_beh.exe -prj
unary_vhdl93_tb.prj -top reduction_operators_tb
Running: C:\Xilinx\14.7\ISE_DS\ISE\bin\nt64\unwrapped\fuse.exe -incremental -o
unary_vhdl93_tb_isim_beh.exe -prj unary_vhdl93_tb.prj -top reduction_operators_tb
ISim P.20131013 (signature 0x7708f090)
Number of CPUs detected in this system: 8
Turning on mult-threading, number of parallel sub-compilation jobs: 16
Determining compilation order of HDL files
Parsing VHDL file "unary_operators_vhdl_93.vhd" into library work
Parsing VHDL file "unary_operators_vhdl93_IDEAL_tb.vhd" into library work

```
Starting static elaboration
Completed static elaboration
Compiling package standard
Compiling package std_logic_1164
Compiling package numeric_std
Compiling package textio
Compiling package std_logic_textio
Compiling architecture vhdl_93_process of entity reduction_operators
[\\reduction_operators(3)\\]
Compiling architecture test of entity reduction_operators_tb
Time Resolution for simulation is 1ps.
Waiting for 1 sub-compilation(s) to finish...
Compiled 8 VHDL Units
Built simulation executable unary_vhdl93_tb_isim_beh.exe
Fuse Memory Usage: 36656 KB
Fuse CPU Usage: 921 ms
```

```
64210382>if exist reduction_operators.csv del reduction_operators.csv
```

```
64210382>if exist reduction_operators_64210382.csv del
reduction_operators_64210382.csv
```

```
64210382>unary_vhdl93_tb_isim_beh.exe -tclbatch isim.tcl -wdb
unary_vhdl93_tb_isim_beh.wdb
ISim P.20131013 (signature 0x7708f090)
WARNING: A WEBPACK license was found.
WARNING: Please use Xilinx License Configuration Manager to check out a full ISim
license.
WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for
more information on the differences between the Lite and the Full version.
This is a Lite version of ISim.
Time resolution is 1 ps
Simulator is doing circuit initialization process.
Finished circuit initialization process.
```

```
64210382>rem ren reduction_operators.csv reduction_operators_64210382.csv
```

```
-- *****
-- **** STUDENT: 64210384
-- *****
-- KOMENTARJI K OCENI NALOGE
-- Matej Možek: Ni pripomb
-- *****
```

```
64210384>if not exist "xst" mkdir xst
```

```
64210384>cd XST
```

```
64210384\xst>if not exist "projnav.tmp" mkdir "projnav.tmp"
```

```
64210384\xst>cd ..
```

```
64210384>xst -ifn unary_tree.xst
Release 14.7 - xst P.20131013 (nt64)
Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.
--> Parameter TMPDIR set to xst/projnav.tmp
```

```
Total REAL time to Xst completion: 1.00 secs
Total CPU time to Xst completion: 0.23 secs
```

```
--> Parameter xsthdpdir set to xst
```

```
Total REAL time to Xst completion: 1.00 secs
Total CPU time to Xst completion: 0.23 secs
```

```
-->
```

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 - 8.4.5) Cross Clock Domains Report

```
=====
*      Synthesis Options Summary      *
=====
```

---- Source Parameters

```
Input File Name      : "unary_tree.prj"
Ignore Synthesis Constraint File : NO
```

---- Target Parameters

```
Output File Name     : "Unary_Op_Bin_Tree"
```


Output Format : NGC
Target Device : xc6slx4-3-tqg144

---- Source Options

Top Module Name : Unary_Op_Bin_Tree
Automatic FSM Extraction : YES
FSM Encoding Algorithm : Auto
Safe Implementation : No
FSM Style : LUT
RAM Extraction : Yes
RAM Style : Auto
ROM Extraction : Yes
Shift Register Extraction : YES
ROM Style : Auto
Resource Sharing : YES
Asynchronous To Synchronous : NO
Shift Register Minimum Size : 2
Use DSP Block : Auto
Automatic Register Balancing : No

---- Target Options

LUT Combining : Auto
Reduce Control Sets : Auto
Add IO Buffers : YES
Global Maximum Fanout : 100000
Add Generic Clock Buffer(BUFG) : 16
Register Duplication : YES
Optimize Instantiated Primitives : NO
Use Clock Enable : Auto
Use Synchronous Set : Auto
Use Synchronous Reset : Auto
Pack IO Registers into IOBs : Auto
Equivalent register Removal : YES

---- General Options

Optimization Goal : Speed
Optimization Effort : 1
Power Reduction : NO
Keep Hierarchy : No
Netlist Hierarchy : As_Optimized
RTL Output : Yes
Global Optimization : AllClockNets
Read Cores : YES
Write Timing Constraints : NO
Cross Clock Analysis : NO
Hierarchy Separator : /
Bus Delimiter : <>
Case Specifier : Maintain
Slice Utilization Ratio : 100
BRAM Utilization Ratio : 100
DSP48 Utilization Ratio : 100
Auto BRAM Packing : NO
Slice Utilization Ratio Delta : 5

=====

=====

* HDL Parsing *

=====

Parsing VHDL file "64210384\unary_op_xor_tree_lut6.vhd" into library work
Parsing entity <XorTreeStage>.
Parsing architecture <tree_of_xor_lut6> of entity <xortreestage>.
Parsing VHDL file "64210384\unary_op_tree.vhd" into library work
Parsing entity <Unary_Op_Bin_Tree>.
Parsing architecture <t> of entity <unary_op_bin_tree>.

```
=====
*          HDL Elaboration          *
=====
```

Elaborating entity <Unary_Op_Bin_Tree> (architecture <t>) with generics from library <work>.

Elaborating entity <XorTreeStage> (architecture <tree_of_xor_lut6>) with generics from library <work>.

Elaborating entity <XorTreeStage> (architecture <tree_of_xor_lut6>) with generics from library <work>.

Elaborating entity <XorTreeStage> (architecture <tree_of_xor_lut6>) with generics from library <work>.

Elaborating entity <XorTreeStage> (architecture <tree_of_xor_lut6>) with generics from library <work>.

Elaborating entity <XorTreeStage> (architecture <tree_of_xor_lut6>) with generics from library <work>.

Elaborating entity <XorTreeStage> (architecture <tree_of_xor_lut6>) with generics from library <work>.

Elaborating entity <XorTreeStage> (architecture <tree_of_xor_lut6>) with generics from library <work>.

Elaborating entity <XorTreeStage> (architecture <tree_of_xor_lut6>) with generics from library <work>.

Elaborating entity <XorTreeStage> (architecture <tree_of_xor_lut6>) with generics from library <work>.

```
=====
*          HDL Synthesis            *
=====
```

Synthesizing Unit <Unary_Op_Bin_Tree>.
Related source file is "64210384\unary_op_tree.vhd".
N = 4096
Summary:
no macro.
Unit <Unary_Op_Bin_Tree> synthesized.

Synthesizing Unit <XorTreeStage_1>.
Related source file is "64210384\unary_op_xor_tree_lut6.vhd".
N = 4096
Summary:
no macro.
Unit <XorTreeStage_1> synthesized.

Synthesizing Unit <XorTreeStage_2>.
Related source file is "64210384\unary_op_xor_tree_lut6.vhd".
N = 682
Summary:
no macro.
Unit <XorTreeStage_2> synthesized.

Synthesizing Unit <XorTreeStage_3>.
Related source file is "64210384\unary_op_xor_tree_lut6.vhd".
N = 113
Summary:
no macro.
Unit <XorTreeStage_3> synthesized.

Synthesizing Unit <XorTreeStage_4>.
Related source file is "64210384\unary_op_xor_tree_lut6.vhd".
N = 18
Summary:
no macro.
Unit <XorTreeStage_4> synthesized.

Synthesizing Unit <XorTreeStage_5>.
Related source file is "64210384\unary_op_xor_tree_lut6.vhd".
N = 3
Summary:
no macro.
Unit <XorTreeStage_5> synthesized.

Synthesizing Unit <XorTreeStage_6>.
Related source file is "64210384\unary_op_xor_tree_lut6.vhd".
N = 19
Summary:
no macro.
Unit <XorTreeStage_6> synthesized.

Synthesizing Unit <XorTreeStage_7>.
Related source file is "64210384\unary_op_xor_tree_lut6.vhd".
N = 4
Summary:
no macro.
Unit <XorTreeStage_7> synthesized.

Synthesizing Unit <XorTreeStage_8>.
Related source file is "64210384\unary_op_xor_tree_lut6.vhd".
N = 114
Summary:
no macro.
Unit <XorTreeStage_8> synthesized.

Synthesizing Unit <XorTreeStage_9>.
Related source file is "64210384\unary_op_xor_tree_lut6.vhd".
N = 683
Summary:
no macro.
Unit <XorTreeStage_9> synthesized.

=====
HDL Synthesis Report

Found no macro

```
=====
*      Advanced HDL Synthesis      *
=====
```

```
=====
Advanced HDL Synthesis Report
=====
```

Found no macro

```
=====
*      Low Level Synthesis      *
=====
```

Optimizing unit <Unary_Op_Bin_Tree> ...

Mapping all equations...

Building and optimizing final netlist ...

Found area constraint ratio of 100 (+ 5) on block Unary_Op_Bin_Tree, actual ratio is 94.

Final Macro Processing ...

```
=====
Final Register Report
=====
```

Found no macro

```
=====
*      Partition Report      *
=====
```

Partition Implementation Status

No Partitions were found in this design.

```
=====
*      Design Summary      *
=====
```

Top Level Output File Name : Unary_Op_Bin_Tree.ngc

Primitive and Black Box Usage:

# BELS	: 1555
# LUT3	: 1088
# LUT4	: 208
# LUT6	: 259
# IO Buffers	: 4097
# IBUF	: 4096
# OBUF	: 1

Device utilization summary:

Selected Device : 6slx4tqg144-3

Slice Logic Utilization:

Number of Slice LUTs: 1555 out of 2400 64%
Number used as Logic: 1555 out of 2400 64%

Slice Logic Distribution:

Number of LUT Flip Flop pairs used: 1555
Number with an unused Flip Flop: 1555 out of 1555 100%
Number with an unused LUT: 0 out of 1555 0%
Number of fully used LUT-FF pairs: 0 out of 1555 0%
Number of unique control sets: 0

IO Utilization:

Number of IOs: 4097
Number of bonded IOBs: 4097 out of 102 4016% (*)

Specific Feature Utilization:

WARNING:Xst:1336 - (*) More than 100% of Device resources are used

Partition Resource Summary:

No Partitions were found in this design.

=====

Timing Report

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.
FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT
GENERATED AFTER PLACE-and-ROUTE.

Clock Information:

No clock signals found in this design

Asynchronous Control Signals Information:

No asynchronous control signals found in this design

Timing Summary:

Speed Grade: -3

Minimum period: No path found
Minimum input arrival time before clock: No path found
Maximum output required time after clock: No path found
Maximum combinational path delay: 10.106ns

Timing Details:

All values displayed in nanoseconds (ns)

```

=====
Timing constraint: Default path analysis
Total number of paths / destination ports: 4096 / 1
-----
Delay:      10.106ns (Levels of Logic = 7)
Source:     I<0> (PAD)
Destination: O_Xor (PAD)

Data Path: I<0> to O_Xor
Gate Net
Cell:in->out fanout Delay Delay Logical Name (Net Name)
-----
IBUF:I->O      1 1.222 0.808 I_0_IBUF (I_0_IBUF)
LUT3:I0->O     1 0.339 0.944
U_Xor/stages.Tree1/stages.Tree1/stages.Tree1/stage_xor_3.xor3_lut3
(U_Xor/stages.Tree1/stages.Tree1/stages.Tree1/stages.Xor_1)
LUT6:I0->O     1 0.203 0.944
U_Xor/stages.Tree1/stages.Tree1/stages.Tree1/stages.xor6_lut6
(U_Xor/stages.Tree1/stages.Tree1/stages.Xor_1)
LUT6:I0->O     1 0.203 0.944 U_Xor/stages.Tree1/stages.Tree1/stages.xor6_lut6
(U_Xor/stages.Tree1/stages.Xor_1)
LUT6:I0->O     1 0.203 0.944 U_Xor/stages.Tree1/stages.xor6_lut6
(U_Xor/stages.Xor_1)
LUT6:I0->O     1 0.203 0.579 U_Xor/stages.xor6_lut6 (O_Xor_OBUF)
OBUF:I->O      2.571 O_Xor_OBUF (O_Xor)
-----
Total      10.106ns (4.944ns logic, 5.162ns route)
          (48.9% logic, 51.1% route)
=====

```

Cross Clock Domains Report:

```

=====
Total REAL time to Xst completion: 17.00 secs
Total CPU time to Xst completion: 17.01 secs

```

-->

Total memory usage is 4538344 kilobytes

```

Number of errors : 0 ( 0 filtered)
Number of warnings : 1 ( 0 filtered)
Number of infos : 0 ( 0 filtered)

```

```

64210384>fuse -incremental -o unary_tree_tb_isim_beh.exe -prj unary_tree_tb.prj -
top Unary_Op_Bin_Tree_tb
Running: C:\Xilinx\14.7\ISE_DS\ISE\bin\nt64\unwrapped\fuse.exe -incremental -o
unary_tree_tb_isim_beh.exe -prj unary_tree_tb.prj -top Unary_Op_Bin_Tree_tb
ISim P.20131013 (signature 0x7708f090)
Number of CPUs detected in this system: 8
Turning on mult-threading, number of parallel sub-compilation jobs: 16
Determining compilation order of HDL files
Parsing VHDL file "slv_image_pkg.vhd" into library work
Parsing VHDL file "unary_op_xor_tree_lut6.vhd" into library work
Parsing VHDL file "unary_op_tree.vhd" into library work

```

```
Parsing VHDL file "unary_op_tree_IDEAL_tb.vhd" into library work
Starting static elaboration
Completed static elaboration
Compiling package standard
Compiling package std_logic_1164
Compiling package numeric_std
Compiling package textio
Compiling package std_logic_textio
Compiling package slv_image_pkg
Compiling package vcomponents
Compiling package vital_timing
Compiling package vital_primitives
Compiling package vpkg
Compiling architecture tree_of_xor_lut6 of entity XorTreeStage [\XorTreeStage(2)\]
Compiling architecture lut3_v of entity LUT3 [\LUT3("10010110")(0,7)\]
Compiling architecture tree_of_xor_lut6 of entity XorTreeStage [\XorTreeStage(3)\]
Compiling architecture lut6_v of entity LUT6 [\LUT6("0110100110010110100101100...)]
Compiling architecture tree_of_xor_lut6 of entity XorTreeStage
[\XorTreeStage(16)\]
Compiling architecture t of entity Unary_Op_Bin_Tree [\Unary_Op_Bin_Tree(16)\]
Compiling architecture test of entity unary_op_bin_tree_tb
Time Resolution for simulation is 1ps.
Waiting for 1 sub-compilation(s) to finish...
Compiled 23 VHDL Units
Built simulation executable unary_tree_tb_isim_beh.exe
Fuse Memory Usage: 59892 KB
Fuse CPU Usage: 1280 ms
```

```
64210384>if exist Unary_Op_Bin_Tree.csv del Unary_Op_Bin_Tree.csv
```

```
64210384>if exist Unary_Op_Bin_Tree_64210384.csv del
Unary_Op_Bin_Tree_64210384.csv
```

```
64210384>unary_tree_tb_isim_beh.exe -tclbatch isim.tcl -wdb
unary_tree_tb_isim_beh.wdb
ISim P.20131013 (signature 0x7708f090)
WARNING: A WEBPACK license was found.
WARNING: Please use Xilinx License Configuration Manager to check out a full ISim
license.
WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for
more information on the differences between the Lite and the Full version.
This is a Lite version of ISim.
Time resolution is 1 ps
Simulator is doing circuit initialization process.
Finished circuit initialization process.
```

```
64210384>rem ren Unary_Op_Bin_Tree.csv Unary_Op_Bin_Tree_64210384.csv
```

```
64210384>xst -ifn unary_vhdl93.xst
Release 14.7 - xst P.20131013 (nt64)
Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.
--> Parameter TMPDIR set to xst/projnav.tmp
```

```
Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.25 secs
```

```
--> Parameter xsthdpdir set to xst
```

```
Total REAL time to Xst completion: 0.00 secs
```

Total CPU time to Xst completion: 0.25 secs

-->

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```
=====
*      Synthesis Options Summary      *
=====
```

---- Source Parameters

Input File Name : "./unary_vhd193.prj"
Ignore Synthesis Constraint File : NO

---- Target Parameters

Output File Name : "reduction_operators"
Output Format : NGC
Target Device : xc6slx4-3-tqg144

---- Source Options

Top Module Name : reduction_operators
Automatic FSM Extraction : YES
FSM Encoding Algorithm : Auto
Safe Implementation : No
FSM Style : LUT
RAM Extraction : Yes
RAM Style : Auto
ROM Extraction : Yes
Shift Register Extraction : YES
ROM Style : Auto
Resource Sharing : YES
Asynchronous To Synchronous : NO
Shift Register Minimum Size : 2
Use DSP Block : Auto
Automatic Register Balancing : No

---- Target Options

LUT Combining : Auto
Reduce Control Sets : Auto
Add IO Buffers : YES
Global Maximum Fanout : 100000
Add Generic Clock Buffer(BUFG) : 16

Register Duplication : YES
Optimize Instantiated Primitives : NO
Use Clock Enable : Auto
Use Synchronous Set : Auto
Use Synchronous Reset : Auto
Pack IO Registers into IOBs : Auto
Equivalent register Removal : YES

---- General Options

Optimization Goal : Speed
Optimization Effort : 1
Power Reduction : NO
Keep Hierarchy : No
Netlist Hierarchy : As_Optimized
RTL Output : Yes
Global Optimization : AllClockNets
Read Cores : YES
Write Timing Constraints : NO
Cross Clock Analysis : NO
Hierarchy Separator : /
Bus Delimiter : <>
Case Specifier : Maintain
Slice Utilization Ratio : 100
BRAM Utilization Ratio : 100
DSP48 Utilization Ratio : 100
Auto BRAM Packing : NO
Slice Utilization Ratio Delta : 5

=====

=====

* HDL Parsing *

=====

Parsing VHDL file "64210384\unary_operators_vhdl_93.vhd" into library work
Parsing entity <reduction_operators>.
Parsing architecture <vhdl_93_process> of entity <reduction_operators>.

=====

* HDL Elaboration *

=====

Elaborating entity <reduction_operators> (architecture <vhdl_93_process>) with
generics from library <work>.

=====

* HDL Synthesis *

=====

Synthesizing Unit <reduction_operators>.
Related source file is "64210384\unary_operators_vhdl_93.vhd".
N = 64
Summary:
inferred 128 Multiplexer(s).
Unit <reduction_operators> synthesized.

=====

HDL Synthesis Report

Macro Statistics

```
# Multiplexers          : 128
 1-bit 2-to-1 multiplexer : 128
# Xors                  : 1
 1-bit xor64            : 1
```

=====

=====

```
*      Advanced HDL Synthesis      *
```

=====

=====

Advanced HDL Synthesis Report

Macro Statistics

```
# Multiplexers          : 128
 1-bit 2-to-1 multiplexer : 128
# Xors                  : 1
 1-bit xor64            : 1
```

=====

=====

```
*      Low Level Synthesis      *
```

=====

Optimizing unit <reduction_operators> ...

Mapping all equations...

Building and optimizing final netlist ...

Found area constraint ratio of 100 (+ 5) on block reduction_operators, actual ratio is 1.

Final Macro Processing ...

=====

Final Register Report

Found no macro

=====

=====

```
*      Partition Report      *
```

=====

Partition Implementation Status

No Partitions were found in this design.

=====

```
*      Design Summary      *
```

=====

Top Level Output File Name : reduction_operators.ngc

Primitive and Black Box Usage:

```
-----
# BELS      : 59
# GND       : 1
# LUT4      : 3
# LUT6      : 32
# MUXCY     : 22
# VCC       : 1
# IO Buffers : 67
# IBUF      : 64
# OBUF      : 3
```

Device utilization summary:

Selected Device : 6slx4tqg144-3

Slice Logic Utilization:

Number of Slice LUTs: 35 out of 2400 1%
Number used as Logic: 35 out of 2400 1%

Slice Logic Distribution:

Number of LUT Flip Flop pairs used: 35
Number with an unused Flip Flop: 35 out of 35 100%
Number with an unused LUT: 0 out of 35 0%
Number of fully used LUT-FF pairs: 0 out of 35 0%
Number of unique control sets: 0

IO Utilization:

Number of IOs: 67
Number of bonded IOBs: 67 out of 102 65%

Specific Feature Utilization:

Partition Resource Summary:

No Partitions were found in this design.

=====

Timing Report

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.
FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT
GENERATED AFTER PLACE-and-ROUTE.

Clock Information:

No clock signals found in this design

Asynchronous Control Signals Information:

No asynchronous control signals found in this design

Timing Summary:

Speed Grade: -3

Minimum period: No path found
Minimum input arrival time before clock: No path found
Maximum output required time after clock: No path found
Maximum combinational path delay: 7.522ns

Timing Details:

All values displayed in nanoseconds (ns)

=====

Timing constraint: Default path analysis
Total number of paths / destination ports: 192 / 3

Delay: 7.522ns (Levels of Logic = 5)
Source: A<22> (PAD)
Destination: reduced_XOR (PAD)

Data Path: A<22> to reduced_XOR
Gate Net

Cell:in->out fanout Delay Delay Logical Name (Net Name)

IBUF:I->O 3 1.222 1.015 A_22_IBUF (A_22_IBUF)
LUT6:I0->O 1 0.203 0.944 Mxor_reduced_XOR_xo<0>3 (Mxor_reduced_XOR_xo<0>2)
LUT6:I0->O 1 0.203 0.580 Mxor_reduced_XOR_xo<0>14_SW0 (N01)
LUT6:I5->O 1 0.205 0.579 Mxor_reduced_XOR_xo<0>14 (reduced_XOR_OBUF)
OBUF:I->O 2.571 reduced_XOR_OBUF (reduced_XOR)

Total 7.522ns (4.404ns logic, 3.118ns route)
(58.5% logic, 41.5% route)

Cross Clock Domains Report:

=====

Total REAL time to Xst completion: 14.00 secs
Total CPU time to Xst completion: 14.40 secs

-->

Total memory usage is 4487516 kilobytes

Number of errors : 0 (0 filtered)
Number of warnings : 0 (0 filtered)
Number of infos : 0 (0 filtered)

64210384>fuse -incremental -o unary_vhdl93_tb_isim_beh.exe -prj
unary_vhdl93_tb.prj -top reduction_operators_tb
Running: C:\Xilinx\14.7\ISE_DS\ISE\bin\nt64\unwrapped\fuse.exe -incremental -o
unary_vhdl93_tb_isim_beh.exe -prj unary_vhdl93_tb.prj -top reduction_operators_tb
ISim P.20131013 (signature 0x7708f090)
Number of CPUs detected in this system: 8
Turning on mult-threading, number of parallel sub-compilation jobs: 16
Determining compilation order of HDL files
Parsing VHDL file "unary_operators_vhdl_93.vhd" into library work
Parsing VHDL file "unary_operators_vhdl93_IDEAL_tb.vhd" into library work

```
Starting static elaboration
Completed static elaboration
Compiling package standard
Compiling package std_logic_1164
Compiling package numeric_std
Compiling package textio
Compiling package std_logic_textio
Compiling architecture vhdl_93_process of entity reduction_operators
[\\reduction_operators(3)\\]
Compiling architecture test of entity reduction_operators_tb
Time Resolution for simulation is 1ps.
Waiting for 1 sub-compilation(s) to finish...
Compiled 8 VHDL Units
Built simulation executable unary_vhdl93_tb_isim_beh.exe
Fuse Memory Usage: 36832 KB
Fuse CPU Usage: 874 ms
```

```
64210384>if exist reduction_operators.csv del reduction_operators.csv
```

```
64210384>if exist reduction_operators_64210384.csv del
reduction_operators_64210384.csv
```

```
64210384>unary_vhdl93_tb_isim_beh.exe -tclbatch isim.tcl -wdb
unary_vhdl93_tb_isim_beh.wdb
ISim P.20131013 (signature 0x7708f090)
WARNING: A WEBPACK license was found.
WARNING: Please use Xilinx License Configuration Manager to check out a full ISim
license.
WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for
more information on the differences between the Lite and the Full version.
This is a Lite version of ISim.
Time resolution is 1 ps
Simulator is doing circuit initialization process.
Finished circuit initialization process.
```

```
64210384>rem ren reduction_operators.csv reduction_operators_64210384.csv
```

```
-- *****
-- **** STUDENT: 64210386
-- *****
-- KOMENTARJI K OCENI NALOGE
-- Matej Možek: Ni pripomb
-- *****
```

```
64210386>if not exist "xst" mkdir xst
```

```
64210386>cd XST
```

```
64210386\xst>if not exist "projnav.tmp" mkdir "projnav.tmp"
```

```
64210386\xst>cd ..
```

```
64210386>xst -ifn unary_tree.xst
Release 14.7 - xst P.20131013 (nt64)
Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.
--> Parameter TMPDIR set to xst/projnav.tmp
```

```
Total REAL time to Xst completion: 0.00 secs
```

```
Total CPU time to Xst completion: 0.23 secs
```

```
--> Parameter xsthdpdir set to xst
```

```
Total REAL time to Xst completion: 0.00 secs
```

```
Total CPU time to Xst completion: 0.23 secs
```

```
-->
```

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```
=====
*      Synthesis Options Summary      *
=====
```

---- Source Parameters

```
Input File Name      : "unary_tree.prj"
Ignore Synthesis Constraint File : NO
```

---- Target Parameters

```
Output File Name     : "Unary_Op_Bin_Tree"
```

Output Format : NGC
Target Device : xc6slx4-3-tqg144

----- Source Options

Top Module Name : Unary_Op_Bin_Tree
Automatic FSM Extraction : YES
FSM Encoding Algorithm : Auto
Safe Implementation : No
FSM Style : LUT
RAM Extraction : Yes
RAM Style : Auto
ROM Extraction : Yes
Shift Register Extraction : YES
ROM Style : Auto
Resource Sharing : YES
Asynchronous To Synchronous : NO
Shift Register Minimum Size : 2
Use DSP Block : Auto
Automatic Register Balancing : No

----- Target Options

LUT Combining : Auto
Reduce Control Sets : Auto
Add IO Buffers : YES
Global Maximum Fanout : 100000
Add Generic Clock Buffer(BUFG) : 16
Register Duplication : YES
Optimize Instantiated Primitives : NO
Use Clock Enable : Auto
Use Synchronous Set : Auto
Use Synchronous Reset : Auto
Pack IO Registers into IOBs : Auto
Equivalent register Removal : YES

----- General Options

Optimization Goal : Speed
Optimization Effort : 1
Power Reduction : NO
Keep Hierarchy : No
Netlist Hierarchy : As_Optimized
RTL Output : Yes
Global Optimization : AllClockNets
Read Cores : YES
Write Timing Constraints : NO
Cross Clock Analysis : NO
Hierarchy Separator : /
Bus Delimiter : <>
Case Specifier : Maintain
Slice Utilization Ratio : 100
BRAM Utilization Ratio : 100
DSP48 Utilization Ratio : 100
Auto BRAM Packing : NO
Slice Utilization Ratio Delta : 5

=====

=====

* HDL Parsing *

=====

```

Parsing VHDL file "64210386\unary_op_xor_tree_lut6.vhd" into library work
Parsing entity <XorTreeStage>.
Parsing architecture <tree_of_xor_lut6> of entity <xortreestage>.
ERROR:HDLCompiler:806 - "64210386\unary_op_xor_tree_lut6.vhd" Line 105: Syntax
error near "signal".
ERROR:HDLCompiler:40 - "64210386\unary_op_xor_tree_lut6.vhd" Line 105: std_logic
is not a component
ERROR:HDLCompiler:806 - "64210386\unary_op_xor_tree_lut6.vhd" Line 106: Syntax
error near "signal".
ERROR:HDLCompiler:40 - "64210386\unary_op_xor_tree_lut6.vhd" Line 106:
std_logic_vector is not a component
ERROR:HDLCompiler:402 - "64210386\unary_op_xor_tree_lut6.vhd" Line 106: Expected
an architecture identifier in index
ERROR:HDLCompiler:806 - "64210386\unary_op_xor_tree_lut6.vhd" Line 107: Syntax
error near "signal".
ERROR:HDLCompiler:40 - "64210386\unary_op_xor_tree_lut6.vhd" Line 107:
std_logic_vector is not a component
ERROR:HDLCompiler:402 - "64210386\unary_op_xor_tree_lut6.vhd" Line 107: Expected
an architecture identifier in index
ERROR:HDLCompiler:806 - "64210386\unary_op_xor_tree_lut6.vhd" Line 108: Syntax
error near "signal".
ERROR:HDLCompiler:40 - "64210386\unary_op_xor_tree_lut6.vhd" Line 108:
std_logic_vector is not a component
ERROR:HDLCompiler:402 - "64210386\unary_op_xor_tree_lut6.vhd" Line 108: Expected
an architecture identifier in index
ERROR:HDLCompiler:806 - "64210386\unary_op_xor_tree_lut6.vhd" Line 109: Syntax
error near "signal".
ERROR:HDLCompiler:40 - "64210386\unary_op_xor_tree_lut6.vhd" Line 109:
std_logic_vector is not a component
ERROR:HDLCompiler:402 - "64210386\unary_op_xor_tree_lut6.vhd" Line 109: Expected
an architecture identifier in index
ERROR:HDLCompiler:806 - "64210386\unary_op_xor_tree_lut6.vhd" Line 110: Syntax
error near "signal".
ERROR:HDLCompiler:40 - "64210386\unary_op_xor_tree_lut6.vhd" Line 110:
std_logic_vector is not a component
ERROR:HDLCompiler:402 - "64210386\unary_op_xor_tree_lut6.vhd" Line 110: Expected
an architecture identifier in index
ERROR:HDLCompiler:806 - "64210386\unary_op_xor_tree_lut6.vhd" Line 111: Syntax
error near "signal".
ERROR:HDLCompiler:40 - "64210386\unary_op_xor_tree_lut6.vhd" Line 111:
std_logic_vector is not a component
Sorry, too many errors..
-->

```

Total memory usage is 4466696 kilobytes

```

Number of errors : 19 ( 0 filtered)
Number of warnings : 0 ( 0 filtered)
Number of infos : 0 ( 0 filtered)

```

```

64210386>fuse -incremental -o unary_tree_tb_isim_beh.exe -prj unary_tree_tb.prj -
top Unary_Op_Bin_Tree_tb
Running: C:\Xilinx\14.7\ISE_DS\ISE\bin\nt64\unwrapped\fuse.exe -incremental -o
unary_tree_tb_isim_beh.exe -prj unary_tree_tb.prj -top Unary_Op_Bin_Tree_tb
ISim P.20131013 (signature 0x7708f090)
Number of CPUs detected in this system: 8
Turning on mult-threading, number of parallel sub-compilation jobs: 16
Determining compilation order of HDL files
Parsing VHDL file "slv_image_pkg.vhd" into library work

```


Parsing VHDL file "unary_op_xor_tree_lut6.vhd" into library work
Sorry, too many errors..

```
64210386>if exist Unary_Op_Bin_Tree.csv del Unary_Op_Bin_Tree.csv
```

```
64210386>if exist Unary_Op_Bin_Tree_64210386.csv del  
Unary_Op_Bin_Tree_64210386.csv
```

```
64210386>unary_tree_tb_isim_beh.exe -tclbatch isim.tcl -wdb  
unary_tree_tb_isim_beh.wdb
```

```
64210386>rem ren Unary_Op_Bin_Tree.csv Unary_Op_Bin_Tree_64210386.csv
```

```
64210386>xst -ifn unary_vhdl93.xst  
Release 14.7 - xst P.20131013 (nt64)  
Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.  
--> Parameter TMPDIR set to xst/projnav.tmp
```

```
Total REAL time to Xst completion: 0.00 secs  
Total CPU time to Xst completion: 0.24 secs
```

```
--> Parameter xsthdpdir set to xst
```

```
Total REAL time to Xst completion: 0.00 secs  
Total CPU time to Xst completion: 0.24 secs
```

```
-->
```

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 - 8.4.5) Cross Clock Domains Report

```
=====
```

*	Synthesis Options Summary	*
---	---------------------------	---

```
=====
```

---- Source Parameters

```
Input File Name      : "./unary_vhdl93.prj"  
Ignore Synthesis Constraint File : NO
```

---- Target Parameters

```
Output File Name     : "reduction_operators"  
Output Format        : NGC  
Target Device       : xc6slx4-3-tqg144
```

----- Source Options

Top Module Name : reduction_operators
Automatic FSM Extraction : YES
FSM Encoding Algorithm : Auto
Safe Implementation : No
FSM Style : LUT
RAM Extraction : Yes
RAM Style : Auto
ROM Extraction : Yes
Shift Register Extraction : YES
ROM Style : Auto
Resource Sharing : YES
Asynchronous To Synchronous : NO
Shift Register Minimum Size : 2
Use DSP Block : Auto
Automatic Register Balancing : No

----- Target Options

LUT Combining : Auto
Reduce Control Sets : Auto
Add IO Buffers : YES
Global Maximum Fanout : 100000
Add Generic Clock Buffer(BUFG) : 16
Register Duplication : YES
Optimize Instantiated Primitives : NO
Use Clock Enable : Auto
Use Synchronous Set : Auto
Use Synchronous Reset : Auto
Pack IO Registers into IOBs : Auto
Equivalent register Removal : YES

----- General Options

Optimization Goal : Speed
Optimization Effort : 1
Power Reduction : NO
Keep Hierarchy : No
Netlist Hierarchy : As_Optimized
RTL Output : Yes
Global Optimization : AllClockNets
Read Cores : YES
Write Timing Constraints : NO
Cross Clock Analysis : NO
Hierarchy Separator : /
Bus Delimiter : <>
Case Specifier : Maintain
Slice Utilization Ratio : 100
BRAM Utilization Ratio : 100
DSP48 Utilization Ratio : 100
Auto BRAM Packing : NO
Slice Utilization Ratio Delta : 5

=====

=====

```
*          HDL Parsing          *
```

=====

Parsing VHDL file "64210386\unary_operators_vhdl_93.vhd" into library work
Parsing entity <reduction_operators>.

Parsing **architecture** <vhdl_93_process> of **entity** <reduction_operators>.

```
=====
*          HDL Elaboration          *
=====
```

Elaborating **entity** <reduction_operators> (**architecture** <vhdl_93_process>) with
generics from **library** <work>.

```
=====
*          HDL Synthesis            *
=====
```

Synthesizing Unit <reduction_operators>.

Related source **file** is "64210386\unary_operators_vhdl_93.vhd".

N = 64

Summary:

inferred 128 Multiplexer(s).

Unit <reduction_operators> synthesized.

```
=====
HDL Synthesis Report
=====
```

Macro Statistics

```
# Multiplexers          : 128
  1-bit 2-to-1 multiplexer      : 128
# Xors                   : 1
  1-bit xor64                 : 1
```

```
=====
*          Advanced HDL Synthesis    *
=====
```

```
=====
Advanced HDL Synthesis Report
=====
```

Macro Statistics

```
# Multiplexers          : 128
  1-bit 2-to-1 multiplexer      : 128
# Xors                   : 1
  1-bit xor64                 : 1
```

```
=====
*          Low Level Synthesis        *
=====
```

Optimizing unit <reduction_operators> ...

Mapping all equations...

Building and optimizing final netlist ...

Found area constraint ratio of 100 (+ 5) on block reduction_operators, actual
ratio is 1.

Final Macro Processing ...

=====

Final Register Report

Found no macro

=====

=====

* Partition Report *

=====

Partition Implementation Status

No Partitions were found in this design.

=====

* Design Summary *

=====

Top Level Output File Name : reduction_operators.ngc

Primitive and Black Box Usage:

```
# BELS      : 59
# GND       : 1
# LUT4      : 3
# LUT6      : 32
# MUXCY     : 22
# VCC       : 1
# IO Buffers : 67
# IBUF      : 64
# OBUF      : 3
```

Device utilization summary:

Selected Device : 6slx4tqg144-3

Slice Logic Utilization:

```
Number of Slice LUTs:    35 out of 2400 1%
Number used as Logic:    35 out of 2400 1%
```

Slice Logic Distribution:

```
Number of LUT Flip Flop pairs used: 35
Number with an unused Flip Flop: 35 out of 35 100%
Number with an unused LUT: 0 out of 35 0%
Number of fully used LUT-FF pairs: 0 out of 35 0%
Number of unique control sets: 0
```

IO Utilization:

```
Number of IOs: 67
Number of bonded IOBs: 67 out of 102 65%
```

Specific Feature Utilization:

Partition Resource Summary:

No Partitions were found in this design.

=====
Timing Report

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.
FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT
GENERATED AFTER PLACE-and-ROUTE.

Clock Information:

No clock signals found in this design

Asynchronous Control Signals Information:

No asynchronous control signals found in this design

Timing Summary:

Speed Grade: -3

Minimum period: No path found
Minimum input arrival time before clock: No path found
Maximum output required time after clock: No path found
Maximum combinational path delay: 7.522ns

Timing Details:

All values displayed in nanoseconds (ns)

=====
Timing constraint: Default path analysis

Total number of paths / destination ports: 192 / 3

Delay: 7.522ns (Levels of Logic = 5)

Source: A<22> (PAD)

Destination: reduced_XOR (PAD)

Data Path: A<22> to reduced_XOR

Gate Net

Cell:in->out fanout Delay Delay Logical Name (Net Name)

IBUF:I->O 3 1.222 1.015 A_22_IBUF (A_22_IBUF)
LUT6:I0->O 1 0.203 0.944 Mxor_reduced_XOR_xo<0>3 (Mxor_reduced_XOR_xo<0>2)
LUT6:I0->O 1 0.203 0.580 Mxor_reduced_XOR_xo<0>14_SW0 (N01)
LUT6:I5->O 1 0.205 0.579 Mxor_reduced_XOR_xo<0>14 (reduced_XOR_OBUF)
OBUF:I->O 2.571 reduced_XOR_OBUF (reduced_XOR)

Total 7.522ns (4.404ns logic, 3.118ns route)
(58.5% logic, 41.5% route)

=====
Cross Clock Domains Report:

=====
Total REAL time to Xst completion: 10.00 secs
Total CPU time to Xst completion: 10.44 secs

-->

Total memory usage is 4487516 kilobytes

Number of errors : 0 (0 filtered)
Number of warnings : 0 (0 filtered)
Number of infos : 0 (0 filtered)

64210386>fuse -incremental -o unary_vhdl93_tb_isim_beh.exe -prj
unary_vhdl93_tb.prj -top reduction_operators_tb
Running: C:\Xilinx\14.7\ISE_DS\ISE\bin\nt64\unwrapped\fuse.exe -incremental -o
unary_vhdl93_tb_isim_beh.exe -prj unary_vhdl93_tb.prj -top reduction_operators_tb
ISim P.20131013 (signature 0x7708f090)
Number of CPUs detected in this system: 8
Turning on mult-threading, number of parallel sub-compilation jobs: 16
Determining compilation order of HDL files
Parsing VHDL file "unary_operators_vhdl_93.vhd" into library work
Parsing VHDL file "unary_operators_vhdl93_IDEAL_tb.vhd" into library work
Starting static elaboration
Completed static elaboration
Compiling package standard
Compiling package std_logic_1164
Compiling package numeric_std
Compiling package textio
Compiling package std_logic_textio
Compiling architecture vhdl_93_process of entity reduction_operators
[\reduction_operators(3)\]
Compiling architecture test of entity reduction_operators_tb
Time Resolution for simulation is 1ps.
Compiled 8 VHDL Units
Built simulation executable unary_vhdl93_tb_isim_beh.exe
Fuse Memory Usage: 36752 KB
Fuse CPU Usage: 828 ms

64210386>if exist reduction_operators.csv del reduction_operators.csv

64210386>if exist reduction_operators_64210386.csv del
reduction_operators_64210386.csv

64210386>unary_vhdl93_tb_isim_beh.exe -tclbatch isim.tcl -wdb
unary_vhdl93_tb_isim_beh.wdb
ISim P.20131013 (signature 0x7708f090)
WARNING: A WEBPACK license was found.
WARNING: Please use Xilinx License Configuration Manager to check out a full ISim
license.
WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for
more information on the differences between the Lite and the Full version.
This is a Lite version of ISim.
Time resolution is 1 ps
Simulator is doing circuit initialization process.
Finished circuit initialization process.

64210386>rem ren reduction_operators.csv reduction_operators_64210386.csv


```
-- *****
-- **** STUDENT: 64210445
-- *****
-- KOMENTARJI K OCENI NALOGE
-- Matej Možek: Ni pripomb
-- *****
```

```
64210445>if not exist "xst" mkdir xst
```

```
64210445>cd XST
```

```
64210445\xst>if not exist "projnav.tmp" mkdir "projnav.tmp"
```

```
64210445\xst>cd ..
```

```
64210445>xst -ifn unary_tree.xst
Release 14.7 - xst P.20131013 (nt64)
Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.
--> Parameter TMPDIR set to xst/projnav.tmp
```

```
Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.26 secs
```

```
--> Parameter xsthdpdir set to xst
```

```
Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.26 secs
```

```
-->
```

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 - 8.4.3) Timing Summary
 - 8.4.4) Timing Details
 - 8.4.5) Cross Clock Domains Report

```
=====
*      Synthesis Options Summary      *
=====
```

---- Source Parameters

```
Input File Name      : "unary_tree.prj"
Ignore Synthesis Constraint File : NO
```

---- Target Parameters

```
Output File Name     : "Unary_Op_Bin_Tree"
```


Output Format : NGC
Target Device : xc6slx4-3-tqg144

----- Source Options

Top Module Name : Unary_Op_Bin_Tree
Automatic FSM Extraction : YES
FSM Encoding Algorithm : Auto
Safe Implementation : No
FSM Style : LUT
RAM Extraction : Yes
RAM Style : Auto
ROM Extraction : Yes
Shift Register Extraction : YES
ROM Style : Auto
Resource Sharing : YES
Asynchronous To Synchronous : NO
Shift Register Minimum Size : 2
Use DSP Block : Auto
Automatic Register Balancing : No

----- Target Options

LUT Combining : Auto
Reduce Control Sets : Auto
Add IO Buffers : YES
Global Maximum Fanout : 100000
Add Generic Clock Buffer(BUFG) : 16
Register Duplication : YES
Optimize Instantiated Primitives : NO
Use Clock Enable : Auto
Use Synchronous Set : Auto
Use Synchronous Reset : Auto
Pack IO Registers into IOBs : Auto
Equivalent register Removal : YES

----- General Options

Optimization Goal : Speed
Optimization Effort : 1
Power Reduction : NO
Keep Hierarchy : No
Netlist Hierarchy : As_Optimized
RTL Output : Yes
Global Optimization : AllClockNets
Read Cores : YES
Write Timing Constraints : NO
Cross Clock Analysis : NO
Hierarchy Separator : /
Bus Delimiter : <>
Case Specifier : Maintain
Slice Utilization Ratio : 100
BRAM Utilization Ratio : 100
DSP48 Utilization Ratio : 100
Auto BRAM Packing : NO
Slice Utilization Ratio Delta : 5

=====

=====

* HDL Parsing *

=====

Parsing VHDL file "64210445\unary_op_xor_tree_lut6.vhd" into library work
Parsing entity <XorTreeStage>.
Parsing architecture <tree_of_xor_lut6> of entity <xortreestage>.
Parsing VHDL file "64210445\unary_op_tree.vhd" into library work
Parsing entity <Unary_Op_Bin_Tree>.
Parsing architecture <t> of entity <unary_op_bin_tree>.

```
=====
*           HDL Elaboration           *
=====
```

Elaborating entity <Unary_Op_Bin_Tree> (architecture <t>) with generics from library <work>.

Elaborating entity <XorTreeStage> (architecture <tree_of_xor_lut6>) with generics from library <work>.

Elaborating entity <XorTreeStage> (architecture <tree_of_xor_lut6>) with generics from library <work>.

Elaborating entity <XorTreeStage> (architecture <tree_of_xor_lut6>) with generics from library <work>.

Elaborating entity <XorTreeStage> (architecture <tree_of_xor_lut6>) with generics from library <work>.

Elaborating entity <XorTreeStage> (architecture <tree_of_xor_lut6>) with generics from library <work>.

Elaborating entity <XorTreeStage> (architecture <tree_of_xor_lut6>) with generics from library <work>.

Elaborating entity <XorTreeStage> (architecture <tree_of_xor_lut6>) with generics from library <work>.

Elaborating entity <XorTreeStage> (architecture <tree_of_xor_lut6>) with generics from library <work>.

Elaborating entity <XorTreeStage> (architecture <tree_of_xor_lut6>) with generics from library <work>.

Elaborating entity <XorTreeStage> (architecture <tree_of_xor_lut6>) with generics from library <work>.

Elaborating entity <XorTreeStage> (architecture <tree_of_xor_lut6>) with generics from library <work>.

```
=====
*           HDL Synthesis             *
=====
```

Synthesizing Unit <Unary_Op_Bin_Tree>.
Related source file is "64210445\unary_op_tree.vhd".
N = 4096
Summary:
no macro.
Unit <Unary_Op_Bin_Tree> synthesized.

Synthesizing Unit <XorTreeStage_1>.

Related source file is "64210445\unary_op_xor_tree_lut6.vhd".
N = 4096
Summary:
no macro.
Unit <XorTreeStage_1> synthesized.

Synthesizing Unit <XorTreeStage_2>.
Related source file is "64210445\unary_op_xor_tree_lut6.vhd".
N = 682
Summary:
no macro.
Unit <XorTreeStage_2> synthesized.

Synthesizing Unit <XorTreeStage_3>.
Related source file is "64210445\unary_op_xor_tree_lut6.vhd".
N = 113
Summary:
no macro.
Unit <XorTreeStage_3> synthesized.

Synthesizing Unit <XorTreeStage_4>.
Related source file is "64210445\unary_op_xor_tree_lut6.vhd".
N = 18
Summary:
no macro.
Unit <XorTreeStage_4> synthesized.

Synthesizing Unit <XorTreeStage_5>.
Related source file is "64210445\unary_op_xor_tree_lut6.vhd".
N = 3
Summary:
no macro.
Unit <XorTreeStage_5> synthesized.

Synthesizing Unit <XorTreeStage_6>.
Related source file is "64210445\unary_op_xor_tree_lut6.vhd".
N = 19
Summary:
no macro.
Unit <XorTreeStage_6> synthesized.

Synthesizing Unit <XorTreeStage_7>.
Related source file is "64210445\unary_op_xor_tree_lut6.vhd".
N = 4
Summary:
no macro.
Unit <XorTreeStage_7> synthesized.

Synthesizing Unit <XorTreeStage_8>.
Related source file is "64210445\unary_op_xor_tree_lut6.vhd".
N = 20
Summary:
no macro.
Unit <XorTreeStage_8> synthesized.

Synthesizing Unit <XorTreeStage_9>.
Related source file is "64210445\unary_op_xor_tree_lut6.vhd".
N = 114
Summary:

no macro.
Unit <XorTreeStage_9> synthesized.

Synthesizing Unit <XorTreeStage_10>.
Related source file is "64210445\unary_op_xor_tree_lut6.vhd".
N = 683
Summary:
no macro.

Unit <XorTreeStage_10> synthesized.

Synthesizing Unit <XorTreeStage_11>.
Related source file is "64210445\unary_op_xor_tree_lut6.vhd".
N = 115
Summary:
no macro.

Unit <XorTreeStage_11> synthesized.

=====
HDL Synthesis Report

Found no macro
=====

=====
* Advanced HDL Synthesis *
=====

=====
Advanced HDL Synthesis Report

Found no macro
=====

=====
* Low Level Synthesis *
=====

Optimizing unit <Unary_Op_Bin_Tree> ...

Mapping all equations...
Building and optimizing final netlist ...
Found area constraint ratio of 100 (+ 5) on block Unary_Op_Bin_Tree, actual ratio is 94.

Final Macro Processing ...

=====
Final Register Report

Found no macro
=====

=====
* Partition Report *
=====

Partition Implementation Status

No Partitions were found in this design.

=====

*	Design Summary	*
---	----------------	---

=====

Top Level Output File Name : Unary_Op_Bin_Tree.ngc

Primitive and Black Box Usage:

BELS : 1556
GND : 1
LUT6 : 1555
IO Buffers : 4097
IBUF : 4096
OBUF : 1

Device utilization summary:

Selected Device : 6slx4tqg144-3

Slice Logic Utilization:

Number of Slice LUTs: 1555 out of 2400 64%
Number used as Logic: 1555 out of 2400 64%

Slice Logic Distribution:

Number of LUT Flip Flop pairs used: 1555
Number with an unused Flip Flop: 1555 out of 1555 100%
Number with an unused LUT: 0 out of 1555 0%
Number of fully used LUT-FF pairs: 0 out of 1555 0%
Number of unique control sets: 0

IO Utilization:

Number of IOs: 4097
Number of bonded IOBs: 4097 out of 102 4016% (*)

Specific Feature Utilization:

WARNING:Xst:1336 - (*) More than 100% of Device resources are used

Partition Resource Summary:

No Partitions were found in this design.

=====

Timing Report

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.

FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT
GENERATED AFTER PLACE-and-ROUTE.

Clock Information:

No clock signals found in this design

Asynchronous Control Signals Information:

No asynchronous control signals found in this design

Timing Summary:

Speed Grade: -3

Minimum period: No path found
Minimum input arrival time before clock: No path found
Maximum output required time after clock: No path found
Maximum combinational path delay: 10.106ns

Timing Details:

All values displayed in nanoseconds (ns)

=====

Timing constraint: Default path analysis
Total number of paths / destination ports: 4096 / 1

Delay: 10.106ns (Levels of Logic = 7)
Source: I<0> (PAD)
Destination: O_Xor (PAD)

Data Path: I<0> to O_Xor

Gate Net

Cell:in->out fanout Delay Delay Logical Name (Net Name)

IBUF:I->0 1 1.222 0.944 I_0_IBUF (I_0_IBUF)
LUT6:I0->0 1 0.203 0.944
U_Xor/Stages.Six1/Stages.Six1/Stages.Six1/Stages.Six1/Stage_xor_3.XOR6_LUT
(U_Xor/Stages.Six1/Stages.Six1/Stages.Six1/Stages.Sixth1_in)
LUT6:I0->0 1 0.203 0.944
U_Xor/Stages.Six1/Stages.Six1/Stages.Six1/Stages.XOR6_LUT
(U_Xor/Stages.Six1/Stages.Six1/Stages.Sixth1_in)
LUT6:I0->0 1 0.203 0.944 U_Xor/Stages.Six1/Stages.Six1/Stages.XOR6_LUT
(U_Xor/Stages.Six1/Stages.Sixth1_in)
LUT6:I0->0 1 0.203 0.944 U_Xor/Stages.Six1/Stages.XOR6_LUT
(U_Xor/Stages.Sixth1_in)
LUT6:I0->0 1 0.203 0.579 U_Xor/Stages.XOR6_LUT (O_Xor_OBUF)
OBUF:I->0 2.571 O_Xor_OBUF (O_Xor)

Total 10.106ns (4.808ns logic, 5.298ns route)
(47.6% logic, 52.4% route)

Cross Clock Domains Report:

=====

Total REAL time to Xst completion: 18.00 secs
Total CPU time to Xst completion: 18.14 secs

-->

Total memory usage is 4539588 kilobytes

Number of errors : 0 (0 filtered)

Number of warnings : 1 (0 filtered)

Number of infos : 0 (0 filtered)

64210445>fuse -incremental -o unary_tree_tb_isim_beh.exe -prj unary_tree_tb.prj -top Unary_Op_Bin_Tree_tb

Running: C:\Xilinx\14.7\ISE_DS\ISE\bin\nt64\unwrapped\fuse.exe -incremental -o unary_tree_tb_isim_beh.exe -prj unary_tree_tb.prj -top Unary_Op_Bin_Tree_tb

ISim P.20131013 (signature 0x7708f090)

Number of CPUs detected in this system: 8

Turning on mult-threading, number of parallel sub-compilation jobs: 16

Determining compilation order of HDL files

Parsing VHDL file "slv_image_pkg.vhd" into library work

Parsing VHDL file "unary_op_xor_tree_lut6.vhd" into library work

Parsing VHDL file "unary_op_tree.vhd" into library work

Parsing VHDL file "unary_op_tree_IDEAL_tb.vhd" into library work

Starting static elaboration

Completed static elaboration

Compiling package standard

Compiling package std_logic_1164

Compiling package numeric_std

Compiling package textio

Compiling package std_logic_textio

Compiling package slv_image_pkg

Compiling package vcomponents

Compiling package vital_timing

Compiling package vital_primitives

Compiling package vpkg

Compiling architecture lut6_v of entity LUT6 [\LUT6("0110100110010110100101100...)]

Compiling architecture tree_of_xor_lut6 of entity XorTreeStage [\XorTreeStage(2)\]

Compiling architecture tree_of_xor_lut6 of entity XorTreeStage [\XorTreeStage(3)\]

Compiling architecture tree_of_xor_lut6 of entity XorTreeStage

[\XorTreeStage(16)\]

Compiling architecture t of entity Unary_Op_Bin_Tree [\Unary_Op_Bin_Tree(16)\]

Compiling architecture test of entity unary_op_bin_tree_tb

Time Resolution for simulation is 1ps.

Waiting for 1 sub-compilation(s) to finish...

Compiled 21 VHDL Units

Built simulation executable unary_tree_tb_isim_beh.exe

Fuse Memory Usage: 59624 KB

Fuse CPU Usage: 1359 ms

64210445>if exist Unary_Op_Bin_Tree.csv del Unary_Op_Bin_Tree.csv

64210445>if exist Unary_Op_Bin_Tree_64210445.csv del

Unary_Op_Bin_Tree_64210445.csv

64210445>unary_tree_tb_isim_beh.exe -tclbatch isim.tcl -wdb

unary_tree_tb_isim_beh.wdb

ISim P.20131013 (signature 0x7708f090)

WARNING: A WEBPACK license was found.

WARNING: Please use Xilinx License Configuration Manager to check out a full ISim license.

WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for more information on the differences between the Lite and the Full version.

This is a Lite version of ISim.
Time resolution is 1 ps
Simulator is doing circuit initialization process.
Finished circuit initialization process.

```
64210445>rem ren Unary_Op_Bin_Tree.csv Unary_Op_Bin_Tree_64210445.csv
```

```
64210445>xst -ifn unary_vhdl93.xst
Release 14.7 - xst P.20131013 (nt64)
Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.
--> Parameter TMPDIR set to xst/projnav.tmp
```

```
Total REAL time to Xst completion: 1.00 secs
Total CPU time to Xst completion: 0.26 secs
```

```
--> Parameter xsthdpdir set to xst
```

```
Total REAL time to Xst completion: 1.00 secs
Total CPU time to Xst completion: 0.26 secs
```

```
-->
```

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```
=====
*      Synthesis Options Summary      *
```

----- Source Parameters

```
Input File Name      : "./unary_vhdl93.prj"
Ignore Synthesis Constraint File : NO
```

----- Target Parameters

```
Output File Name     : "reduction_operators"
Output Format         : NGC
Target Device        : xc6slx4-3-tqg144
```

----- Source Options

```
Top Module Name      : reduction_operators
Automatic FSM Extraction : YES
FSM Encoding Algorithm : Auto
Safe Implementation   : No
```


FSM Style : LUT
RAM Extraction : Yes
RAM Style : Auto
ROM Extraction : Yes
Shift Register Extraction : YES
ROM Style : Auto
Resource Sharing : YES
Asynchronous To Synchronous : NO
Shift Register Minimum Size : 2
Use DSP Block : Auto
Automatic Register Balancing : No

---- Target Options

LUT Combining : Auto
Reduce Control Sets : Auto
Add IO Buffers : YES
Global Maximum Fanout : 100000
Add Generic Clock Buffer(BUFG) : 16
Register Duplication : YES
Optimize Instantiated Primitives : NO
Use Clock Enable : Auto
Use Synchronous Set : Auto
Use Synchronous Reset : Auto
Pack IO Registers into IOBs : Auto
Equivalent register Removal : YES

---- General Options

Optimization Goal : Speed
Optimization Effort : 1
Power Reduction : NO
Keep Hierarchy : No
Netlist Hierarchy : As_Optimized
RTL Output : Yes
Global Optimization : AllClockNets
Read Cores : YES
Write Timing Constraints : NO
Cross Clock Analysis : NO
Hierarchy Separator : /
Bus Delimiter : <>
Case Specifier : Maintain
Slice Utilization Ratio : 100
BRAM Utilization Ratio : 100
DSP48 Utilization Ratio : 100
Auto BRAM Packing : NO
Slice Utilization Ratio Delta : 5

=====

=====

* HDL Parsing *

=====

Parsing VHDL file "64210445\unary_operators_vhdl_93.vhd" into library work
Parsing entity <reduction_operators>.
Parsing architecture <vhdl_93_process> of entity <reduction_operators>.

=====

* HDL Elaboration *

=====

Elaborating entity <reduction_operators> (architecture <vhd1_93_process>) with generics from library <work>.

```
=====
*      HDL Synthesis      *
=====
```

Synthesizing Unit <reduction_operators>.

Related source file is "64210445\unary_operators_vhd1_93.vhd".

N = 64

Summary:

inferred 128 Multiplexer(s).

Unit <reduction_operators> synthesized.

```
=====
HDL Synthesis Report
```

Macro Statistics

```
# Multiplexers      : 128
  1-bit 2-to-1 multiplexer      : 128
# Xors              : 1
  1-bit xor64              : 1
```

```
=====
*      Advanced HDL Synthesis      *
=====
```

```
=====
Advanced HDL Synthesis Report
```

Macro Statistics

```
# Multiplexers      : 128
  1-bit 2-to-1 multiplexer      : 128
# Xors              : 1
  1-bit xor64              : 1
```

```
=====
*      Low Level Synthesis      *
=====
```

Optimizing unit <reduction_operators> ...

Mapping all equations...

Building and optimizing final netlist ...

Found area constraint ratio of 100 (+ 5) on block reduction_operators, actual ratio is 1.

Final Macro Processing ...

```
=====
Final Register Report
```

Found no macro

```
=====
```

```
=====
*      Partition Report      *
=====
```

Partition Implementation Status

No Partitions were found in this design.

```
=====
*      Design Summary      *
=====
```

Top Level Output File Name : reduction_operators.ngc

Primitive and Black Box Usage:

```
# BELS      : 59
# GND       : 1
# LUT4      : 3
# LUT6      : 32
# MUXCY     : 22
# VCC       : 1
# IO Buffers : 67
# IBUF      : 64
# OBUF      : 3
```

Device utilization summary:

Selected Device : 6slx4tqg144-3

Slice Logic Utilization:

```
Number of Slice LUTs:      35 out of 2400 1%
Number used as Logic:      35 out of 2400 1%
```

Slice Logic Distribution:

```
Number of LUT Flip Flop pairs used: 35
Number with an unused Flip Flop: 35 out of 35 100%
Number with an unused LUT: 0 out of 35 0%
Number of fully used LUT-FF pairs: 0 out of 35 0%
Number of unique control sets: 0
```

IO Utilization:

```
Number of IOs: 67
Number of bonded IOBs: 67 out of 102 65%
```

Specific Feature Utilization:

Partition Resource Summary:

No Partitions were found in this design.

=====

Timing Report

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.
FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT
GENERATED AFTER PLACE-and-ROUTE.

Clock Information:

No clock signals found in this design

Asynchronous Control Signals Information:

No asynchronous control signals found in this design

Timing Summary:

Speed Grade: -3

Minimum period: No path found
Minimum input arrival time before clock: No path found
Maximum output required time after clock: No path found
Maximum combinational path delay: 7.522ns

Timing Details:

All values displayed in nanoseconds (ns)

=====

Timing constraint: Default path analysis

Total number of paths / destination ports: 192 / 3

Delay: 7.522ns (Levels of Logic = 5)

Source: A<22> (PAD)

Destination: reduced_XOR (PAD)

Data Path: A<22> to reduced_XOR

Gate Net

Cell:in->out fanout Delay Delay Logical Name (Net Name)

IBUF:I->O 3 1.222 1.015 A_22_IBUF (A_22_IBUF)
LUT6:I0->O 1 0.203 0.944 Mxor_reduced_XOR_xo<0>3 (Mxor_reduced_XOR_xo<0>2)
LUT6:I0->O 1 0.203 0.580 Mxor_reduced_XOR_xo<0>14_SW0 (N01)
LUT6:I5->O 1 0.205 0.579 Mxor_reduced_XOR_xo<0>14 (reduced_XOR_OBUF)
OBUF:I->O 2.571 reduced_XOR_OBUF (reduced_XOR)

Total 7.522ns (4.404ns logic, 3.118ns route)
(58.5% logic, 41.5% route)

=====

Cross Clock Domains Report:

Total REAL time to Xst completion: 10.00 secs

Total CPU time to Xst completion: 9.93 secs

-->

Total memory usage is 4487516 kilobytes

Number of errors : 0 (0 filtered)

Number of warnings : 0 (0 filtered)

Number of infos : 0 (0 filtered)

```
64210445>fuse -incremental -o unary_vhdl93_tb_isim_beh.exe -prj
unary_vhdl93_tb.prj -top reduction_operators_tb
Running: C:\Xilinx\14.7\ISE_DS\ISE\bin\nt64\unwrapped\fuse.exe -incremental -o
unary_vhdl93_tb_isim_beh.exe -prj unary_vhdl93_tb.prj -top reduction_operators_tb
ISim P.20131013 (signature 0x7708f090)
Number of CPUs detected in this system: 8
Turning on mult-threading, number of parallel sub-compilation jobs: 16
Determining compilation order of HDL files
Parsing VHDL file "unary_operators_vhdl_93.vhd" into library work
Parsing VHDL file "unary_operators_vhdl93_IDEAL_tb.vhd" into library work
Starting static elaboration
Completed static elaboration
Compiling package standard
Compiling package std_logic_1164
Compiling package numeric_std
Compiling package textio
Compiling package std_logic_textio
Compiling architecture vhdl_93_process of entity reduction_operators
[\reduction_operators(3)\]
Compiling architecture test of entity reduction_operators_tb
Time Resolution for simulation is 1ps.
Waiting for 1 sub-compilation(s) to finish...
Compiled 8 VHDL Units
Built simulation executable unary_vhdl93_tb_isim_beh.exe
Fuse Memory Usage: 37240 KB
Fuse CPU Usage: 874 ms
```

```
64210445>if exist reduction_operators.csv del reduction_operators.csv
```

```
64210445>if exist reduction_operators_64210445.csv del
reduction_operators_64210445.csv
```

```
64210445>unary_vhdl93_tb_isim_beh.exe -tclbatch isim.tcl -wdb
unary_vhdl93_tb_isim_beh.wdb
ISim P.20131013 (signature 0x7708f090)
WARNING: A WEBPACK license was found.
WARNING: Please use Xilinx License Configuration Manager to check out a full ISim
license.
WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for
more information on the differences between the Lite and the Full version.
This is a Lite version of ISim.
Time resolution is 1 ps
Simulator is doing circuit initialization process.
Finished circuit initialization process.
```

```
64210445>rem ren reduction_operators.csv reduction_operators_64210445.csv
```

```
-- *****
-- **** STUDENT: 64210455
-- *****
-- KOMENTARJI K OCENI NALOGE
-- Matej Možek: Ni pripomb
-- *****
```

```
64210455>if not exist "xst" mkdir xst
```

```
64210455>cd XST
```

```
64210455\xst>if not exist "projnav.tmp" mkdir "projnav.tmp"
```

```
64210455\xst>cd ..
```

```
64210455>xst -ifn unary_tree.xst
Release 14.7 - xst P.20131013 (nt64)
Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.
--> Parameter TMPDIR set to xst/projnav.tmp
```

```
Total REAL time to Xst completion: 0.00 secs
```

```
Total CPU time to Xst completion: 0.26 secs
```

```
--> Parameter xsthdpdir set to xst
```

```
Total REAL time to Xst completion: 1.00 secs
```

```
Total CPU time to Xst completion: 0.58 secs
```

```
-->
```

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```
=====
*      Synthesis Options Summary      *
=====
```

---- Source Parameters

```
Input File Name      : "unary_tree.prj"
Ignore Synthesis Constraint File : NO
```

---- Target Parameters

```
Output File Name     : "Unary_Op_Bin_Tree"
```

Output Format : NGC
Target Device : xc6slx4-3-tqg144

----- Source Options

Top Module Name : Unary_Op_Bin_Tree
Automatic FSM Extraction : YES
FSM Encoding Algorithm : Auto
Safe Implementation : No
FSM Style : LUT
RAM Extraction : Yes
RAM Style : Auto
ROM Extraction : Yes
Shift Register Extraction : YES
ROM Style : Auto
Resource Sharing : YES
Asynchronous To Synchronous : NO
Shift Register Minimum Size : 2
Use DSP Block : Auto
Automatic Register Balancing : No

----- Target Options

LUT Combining : Auto
Reduce Control Sets : Auto
Add IO Buffers : YES
Global Maximum Fanout : 100000
Add Generic Clock Buffer(BUFG) : 16
Register Duplication : YES
Optimize Instantiated Primitives : NO
Use Clock Enable : Auto
Use Synchronous Set : Auto
Use Synchronous Reset : Auto
Pack IO Registers into IOBs : Auto
Equivalent register Removal : YES

----- General Options

Optimization Goal : Speed
Optimization Effort : 1
Power Reduction : NO
Keep Hierarchy : No
Netlist Hierarchy : As_Optimized
RTL Output : Yes
Global Optimization : AllClockNets
Read Cores : YES
Write Timing Constraints : NO
Cross Clock Analysis : NO
Hierarchy Separator : /
Bus Delimiter : <>
Case Specifier : Maintain
Slice Utilization Ratio : 100
BRAM Utilization Ratio : 100
DSP48 Utilization Ratio : 100
Auto BRAM Packing : NO
Slice Utilization Ratio Delta : 5

=====

=====

* HDL Parsing *

=====

Parsing VHDL file "64210455\unary_op_xor_tree_lut6.vhd" into library work
Parsing entity <XorTreeStage>.
Parsing architecture <tree_of_xor_lut6> of entity <xortreestage>.
Parsing VHDL file "64210455\unary_op_tree.vhd" into library work
Parsing entity <Unary_Op_Bin_Tree>.
Parsing architecture <t> of entity <unary_op_bin_tree>.

```
=====
*          HDL Elaboration          *
=====
```

Elaborating entity <Unary_Op_Bin_Tree> (architecture <t>) with generics from library <work>.

Elaborating entity <XorTreeStage> (architecture <tree_of_xor_lut6>) with generics from library <work>.

Elaborating entity <XorTreeStage> (architecture <tree_of_xor_lut6>) with generics from library <work>.

Elaborating entity <XorTreeStage> (architecture <tree_of_xor_lut6>) with generics from library <work>.

Elaborating entity <XorTreeStage> (architecture <tree_of_xor_lut6>) with generics from library <work>.

Elaborating entity <XorTreeStage> (architecture <tree_of_xor_lut6>) with generics from library <work>.

Elaborating entity <XorTreeStage> (architecture <tree_of_xor_lut6>) with generics from library <work>.

Elaborating entity <XorTreeStage> (architecture <tree_of_xor_lut6>) with generics from library <work>.

Elaborating entity <XorTreeStage> (architecture <tree_of_xor_lut6>) with generics from library <work>.

Elaborating entity <XorTreeStage> (architecture <tree_of_xor_lut6>) with generics from library <work>.

```
=====
*          HDL Synthesis            *
=====
```

Synthesizing Unit <Unary_Op_Bin_Tree>.
Related source file is "64210455\unary_op_tree.vhd".
N = 4096
Summary:
no macro.
Unit <Unary_Op_Bin_Tree> synthesized.

Synthesizing Unit <XorTreeStage_1>.
Related source file is "64210455\unary_op_xor_tree_lut6.vhd".
N = 4096
Summary:
no macro.
Unit <XorTreeStage_1> synthesized.

Synthesizing Unit <XorTreeStage_2>.
Related source file is "64210455\unary_op_xor_tree_lut6.vhd".
N = 683
Summary:
no macro.
Unit <XorTreeStage_2> synthesized.

Synthesizing Unit <XorTreeStage_3>.
Related source file is "64210455\unary_op_xor_tree_lut6.vhd".
N = 114
Summary:
no macro.
Unit <XorTreeStage_3> synthesized.

Synthesizing Unit <XorTreeStage_4>.
Related source file is "64210455\unary_op_xor_tree_lut6.vhd".
N = 19
Summary:
no macro.
Unit <XorTreeStage_4> synthesized.

Synthesizing Unit <XorTreeStage_5>.
Related source file is "64210455\unary_op_xor_tree_lut6.vhd".
N = 4
Summary:
no macro.
Unit <XorTreeStage_5> synthesized.

Synthesizing Unit <XorTreeStage_6>.
Related source file is "64210455\unary_op_xor_tree_lut6.vhd".
N = 3
Summary:
no macro.
Unit <XorTreeStage_6> synthesized.

Synthesizing Unit <XorTreeStage_7>.
Related source file is "64210455\unary_op_xor_tree_lut6.vhd".
N = 113
Summary:
no macro.
Unit <XorTreeStage_7> synthesized.

Synthesizing Unit <XorTreeStage_8>.
Related source file is "64210455\unary_op_xor_tree_lut6.vhd".
N = 18
Summary:
no macro.
Unit <XorTreeStage_8> synthesized.

Synthesizing Unit <XorTreeStage_9>.
Related source file is "64210455\unary_op_xor_tree_lut6.vhd".
N = 682
Summary:
no macro.
Unit <XorTreeStage_9> synthesized.

=====
HDL Synthesis Report

Found no macro

```
=====
*      Advanced HDL Synthesis      *
```

```
=====
Advanced HDL Synthesis Report
```

Found no macro

```
=====
*      Low Level Synthesis      *
```

Optimizing unit <Unary_Op_Bin_Tree> ...

Mapping all equations...

Building and optimizing final netlist ...

Found area constraint ratio of 100 (+ 5) on block Unary_Op_Bin_Tree, actual ratio is 94.

Final Macro Processing ...

```
=====
Final Register Report
```

Found no macro

```
=====
*      Partition Report      *
```

Partition Implementation Status

No Partitions were found in this design.

```
=====
*      Design Summary      *
```

Top Level Output File Name : Unary_Op_Bin_Tree.ngc

Primitive and Black Box Usage:

BELS : 1555
LUT3 : 1088
LUT4 : 208
LUT6 : 259
IO Buffers : 4097
IBUF : 4096
OBUF : 1

Device utilization summary:

Selected Device : 6slx4tqg144-3

Slice Logic Utilization:

Number of Slice LUTs: 1555 out of 2400 64%
Number used as Logic: 1555 out of 2400 64%

Slice Logic Distribution:

Number of LUT Flip Flop pairs used: 1555
Number with an unused Flip Flop: 1555 out of 1555 100%
Number with an unused LUT: 0 out of 1555 0%
Number of fully used LUT-FF pairs: 0 out of 1555 0%
Number of unique control sets: 0

IO Utilization:

Number of IOs: 4097
Number of bonded IOBs: 4097 out of 102 4016% (*)

Specific Feature Utilization:

WARNING:Xst:1336 - (*) More than 100% of Device resources are used

Partition Resource Summary:

No Partitions were found in this design.

=====

Timing Report

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.
FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT
GENERATED AFTER PLACE-and-ROUTE.

Clock Information:

No clock signals found in this design

Asynchronous Control Signals Information:

No asynchronous control signals found in this design

Timing Summary:

Speed Grade: -3

Minimum period: No path found
Minimum input arrival time before clock: No path found
Maximum output required time after clock: No path found
Maximum combinational path delay: 10.106ns

Timing Details:

All values displayed in nanoseconds (ns)

```

=====
Timing constraint: Default path analysis
Total number of paths / destination ports: 4096 / 1
-----
Delay:      10.106ns (Levels of Logic = 7)
Source:     I<4092> (PAD)
Destination: O_Xor (PAD)

Data Path: I<4092> to O_Xor
Gate Net
Cell:in->out fanout Delay Delay Logical Name (Net Name)
-----
IBUF:I->O      1 1.222 0.827 I_4092_IBUF (I_4092_IBUF)
LUT4:I0->O     1 0.320 0.944
U_Xor/MultiStage.XOR_Stage1/MultiStage.XOR_Stage1/MultiStage
.XOR_Stage1/Quad_Input.LUT4_XOR
(U_Xor/MultiStage.XOR_Stage1/MultiStage.XOR_Stage1/MultiStage.XOR_Stage1/MultiStage.Xor_1)
LUT6:I0->O     1 0.203 0.944
U_Xor/MultiStage.XOR_Stage1/MultiStage.XOR_Stage1/MultiStage.XOR_Stage1/MultiStage
.Final_XOR_LUT6
(U_Xor/MultiStage.XOR_Stage1/MultiStage.XOR_Stage1/MultiStage.Xor_1)
LUT6:I0->O     1 0.203 0.944
U_Xor/MultiStage.XOR_Stage1/MultiStage.XOR_Stage1/MultiStage.Final_XOR_LUT6
(U_Xor/MultiStage.XOR_Stage1/MultiStage.Xor_1)
LUT6:I0->O     1 0.203 0.944 U_Xor/MultiStage.XOR_Stage1/MultiStage.Final_XOR_LUT6
(U_Xor/MultiStage.Xor_1)
LUT6:I0->O     1 0.203 0.579 U_Xor/MultiStage.Final_XOR_LUT6 (O_Xor_OBUF)
OBUF:I->O      2.571  O_Xor_OBUF (O_Xor)
-----
Total      10.106ns (4.925ns logic, 5.181ns route)
           (48.7% logic, 51.3% route)
=====

```

Cross Clock Domains Report:

```

-----

```

```

=====
Total REAL time to Xst completion: 19.00 secs
Total CPU time to Xst completion: 19.18 secs

```

-->

Total memory usage is 4538384 kilobytes

Number of errors : 0 (0 filtered)
Number of warnings : 1 (0 filtered)
Number of infos : 0 (0 filtered)

```

64210455>fuse -incremental -o unary_tree_tb_isim_beh.exe -prj unary_tree_tb.prj -
top Unary_Op_Bin_Tree_tb
Running: C:\Xilinx\14.7\ISE_DS\ISE\bin\nt64\unwrapped\fuse.exe -incremental -o
unary_tree_tb_isim_beh.exe -prj unary_tree_tb.prj -top Unary_Op_Bin_Tree_tb
ISim P.20131013 (signature 0x7708f090)
Number of CPUs detected in this system: 8
Turning on mult-threading, number of parallel sub-compilation jobs: 16

```

```
Determining compilation order of HDL files
Parsing VHDL file "slv_image_pkg.vhd" into library work
Parsing VHDL file "unary_op_xor_tree_lut6.vhd" into library work
Parsing VHDL file "unary_op_tree.vhd" into library work
Parsing VHDL file "unary_op_tree_IDEAL_tb.vhd" into library work
Starting static elaboration
Completed static elaboration
Compiling package standard
Compiling package std_logic_1164
Compiling package numeric_std
Compiling package textio
Compiling package std_logic_textio
Compiling package slv_image_pkg
Compiling package vcomponents
Compiling package vital_timing
Compiling package vital_primitives
Compiling package vpkg
Compiling architecture lut3_v of entity LUT3 [\LUT3("10010110")(0,7)\]
Compiling architecture tree_of_xor_lut6 of entity XorTreeStage [\XorTreeStage(3)\]
Compiling architecture tree_of_xor_lut6 of entity XorTreeStage [\XorTreeStage(2)\]
Compiling architecture lut6_v of entity LUT6 [\LUT6("0110100110010110100101100...)]
Compiling architecture tree_of_xor_lut6 of entity XorTreeStage
[\XorTreeStage(16)\]
Compiling architecture t of entity Unary_Op_Bin_Tree [\Unary_Op_Bin_Tree(16)\]
Compiling architecture test of entity unary_op_bin_tree_tb
Time Resolution for simulation is 1ps.
Waiting for 1 sub-compilation(s) to finish...
Compiled 23 VHDL Units
Built simulation executable unary_tree_tb_isim_beh.exe
Fuse Memory Usage: 60072 KB
Fuse CPU Usage: 1359 ms
```

```
64210455>if exist Unary_Op_Bin_Tree.csv del Unary_Op_Bin_Tree.csv
```

```
64210455>if exist Unary_Op_Bin_Tree_64210455.csv del
Unary_Op_Bin_Tree_64210455.csv
```

```
64210455>unary_tree_tb_isim_beh.exe -tclbatch isim.tcl -wdb
unary_tree_tb_isim_beh.wdb
ISim P.20131013 (signature 0x7708f090)
WARNING: A WEBPACK license was found.
WARNING: Please use Xilinx License Configuration Manager to check out a full ISim
license.
WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for
more information on the differences between the Lite and the Full version.
This is a Lite version of ISim.
Time resolution is 1 ps
Simulator is doing circuit initialization process.
Finished circuit initialization process.
```

```
64210455>rem ren Unary_Op_Bin_Tree.csv Unary_Op_Bin_Tree_64210455.csv
```

```
64210455>xst -ifn unary_vhdl93.xst
Release 14.7 - xst P.20131013 (nt64)
Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.
--> Parameter TMPDIR set to xst/projnav.tmp
```

```
Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.23 secs
```

--> *Parameter xsthdprdir set to xst*

Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.23 secs

-->

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 - 8.4.4) Timing Details
 - 8.4.5) Cross Clock Domains Report

=====

*	Synthesis Options Summary	*
---	---------------------------	---

=====

---- Source Parameters

Input File Name : *"./unary_vhd193.prj"*
Ignore Synthesis Constraint File : NO

---- Target Parameters

Output File Name : *"reduction_operators"*
Output Format : NGC
Target Device : xc6slx4-3-tqg144

---- Source Options

Top Module Name : reduction_operators
Automatic FSM Extraction : YES
FSM Encoding Algorithm : Auto
Safe Implementation : No
FSM Style : LUT
RAM Extraction : Yes
RAM Style : Auto
ROM Extraction : Yes
Shift Register Extraction : YES
ROM Style : Auto
Resource Sharing : YES
Asynchronous To Synchronous : NO
Shift Register Minimum Size : 2
Use DSP Block : Auto
Automatic Register Balancing : No

---- Target Options

LUT Combining : Auto

Reduce Control Sets : Auto
Add IO Buffers : YES
Global Maximum Fanout : 100000
Add Generic Clock Buffer(BUFG) : 16
Register Duplication : YES
Optimize Instantiated Primitives : NO
Use Clock Enable : Auto
Use Synchronous Set : Auto
Use Synchronous Reset : Auto
Pack IO Registers into IOBs : Auto
Equivalent register Removal : YES

---- General Options

Optimization Goal : Speed
Optimization Effort : 1
Power Reduction : NO
Keep Hierarchy : No
Netlist Hierarchy : As_Optimized
RTL Output : Yes
Global Optimization : AllClockNets
Read Cores : YES
Write Timing Constraints : NO
Cross Clock Analysis : NO
Hierarchy Separator : /
Bus Delimiter : <>
Case Specifier : Maintain
Slice Utilization Ratio : 100
BRAM Utilization Ratio : 100
DSP48 Utilization Ratio : 100
Auto BRAM Packing : NO
Slice Utilization Ratio Delta : 5

=====

=====

* HDL Parsing *

=====

Parsing VHDL file "64210455\unary_operators_vhdl_93.vhd" into library work
Parsing entity <reduction_operators>.
Parsing architecture <vhdl_altered_process> of entity <reduction_operators>.

=====

* HDL Elaboration *

=====

Elaborating entity <reduction_operators> (architecture <vhdl_altered_process>)
with generics from library <work>.

=====

* HDL Synthesis *

=====

Synthesizing Unit <reduction_operators>.

Related source file is "64210455\unary_operators_vhdl_93.vhd".

WIDTH = 64

Summary:

inferred 128 Multiplexer(s).

Unit <reduction_operators> synthesized.

=====

HDL Synthesis Report

Macro Statistics

Multiplexers : 128
1-bit 2-to-1 multiplexer : 128
Xors : 1
1-bit xor65 : 1

=====

* Advanced HDL Synthesis *

=====

=====

Advanced HDL Synthesis Report

Macro Statistics

Multiplexers : 128
1-bit 2-to-1 multiplexer : 128
Xors : 1
1-bit xor65 : 1

=====

* Low Level Synthesis *

=====

WARNING:Xst:2170 - Unit reduction_operators : the following signal(s) form a combinatorial loop: Mmux_process_or.result_or15, Mmux_process_or.result_or6, Mmux_process_or.result_or16, Mmux_process_or.result_or1, Mmux_process_or.result_or13, Mmux_process_or.result_or, Mmux_process_or.result_or4, Mmux_process_or.result_or12, Mmux_process_or.result_or11, reduced_OR, Mmux_process_or.result_or3, Mmux_process_or.result_or8, Mmux_process_or.result_or17, Mmux_process_or.result_or14, Mmux_process_or.result_or18, Mmux_process_or.result_or9, Mmux_process_or.result_or10, Mmux_process_or.result_or19, Mmux_process_or.result_or7, Mmux_process_or.result_or2, Mmux_process_or.result_or5, process_or.result_or_A[63]_OR_1_o.

WARNING:Xst:2170 - Unit reduction_operators : the following signal(s) form a combinatorial loop: Mmux_process_and.result_and12, reduced_AND, process_and.result_and_A[63]_AND_1_o, Mmux_process_and.result_and8, Mmux_process_and.result_and13, Mmux_process_and.result_and17, Mmux_process_and.result_and7, Mmux_process_and.result_and20, Mmux_process_and.result_and18, Mmux_process_and.result_and9, Mmux_process_and.result_and16, Mmux_process_and.result_and, Mmux_process_and.result_and14, Mmux_process_and.result_and6, Mmux_process_and.result_and1, Mmux_process_and.result_and3, Mmux_process_and.result_and11, Mmux_process_and.result_and15, Mmux_process_and.result_and4, Mmux_process_and.result_and19, Mmux_process_and.result_and2, Mmux_process_and.result_and10, Mmux_process_and.result_and5.

WARNING:Xst:2170 - Unit reduction_operators : the following signal(s) form a combinatorial loop: reduced_XOR.

Optimizing unit <reduction_operators> ...

Mapping all equations...
Building and optimizing final netlist ...
Found area constraint ratio of 100 (+ 5) on block reduction_operators, actual ratio is 3.

Final Macro Processing ...

=====
Final Register Report

Found no macro
=====

=====
* Partition Report *
=====

Partition Implementation Status

No Partitions were found in this design.

=====
* Design Summary *
=====

Top Level Output File Name : reduction_operators.ngc

Primitive and Black Box Usage:

BELS : 69
GND : 1
LUT1 : 1
LUT2 : 1
LUT3 : 4
LUT4 : 6
LUT5 : 11
LUT6 : 39
MUXCY : 5
VCC : 1
IO Buffers : 67
IBUF : 64
OBUF : 3

Device utilization summary:

Selected Device : 6slx4tqg144-3

Slice Logic Utilization:

Number of Slice LUTs: 62 out of 2400 2%
Number used as Logic: 62 out of 2400 2%

Slice Logic Distribution:

Number of LUT Flip Flop pairs used: 62
Number with an unused Flip Flop: 62 out of 62 100%
Number with an unused LUT: 0 out of 62 0%

Number of fully used LUT-FF pairs: 0 out of 62 0%
Number of unique control sets: 0

IO Utilization:

Number of IOs: 67
Number of bonded IOBs: 67 out of 102 65%

Specific Feature Utilization:

Partition Resource Summary:

No Partitions were found in this design.

Timing Report

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.
FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT
GENERATED AFTER PLACE-and-ROUTE.

Clock Information:

No clock signals found in this design

Asynchronous Control Signals Information:

No asynchronous control signals found in this design

Timing Summary:

Speed Grade: -3

Minimum period: No path found
Minimum input arrival time before clock: No path found
Maximum output required time after clock: No path found
Maximum combinational path delay: 14.679ns

Timing Details:

All values displayed in nanoseconds (ns)

Timing constraint: Default path analysis

Total number of paths / destination ports: 460 / 3

Delay: 14.679ns (Levels of Logic = 12)

Source: A<49> (PAD)

Destination: reduced_AND (PAD)

Data Path: A<49> to reduced_AND

Gate Net

Cell:in->out fanout Delay Delay Logical Name (Net Name)

IBUF:I->O 5 1.222 1.059 A_49_IBUF (A_49_IBUF)

```

LUT5:I0->O 1 0.203 0.580
process_and.result_and_process_and.result_and_OR_153_o11_SW0 (N2)
LUT6:I5->O 2 0.205 0.981
process_and.result_and_process_and.result_and_OR_153_o11
(process_and.result_and_process_and.result_and_OR_153_o11)
LUT6:I0->O 1 0.203 0.944
process_and.result_and_process_and.result_and_OR_153_o1_SW0 (N4)
LUT6:I0->O 2 0.203 0.981
process_and.result_and_process_and.result_and_OR_153_o1
(process_and.result_and_process_and.result_and_OR_153_o1)
LUT6:I0->O 2 0.203 0.721
process_and.result_and_process_and.result_and_OR_153_o
(process_and.result_and_process_and.result_and_OR_153_o)
LUT6:I4->O 1 0.203 0.580 Mmux_process_and.result_and22231
(Mmux_process_and.result_and2223)
LUT3:I2->O 2 0.205 0.617 Mmux_process_and.result_and22241
(Mmux_process_and.result_and222)
LUT5:I4->O 3 0.205 0.755 process_and.result_and_A[56]_AND_8_o1
(process_and.result_and_A[56]_AND_8_o)
LUT6:I4->O 2 0.203 0.981 Mmux_process_and.result_and104
(Mmux_process_and.result_and9)
LUT6:I0->O 3 0.203 0.650 Mmux_process_and.result_and221 (reduced_AND_OBUF)
OBUF:I->O 2.571 reduced_AND_OBUF (reduced_AND)
-----
Total 14.679ns (5.829ns logic, 8.850ns route)
(39.7% logic, 60.3% route)

```

===== Cross Clock Domains Report: -----

```

=====
Total REAL time to Xst completion: 10.00 secs
Total CPU time to Xst completion: 10.45 secs

```

-->

Total memory usage is 4487516 kilobytes

```

Number of errors : 0 ( 0 filtered)
Number of warnings : 3 ( 0 filtered)
Number of infos : 0 ( 0 filtered)

```

```

64210455>fuse -incremental -o unary_vhdl93_tb_isim_beh.exe -prj
unary_vhdl93_tb.prj -top reduction_operators_tb
Running: C:\Xilinx\14.7\ISE_DS\ISE\bin\nt64\unwrapped\fuse.exe -incremental -o
unary_vhdl93_tb_isim_beh.exe -prj unary_vhdl93_tb.prj -top reduction_operators_tb
ISim P.20131013 (signature 0x7708f090)
Number of CPUs detected in this system: 8
Turning on mult-threading, number of parallel sub-compilation jobs: 16
Determining compilation order of HDL files
Parsing VHDL file "unary_operators_vhdl_93.vhd" into library work
Parsing VHDL file "unary_operators_vhdl93_IDEAL_tb.vhd" into library work
Starting static elaboration

```

```

64210455>if exist reduction_operators.csv del reduction_operators.csv

```

```
64210455>if exist reduction_operators_64210455.csv del  
reduction_operators_64210455.csv
```

```
64210455>unary_vhdl93_tb_isim_beh.exe -tclbatch isim.tcl -wdb  
unary_vhdl93_tb_isim_beh.wdb
```

```
64210455>rem ren reduction_operators.csv reduction_operators_64210455.csv
```

```
-- *****
-- **** STUDENT: 64210457
-- *****
-- KOMENTARJI K OCENI NALOGE
-- Matej Možek: Ni pripomb
-- *****
```

```
64210457>if not exist "xst" mkdir xst
```

```
64210457>cd XST
```

```
64210457\xst>if not exist "projnav.tmp" mkdir "projnav.tmp"
```

```
64210457\xst>cd ..
```

```
64210457>xst -ifn unary_tree.xst
Release 14.7 - xst P.20131013 (nt64)
Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.
--> Parameter TMPDIR set to xst/projnav.tmp
```

```
Total REAL time to Xst completion: 1.00 secs
```

```
Total CPU time to Xst completion: 0.24 secs
```

```
--> Parameter xsthdpdir set to xst
```

```
Total REAL time to Xst completion: 1.00 secs
```

```
Total CPU time to Xst completion: 0.25 secs
```

```
-->
```

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```
=====
*      Synthesis Options Summary      *
=====
```

---- Source Parameters

```
Input File Name      : "unary_tree.prj"
Ignore Synthesis Constraint File : NO
```

---- Target Parameters

```
Output File Name     : "Unary_Op_Bin_Tree"
```

Output Format : NGC
Target Device : xc6slx4-3-tqg144

----- Source Options

Top Module Name : Unary_Op_Bin_Tree
Automatic FSM Extraction : YES
FSM Encoding Algorithm : Auto
Safe Implementation : No
FSM Style : LUT
RAM Extraction : Yes
RAM Style : Auto
ROM Extraction : Yes
Shift Register Extraction : YES
ROM Style : Auto
Resource Sharing : YES
Asynchronous To Synchronous : NO
Shift Register Minimum Size : 2
Use DSP Block : Auto
Automatic Register Balancing : No

----- Target Options

LUT Combining : Auto
Reduce Control Sets : Auto
Add IO Buffers : YES
Global Maximum Fanout : 100000
Add Generic Clock Buffer(BUFG) : 16
Register Duplication : YES
Optimize Instantiated Primitives : NO
Use Clock Enable : Auto
Use Synchronous Set : Auto
Use Synchronous Reset : Auto
Pack IO Registers into IOBs : Auto
Equivalent register Removal : YES

----- General Options

Optimization Goal : Speed
Optimization Effort : 1
Power Reduction : NO
Keep Hierarchy : No
Netlist Hierarchy : As_Optimized
RTL Output : Yes
Global Optimization : AllClockNets
Read Cores : YES
Write Timing Constraints : NO
Cross Clock Analysis : NO
Hierarchy Separator : /
Bus Delimiter : <>
Case Specifier : Maintain
Slice Utilization Ratio : 100
BRAM Utilization Ratio : 100
DSP48 Utilization Ratio : 100
Auto BRAM Packing : NO
Slice Utilization Ratio Delta : 5

=====

=====

* HDL Parsing *

=====

Parsing VHDL file "64210457\unary_op_xor_tree_lut6.vhd" into library work
Parsing entity <XorTreeStage>.
Parsing architecture <tree_of_xor_lut6> of entity <xortreestage>.
Parsing VHDL file "64210457\unary_op_tree.vhd" into library work
Parsing entity <Unary_Op_Bin_Tree>.
Parsing architecture <t> of entity <unary_op_bin_tree>.

```
=====
*          HDL Elaboration          *
=====
```

Elaborating entity <Unary_Op_Bin_Tree> (architecture <t>) with generics from library <work>.

Elaborating entity <XorTreeStage> (architecture <tree_of_xor_lut6>) with generics from library <work>.

Elaborating entity <XorTreeStage> (architecture <tree_of_xor_lut6>) with generics from library <work>.

Elaborating entity <XorTreeStage> (architecture <tree_of_xor_lut6>) with generics from library <work>.

Elaborating entity <XorTreeStage> (architecture <tree_of_xor_lut6>) with generics from library <work>.

Elaborating entity <XorTreeStage> (architecture <tree_of_xor_lut6>) with generics from library <work>.

Elaborating entity <XorTreeStage> (architecture <tree_of_xor_lut6>) with generics from library <work>.

Elaborating entity <XorTreeStage> (architecture <tree_of_xor_lut6>) with generics from library <work>.

Elaborating entity <XorTreeStage> (architecture <tree_of_xor_lut6>) with generics from library <work>.

Elaborating entity <XorTreeStage> (architecture <tree_of_xor_lut6>) with generics from library <work>.

```
=====
*          HDL Synthesis            *
=====
```

Synthesizing Unit <Unary_Op_Bin_Tree>.
Related source file is "64210457\unary_op_tree.vhd".
N = 4096
Summary:
no macro.
Unit <Unary_Op_Bin_Tree> synthesized.

Synthesizing Unit <XorTreeStage_1>.
Related source file is "64210457\unary_op_xor_tree_lut6.vhd".
N = 4096
Summary:
no macro.
Unit <XorTreeStage_1> synthesized.

Synthesizing Unit <XorTreeStage_2>.
Related source file is "64210457\unary_op_xor_tree_lut6.vhd".
N = 683
Summary:
no macro.
Unit <XorTreeStage_2> synthesized.

Synthesizing Unit <XorTreeStage_3>.
Related source file is "64210457\unary_op_xor_tree_lut6.vhd".
N = 114
Summary:
no macro.
Unit <XorTreeStage_3> synthesized.

Synthesizing Unit <XorTreeStage_4>.
Related source file is "64210457\unary_op_xor_tree_lut6.vhd".
N = 19
Summary:
no macro.
Unit <XorTreeStage_4> synthesized.

Synthesizing Unit <XorTreeStage_5>.
Related source file is "64210457\unary_op_xor_tree_lut6.vhd".
N = 4
Summary:
no macro.
Unit <XorTreeStage_5> synthesized.

Synthesizing Unit <XorTreeStage_6>.
Related source file is "64210457\unary_op_xor_tree_lut6.vhd".
N = 3
Summary:
no macro.
Unit <XorTreeStage_6> synthesized.

Synthesizing Unit <XorTreeStage_7>.
Related source file is "64210457\unary_op_xor_tree_lut6.vhd".
N = 113
Summary:
no macro.
Unit <XorTreeStage_7> synthesized.

Synthesizing Unit <XorTreeStage_8>.
Related source file is "64210457\unary_op_xor_tree_lut6.vhd".
N = 18
Summary:
no macro.
Unit <XorTreeStage_8> synthesized.

Synthesizing Unit <XorTreeStage_9>.
Related source file is "64210457\unary_op_xor_tree_lut6.vhd".
N = 682
Summary:
no macro.
Unit <XorTreeStage_9> synthesized.

=====
HDL Synthesis Report

Found no macro

```
=====
*      Advanced HDL Synthesis      *
=====
```

```
=====
Advanced HDL Synthesis Report
=====
```

Found no macro

```
=====
*      Low Level Synthesis      *
=====
```

Optimizing unit <Unary_Op_Bin_Tree> ...

Mapping all equations...

Building and optimizing final netlist ...

Found area constraint ratio of 100 (+ 5) on block Unary_Op_Bin_Tree, actual ratio is 94.

Final Macro Processing ...

```
=====
Final Register Report
=====
```

Found no macro

```
=====
*      Partition Report      *
=====
```

Partition Implementation Status

No Partitions were found in this design.

```
=====
*      Design Summary      *
=====
```

Top Level Output File Name : Unary_Op_Bin_Tree.ngc

Primitive and Black Box Usage:

# BELS	: 1555
# LUT3	: 1088
# LUT4	: 208
# LUT6	: 259
# IO Buffers	: 4097
# IBUF	: 4096
# OBUF	: 1

Device utilization summary:

Selected Device : 6slx4tqg144-3

Slice Logic Utilization:

Number of Slice LUTs: 1555 out of 2400 64%
Number used as Logic: 1555 out of 2400 64%

Slice Logic Distribution:

Number of LUT Flip Flop pairs used: 1555
Number with an unused Flip Flop: 1555 out of 1555 100%
Number with an unused LUT: 0 out of 1555 0%
Number of fully used LUT-FF pairs: 0 out of 1555 0%
Number of unique control sets: 0

IO Utilization:

Number of IOs: 4097
Number of bonded IOBs: 4097 out of 102 4016% (*)

Specific Feature Utilization:

WARNING:Xst:1336 - (*) More than 100% of Device resources are used

Partition Resource Summary:

No Partitions were found in this design.

=====

Timing Report

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.
FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT
GENERATED AFTER PLACE-and-ROUTE.

Clock Information:

No clock signals found in this design

Asynchronous Control Signals Information:

No asynchronous control signals found in this design

Timing Summary:

Speed Grade: -3

Minimum period: No path found
Minimum input arrival time before clock: No path found
Maximum output required time after clock: No path found
Maximum combinational path delay: 10.106ns

Timing Details:

All values displayed in nanoseconds (ns)

```

=====
Timing constraint: Default path analysis
Total number of paths / destination ports: 4096 / 1
-----
Delay:      10.106ns (Levels of Logic = 7)
Source:     I<4092> (PAD)
Destination: O_Xor (PAD)

Data Path: I<4092> to O_Xor
Gate Net
Cell:in->out fanout Delay Delay Logical Name (Net Name)
-----
IBUF:I->O      1 1.222 0.827 I_4092_IBUF (I_4092_IBUF)
LUT4:I0->O     1 0.320 0.944
U_Xor/Stages.XorTreeStage1/Stages.XorTreeStage1/Stages.XorTree
eStage1/Stage_xor_4.XOR4_LUT
(U_Xor/Stages.XorTreeStage1/Stages.XorTreeStage1/Stages.XorTreeStage1/01)
LUT6:I0->O     1 0.203 0.944
U_Xor/Stages.XorTreeStage1/Stages.XorTreeStage1/Stages.XorTreeStage1/Stages.XOR6_L
UT (U_Xor/Stages.XorTreeStage1/Stages.XorTreeStage1/01)
LUT6:I0->O     1 0.203 0.944
U_Xor/Stages.XorTreeStage1/Stages.XorTreeStage1/Stages.XOR6_LUT
(U_Xor/Stages.XorTreeStage1/01)
LUT6:I0->O     1 0.203 0.944 U_Xor/Stages.XorTreeStage1/Stages.XOR6_LUT (U_Xor/01)
LUT6:I0->O     1 0.203 0.579 U_Xor/Stages.XOR6_LUT (O_Xor_OBUF)
OBUF:I->O      2.571  O_Xor_OBUF (O_Xor)
-----
Total      10.106ns (4.925ns logic, 5.181ns route)
           (48.7% logic, 51.3% route)
=====

```

Cross Clock Domains Report:

```

-----
Total REAL time to Xst completion: 22.00 secs
Total CPU time to Xst completion: 21.48 secs

```

-->

Total memory usage is 4538352 kilobytes

```

Number of errors : 0 ( 0 filtered)
Number of warnings : 1 ( 0 filtered)
Number of infos : 0 ( 0 filtered)

```

```

64210457>fuse -incremental -o unary_tree_tb_isim_beh.exe -prj unary_tree_tb.prj -
top Unary_Op_Bin_Tree_tb
Running: C:\Xilinx\14.7\ISE_DS\ISE\bin\nt64\unwrapped\fuse.exe -incremental -o
unary_tree_tb_isim_beh.exe -prj unary_tree_tb.prj -top Unary_Op_Bin_Tree_tb
ISim P.20131013 (signature 0x7708f090)
Number of CPUs detected in this system: 8
Turning on mult-threading, number of parallel sub-compilation jobs: 16
Determining compilation order of HDL files
Parsing VHDL file "slv_image_pkg.vhd" into library work
Parsing VHDL file "unary_op_xor_tree_lut6.vhd" into library work

```

```
Parsing VHDL file "unary_op_tree.vhd" into library work
Parsing VHDL file "unary_op_tree_IDEAL_tb.vhd" into library work
Starting static elaboration
Completed static elaboration
Compiling package standard
Compiling package std_logic_1164
Compiling package numeric_std
Compiling package textio
Compiling package std_logic_textio
Compiling package slv_image_pkg
Compiling package vcomponents
Compiling package vital_timing
Compiling package vital_primitives
Compiling package vpkg
Compiling architecture lut3_v of entity LUT3 [\LUT3("01101001")(0,7)\]
Compiling architecture tree_of_xor_lut6 of entity XorTreeStage [\XorTreeStage(3)\]
Compiling architecture tree_of_xor_lut6 of entity XorTreeStage [\XorTreeStage(2)\]
Compiling architecture lut6_v of entity LUT6 [\LUT6("0110100110010110100101100...)]
Compiling architecture tree_of_xor_lut6 of entity XorTreeStage
[\XorTreeStage(16)\]
Compiling architecture t of entity Unary_Op_Bin_Tree [\Unary_Op_Bin_Tree(16)\]
Compiling architecture test of entity unary_op_bin_tree_tb
Time Resolution for simulation is 1ps.
Waiting for 1 sub-compilation(s) to finish...
Compiled 23 VHDL Units
Built simulation executable unary_tree_tb_isim_beh.exe
Fuse Memory Usage: 59128 KB
Fuse CPU Usage: 1296 ms
```

```
64210457>if exist Unary_Op_Bin_Tree.csv del Unary_Op_Bin_Tree.csv
```

```
64210457>if exist Unary_Op_Bin_Tree_64210457.csv del
Unary_Op_Bin_Tree_64210457.csv
```

```
64210457>unary_tree_tb_isim_beh.exe -tclbatch isim.tcl -wdb
unary_tree_tb_isim_beh.wdb
ISim P.20131013 (signature 0x7708f090)
WARNING: A WEBPACK license was found.
WARNING: Please use Xilinx License Configuration Manager to check out a full ISim
license.
WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for
more information on the differences between the Lite and the Full version.
This is a Lite version of ISim.
Time resolution is 1 ps
Simulator is doing circuit initialization process.
Finished circuit initialization process.
```

```
64210457>rem ren Unary_Op_Bin_Tree.csv Unary_Op_Bin_Tree_64210457.csv
```

```
64210457>xst -ifn unary_vhdl93.xst
Release 14.7 - xst P.20131013 (nt64)
Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.
--> Parameter TMPDIR set to xst/projnav.tmp
```

```
Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.26 secs
```

```
--> Parameter xsthdpdir set to xst
```

Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.26 secs

-->

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 - 8.4.5) Cross Clock Domains Report

```
=====
*      Synthesis Options Summary      *
=====
```

---- Source Parameters

Input File Name : "./unary_vhd193.prj"
Ignore Synthesis Constraint File : NO

---- Target Parameters

Output File Name : "reduction_operators"
Output Format : NGC
Target Device : xc6slx4-3-tqg144

---- Source Options

Top Module Name : reduction_operators
Automatic FSM Extraction : YES
FSM Encoding Algorithm : Auto
Safe Implementation : No
FSM Style : LUT
RAM Extraction : Yes
RAM Style : Auto
ROM Extraction : Yes
Shift Register Extraction : YES
ROM Style : Auto
Resource Sharing : YES
Asynchronous To Synchronous : NO
Shift Register Minimum Size : 2
Use DSP Block : Auto
Automatic Register Balancing : No

---- Target Options

LUT Combining : Auto
Reduce Control Sets : Auto
Add IO Buffers : YES
Global Maximum Fanout : 100000

Add Generic Clock Buffer(BUFG) : 16
Register Duplication : YES
Optimize Instantiated Primitives : NO
Use Clock Enable : Auto
Use Synchronous Set : Auto
Use Synchronous Reset : Auto
Pack IO Registers into IOBs : Auto
Equivalent register Removal : YES

---- General Options

Optimization Goal : Speed
Optimization Effort : 1
Power Reduction : NO
Keep Hierarchy : No
Netlist Hierarchy : As_Optimized
RTL Output : Yes
Global Optimization : AllClockNets
Read Cores : YES
Write Timing Constraints : NO
Cross Clock Analysis : NO
Hierarchy Separator : /
Bus Delimiter : <>
Case Specifier : Maintain
Slice Utilization Ratio : 100
BRAM Utilization Ratio : 100
DSP48 Utilization Ratio : 100
Auto BRAM Packing : NO
Slice Utilization Ratio Delta : 5

=====

=====

* HDL Parsing *

=====

Parsing VHDL file "64210457\unary_operators_vhdl_93.vhd" into library work
Parsing entity <reduction_operators>.
Parsing architecture <vhdl_93_process> of entity <reduction_operators>.

=====

* HDL Elaboration *

=====

Elaborating entity <reduction_operators> (architecture <vhdl_93_process>) with
generics from library <work>.

=====

* HDL Synthesis *

=====

Synthesizing Unit <reduction_operators>.

Related source file is "64210457\unary_operators_vhdl_93.vhd".

N = 64

Summary:

inferred 128 Multiplexer(s).

Unit <reduction_operators> synthesized.

=====

HDL Synthesis Report

Macro Statistics

Multiplexers : 128
1-bit 2-to-1 multiplexer : 128
Xors : 1
1-bit xor64 : 1

=====

=====

* Advanced HDL Synthesis *

=====

=====

Advanced HDL Synthesis Report

Macro Statistics

Multiplexers : 128
1-bit 2-to-1 multiplexer : 128
Xors : 1
1-bit xor64 : 1

=====

=====

* Low Level Synthesis *

=====

Optimizing unit <reduction_operators> ...

Mapping all equations...

Building and optimizing final netlist ...

Found area constraint ratio of 100 (+ 5) on block reduction_operators, actual ratio is 1.

Final Macro Processing ...

=====

Final Register Report

Found no macro

=====

=====

* Partition Report *

=====

Partition Implementation Status

No Partitions were found in this design.

=====

* Design Summary *

=====

Top Level Output File Name : reduction_operators.ngc

Primitive and Black Box Usage:

```
-----
# BELS      : 59
# GND       : 1
# LUT4      : 3
# LUT6      : 32
# MUXCY     : 22
# VCC       : 1
# IO Buffers : 67
# IBUF      : 64
# OBUF      : 3
```

Device utilization summary:

Selected Device : 6slx4tqg144-3

Slice Logic Utilization:

Number of Slice LUTs: 35 out of 2400 1%
Number used as Logic: 35 out of 2400 1%

Slice Logic Distribution:

Number of LUT Flip Flop pairs used: 35
Number with an unused Flip Flop: 35 out of 35 100%
Number with an unused LUT: 0 out of 35 0%
Number of fully used LUT-FF pairs: 0 out of 35 0%
Number of unique control sets: 0

IO Utilization:

Number of IOs: 67
Number of bonded IOBs: 67 out of 102 65%

Specific Feature Utilization:

----- Partition Resource Summary: -----

No Partitions were found in this design.

=====

Timing Report

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.

FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT
GENERATED AFTER PLACE-and-ROUTE.

Clock Information:

No clock signals found in this design

Asynchronous Control Signals Information:

No asynchronous control signals found in this design

Timing Summary:

Speed Grade: -3

Minimum period: No path found

Minimum input arrival time before clock: No path found

Maximum output required time after clock: No path found

Maximum combinational path delay: 7.522ns

Timing Details:

All values displayed in nanoseconds (ns)

=====

Timing constraint: Default path analysis

Total number of paths / destination ports: 192 / 3

Delay: 7.522ns (Levels of Logic = 5)

Source: A<22> (PAD)

Destination: reduced_XOR (PAD)

Data Path: A<22> to reduced_XOR

Gate Net

Cell:in->out fanout Delay Delay Logical Name (Net Name)

IBUF:I->O	3	1.222	1.015	A_22_IBUF	(A_22_IBUF)
LUT6:I0->O	1	0.203	0.944	Mxor_reduced_XOR_xo<0>3	(Mxor_reduced_XOR_xo<0>2)
LUT6:I0->O	1	0.203	0.580	Mxor_reduced_XOR_xo<0>14_SW0	(N01)
LUT6:I5->O	1	0.205	0.579	Mxor_reduced_XOR_xo<0>14	(reduced_XOR_OBUF)
OBUF:I->O	2	2.571		reduced_XOR_OBUF	(reduced_XOR)

Total 7.522ns (4.404ns logic, 3.118ns route)
(58.5% logic, 41.5% route)

=====

Cross Clock Domains Report:

Total REAL time to Xst completion: 10.00 secs

Total CPU time to Xst completion: 9.91 secs

-->

Total memory usage is 4487516 kilobytes

Number of errors : 0 (0 filtered)

Number of warnings : 0 (0 filtered)

Number of infos : 0 (0 filtered)

64210457>fuse -incremental -o unary_vhdl93_tb_isim_beh.exe -prj

unary_vhdl93_tb.prj -top reduction_operators_tb

Running: C:\Xilinx\14.7\ISE_DS\ISE\bin\nt64\unwrapped\fuse.exe -incremental -o
unary_vhdl93_tb_isim_beh.exe -prj unary_vhdl93_tb.prj -top reduction_operators_tb
ISim P.20131013 (signature 0x7708f090)

Number of CPUs detected in this system: 8

Turning on mult-threading, number of parallel sub-compilation jobs: 16

Determining compilation order of HDL files

Parsing VHDL file "unary_operators_vhdl_93.vhd" into library work

```
Parsing VHDL file "unary_operators_vhdl93_IDEAL_tb.vhd" into library work
Starting static elaboration
Completed static elaboration
Compiling package standard
Compiling package std_logic_1164
Compiling package numeric_std
Compiling package textio
Compiling package std_logic_textio
Compiling architecture vhdl_93_process of entity reduction_operators
[\\reduction_operators(3)\\]
Compiling architecture test of entity reduction_operators_tb
Time Resolution for simulation is 1ps.
Waiting for 1 sub-compilation(s) to finish...
Compiled 8 VHDL Units
Built simulation executable unary_vhdl93_tb_isim_beh.exe
Fuse Memory Usage: 36732 KB
Fuse CPU Usage: 812 ms
```

```
64210457>if exist reduction_operators.csv del reduction_operators.csv
```

```
64210457>if exist reduction_operators_64210457.csv del
reduction_operators_64210457.csv
```

```
64210457>unary_vhdl93_tb_isim_beh.exe -tclbatch isim.tcl -wdb
unary_vhdl93_tb_isim_beh.wdb
ISim P.20131013 (signature 0x7708f090)
WARNING: A WEBPACK license was found.
WARNING: Please use Xilinx License Configuration Manager to check out a full ISim
license.
WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for
more information on the differences between the Lite and the Full version.
This is a Lite version of ISim.
Time resolution is 1 ps
Simulator is doing circuit initialization process.
Finished circuit initialization process.
```

```
64210457>rem ren reduction_operators.csv reduction_operators_64210457.csv
```

```
-- *****
-- **** STUDENT: 64240429
-- *****
-- KOMENTARJI K OCENI NALOGE
-- Matej Možek: Ni pripomb
-- *****
```

```
64240429>if not exist "xst" mkdir xst
```

```
64240429>cd XST
```

```
64240429\xst>if not exist "projnav.tmp" mkdir "projnav.tmp"
```

```
64240429\xst>cd ..
```

```
64240429>xst -ifn unary_tree.xst
Release 14.7 - xst P.20131013 (nt64)
Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.
--> Parameter TMPDIR set to xst/projnav.tmp
```

```
Total REAL time to Xst completion: 1.00 secs
```

```
Total CPU time to Xst completion: 0.24 secs
```

```
--> Parameter xsthdpdir set to xst
```

```
Total REAL time to Xst completion: 1.00 secs
```

```
Total CPU time to Xst completion: 0.25 secs
```

```
-->
```

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 - 8.4.4) Timing Details
 - 8.4.5) Cross Clock Domains Report

```
=====
*      Synthesis Options Summary      *
=====
```

---- Source Parameters

```
Input File Name      : "unary_tree.prj"
Ignore Synthesis Constraint File : NO
```

---- Target Parameters

```
Output File Name     : "Unary_Op_Bin_Tree"
```

Output Format : NGC
Target Device : xc6slx4-3-tqg144

----- Source Options

Top Module Name : Unary_Op_Bin_Tree
Automatic FSM Extraction : YES
FSM Encoding Algorithm : Auto
Safe Implementation : No
FSM Style : LUT
RAM Extraction : Yes
RAM Style : Auto
ROM Extraction : Yes
Shift Register Extraction : YES
ROM Style : Auto
Resource Sharing : YES
Asynchronous To Synchronous : NO
Shift Register Minimum Size : 2
Use DSP Block : Auto
Automatic Register Balancing : No

----- Target Options

LUT Combining : Auto
Reduce Control Sets : Auto
Add IO Buffers : YES
Global Maximum Fanout : 100000
Add Generic Clock Buffer(BUFG) : 16
Register Duplication : YES
Optimize Instantiated Primitives : NO
Use Clock Enable : Auto
Use Synchronous Set : Auto
Use Synchronous Reset : Auto
Pack IO Registers into IOBs : Auto
Equivalent register Removal : YES

----- General Options

Optimization Goal : Speed
Optimization Effort : 1
Power Reduction : NO
Keep Hierarchy : No
Netlist Hierarchy : As_Optimized
RTL Output : Yes
Global Optimization : AllClockNets
Read Cores : YES
Write Timing Constraints : NO
Cross Clock Analysis : NO
Hierarchy Separator : /
Bus Delimiter : <>
Case Specifier : Maintain
Slice Utilization Ratio : 100
BRAM Utilization Ratio : 100
DSP48 Utilization Ratio : 100
Auto BRAM Packing : NO
Slice Utilization Ratio Delta : 5

=====

=====

* HDL Parsing *

=====

Parsing VHDL file "64240429\unary_op_xor_tree_lut6.vhd" into library work
Parsing entity <XorTreeStage>.
Parsing architecture <tree_of_xor_lut6> of entity <xortreestage>.
Parsing VHDL file "64240429\unary_op_tree.vhd" into library work
Parsing entity <Unary_Op_Bin_Tree>.
Parsing architecture <t> of entity <unary_op_bin_tree>.

```
=====
*          HDL Elaboration          *
=====
```

Elaborating entity <Unary_Op_Bin_Tree> (architecture <t>) with generics from library <work>.

Elaborating entity <XorTreeStage> (architecture <tree_of_xor_lut6>) with generics from library <work>.

Elaborating entity <XorTreeStage> (architecture <tree_of_xor_lut6>) with generics from library <work>.

Elaborating entity <XorTreeStage> (architecture <tree_of_xor_lut6>) with generics from library <work>.

Elaborating entity <XorTreeStage> (architecture <tree_of_xor_lut6>) with generics from library <work>.

Elaborating entity <XorTreeStage> (architecture <tree_of_xor_lut6>) with generics from library <work>.

Elaborating entity <XorTreeStage> (architecture <tree_of_xor_lut6>) with generics from library <work>.

Elaborating entity <XorTreeStage> (architecture <tree_of_xor_lut6>) with generics from library <work>.

Elaborating entity <XorTreeStage> (architecture <tree_of_xor_lut6>) with generics from library <work>.

Elaborating entity <XorTreeStage> (architecture <tree_of_xor_lut6>) with generics from library <work>.

```
=====
*          HDL Synthesis            *
=====
```

Synthesizing Unit <Unary_Op_Bin_Tree>.
Related source file is "64240429\unary_op_tree.vhd".
N = 4096
Summary:
no macro.
Unit <Unary_Op_Bin_Tree> synthesized.

Synthesizing Unit <XorTreeStage_1>.
Related source file is "64240429\unary_op_xor_tree_lut6.vhd".
N = 4096
Summary:
no macro.
Unit <XorTreeStage_1> synthesized.

Synthesizing Unit <XorTreeStage_2>.
Related source file is "64240429\unary_op_xor_tree_lut6.vhd".
N = 683
Summary:
no macro.
Unit <XorTreeStage_2> synthesized.

Synthesizing Unit <XorTreeStage_3>.
Related source file is "64240429\unary_op_xor_tree_lut6.vhd".
N = 114
Summary:
no macro.
Unit <XorTreeStage_3> synthesized.

Synthesizing Unit <XorTreeStage_4>.
Related source file is "64240429\unary_op_xor_tree_lut6.vhd".
N = 19
Summary:
no macro.
Unit <XorTreeStage_4> synthesized.

Synthesizing Unit <XorTreeStage_5>.
Related source file is "64240429\unary_op_xor_tree_lut6.vhd".
N = 4
Summary:
no macro.
Unit <XorTreeStage_5> synthesized.

Synthesizing Unit <XorTreeStage_6>.
Related source file is "64240429\unary_op_xor_tree_lut6.vhd".
N = 3
Summary:
no macro.
Unit <XorTreeStage_6> synthesized.

Synthesizing Unit <XorTreeStage_7>.
Related source file is "64240429\unary_op_xor_tree_lut6.vhd".
N = 113
Summary:
no macro.
Unit <XorTreeStage_7> synthesized.

Synthesizing Unit <XorTreeStage_8>.
Related source file is "64240429\unary_op_xor_tree_lut6.vhd".
N = 18
Summary:
no macro.
Unit <XorTreeStage_8> synthesized.

Synthesizing Unit <XorTreeStage_9>.
Related source file is "64240429\unary_op_xor_tree_lut6.vhd".
N = 682
Summary:
no macro.
Unit <XorTreeStage_9> synthesized.

=====
HDL Synthesis Report

Found no macro

```
=====
*      Advanced HDL Synthesis      *
=====
```

```
=====
Advanced HDL Synthesis Report
=====
```

Found no macro

```
=====
*      Low Level Synthesis      *
=====
```

Optimizing unit <Unary_Op_Bin_Tree> ...

Mapping all equations...

Building and optimizing final netlist ...

Found area constraint ratio of 100 (+ 5) on block Unary_Op_Bin_Tree, actual ratio is 94.

Final Macro Processing ...

```
=====
Final Register Report
=====
```

Found no macro

```
=====
*      Partition Report      *
=====
```

Partition Implementation Status

No Partitions were found in this design.

```
=====
*      Design Summary      *
=====
```

Top Level Output File Name : Unary_Op_Bin_Tree.ngc

Primitive and Black Box Usage:

# BELS	: 1555
# LUT3	: 1088
# LUT4	: 208
# LUT6	: 259
# IO Buffers	: 4097
# IBUF	: 4096
# OBUF	: 1

Device utilization summary:

Selected Device : 6slx4tqg144-3

Slice Logic Utilization:

Number of Slice LUTs: 1555 out of 2400 64%
Number used as Logic: 1555 out of 2400 64%

Slice Logic Distribution:

Number of LUT Flip Flop pairs used: 1555
Number with an unused Flip Flop: 1555 out of 1555 100%
Number with an unused LUT: 0 out of 1555 0%
Number of fully used LUT-FF pairs: 0 out of 1555 0%
Number of unique control sets: 0

IO Utilization:

Number of IOs: 4097
Number of bonded IOBs: 4097 out of 102 4016% (*)

Specific Feature Utilization:

WARNING:Xst:1336 - (*) More than 100% of Device resources are used

Partition Resource Summary:

No Partitions were found in this design.

=====

Timing Report

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.
FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT
GENERATED AFTER PLACE-and-ROUTE.

Clock Information:

No clock signals found in this design

Asynchronous Control Signals Information:

No asynchronous control signals found in this design

Timing Summary:

Speed Grade: -3

Minimum period: No path found
Minimum input arrival time before clock: No path found
Maximum output required time after clock: No path found
Maximum combinational path delay: 10.106ns

Timing Details:

All values displayed in nanoseconds (ns)


```

=====
Timing constraint: Default path analysis
Total number of paths / destination ports: 4096 / 1
-----
Delay:      10.106ns (Levels of Logic = 7)
Source:     I<4092> (PAD)
Destination: O_Xor (PAD)

Data Path: I<4092> to O_Xor
Gate Net
Cell:in->out fanout Delay Delay Logical Name (Net Name)
-----
IBUF:I->O      1 1.222 0.827 I_4092_IBUF (I_4092_IBUF)
LUT4:I0->O     1 0.320 0.944
U_Xor/Stages.Branch1/Stages.Branch1/Stages.Branch1/Stage_xor_4.XOR4
_LUT4 (U_Xor/Stages.Branch1/Stages.Branch1/Stages.Branch1/Stages.Sixth1_out)
LUT6:I0->O     1 0.203 0.944
U_Xor/Stages.Branch1/Stages.Branch1/Stages.Branch1/Stages.XOR6_LUT6
(U_Xor/Stages.Branch1/Stages.Branch1/Stages.Sixth1_out)
LUT6:I0->O     1 0.203 0.944 U_Xor/Stages.Branch1/Stages.Branch1/Stages.XOR6_LUT6
(U_Xor/Stages.Branch1/Stages.Sixth1_out)
LUT6:I0->O     1 0.203 0.944 U_Xor/Stages.Branch1/Stages.XOR6_LUT6
(U_Xor/Stages.Sixth1_out)
LUT6:I0->O     1 0.203 0.579 U_Xor/Stages.XOR6_LUT6 (O_Xor_OBUF)
OBUF:I->O      2.571 O_Xor_OBUF (O_Xor)
-----
Total      10.106ns (4.925ns logic, 5.181ns route)
          (48.7% logic, 51.3% route)
=====

```

Cross Clock Domains Report:

```

=====
Total REAL time to Xst completion: 20.00 secs
Total CPU time to Xst completion: 19.46 secs

```

-->

Total memory usage is 4538348 kilobytes

```

Number of errors : 0 ( 0 filtered)
Number of warnings : 1 ( 0 filtered)
Number of infos : 0 ( 0 filtered)

```

```

64240429>fuse -incremental -o unary_tree_tb_isim_beh.exe -prj unary_tree_tb.prj -
top Unary_Op_Bin_Tree_tb
Running: C:\Xilinx\14.7\ISE_DS\ISE\bin\nt64\unwrapped\fuse.exe -incremental -o
unary_tree_tb_isim_beh.exe -prj unary_tree_tb.prj -top Unary_Op_Bin_Tree_tb
ISim P.20131013 (signature 0x7708f090)
Number of CPUs detected in this system: 8
Turning on mult-threading, number of parallel sub-compilation jobs: 16
Determining compilation order of HDL files
Parsing VHDL file "slv_image_pkg.vhd" into library work
Parsing VHDL file "unary_op_xor_tree_lut6.vhd" into library work
Parsing VHDL file "unary_op_tree.vhd" into library work

```

```
Parsing VHDL file "unary_op_tree_IDEAL_tb.vhd" into library work
Starting static elaboration
Completed static elaboration
Compiling package standard
Compiling package std_logic_1164
Compiling package numeric_std
Compiling package textio
Compiling package std_logic_textio
Compiling package slv_image_pkg
Compiling package vcomponents
Compiling package vital_timing
Compiling package vital_primitives
Compiling package vpkg
Compiling architecture lut3_v of entity LUT3 [\LUT3("10010110")(0,7)\]
Compiling architecture tree_of_xor_lut6 of entity XorTreeStage [\XorTreeStage(3)\]
Compiling architecture tree_of_xor_lut6 of entity XorTreeStage [\XorTreeStage(2)\]
Compiling architecture lut6_v of entity LUT6 [\LUT6("0110100110010110100101100...")\]
Compiling architecture tree_of_xor_lut6 of entity XorTreeStage
[\XorTreeStage(16)\]
Compiling architecture t of entity Unary_Op_Bin_Tree [\Unary_Op_Bin_Tree(16)\]
Compiling architecture test of entity unary_op_bin_tree_tb
Time Resolution for simulation is 1ps.
Waiting for 1 sub-compilation(s) to finish...
Compiled 23 VHDL Units
Built simulation executable unary_tree_tb_isim_beh.exe
Fuse Memory Usage: 59788 KB
Fuse CPU Usage: 1311 ms
```

```
64240429>if exist Unary_Op_Bin_Tree.csv del Unary_Op_Bin_Tree.csv
```

```
64240429>if exist Unary_Op_Bin_Tree_64240429.csv del
Unary_Op_Bin_Tree_64240429.csv
```

```
64240429>unary_tree_tb_isim_beh.exe -tclbatch isim.tcl -wdb
unary_tree_tb_isim_beh.wdb
ISim P.20131013 (signature 0x7708f090)
WARNING: A WEBPACK license was found.
WARNING: Please use Xilinx License Configuration Manager to check out a full ISim
license.
WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for
more information on the differences between the Lite and the Full version.
This is a Lite version of ISim.
Time resolution is 1 ps
Simulator is doing circuit initialization process.
Finished circuit initialization process.
```

```
64240429>rem ren Unary_Op_Bin_Tree.csv Unary_Op_Bin_Tree_64240429.csv
```

```
64240429>xst -ifn unary_vhdl93.xst
Release 14.7 - xst P.20131013 (nt64)
Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.
--> Parameter TMPDIR set to xst/projnav.tmp
```

```
Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.23 secs
```

```
--> Parameter xsthdpdir set to xst
```

```
Total REAL time to Xst completion: 0.00 secs
```

Total CPU time to Xst completion: 0.23 secs

-->

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```
=====
*      Synthesis Options Summary      *
=====
```

---- Source Parameters

Input File Name : "./unary_vhd193.prj"
Ignore Synthesis Constraint File : NO

---- Target Parameters

Output File Name : "reduction_operators"
Output Format : NGC
Target Device : xc6slx4-3-tqg144

---- Source Options

Top Module Name : reduction_operators
Automatic FSM Extraction : YES
FSM Encoding Algorithm : Auto
Safe Implementation : No
FSM Style : LUT
RAM Extraction : Yes
RAM Style : Auto
ROM Extraction : Yes
Shift Register Extraction : YES
ROM Style : Auto
Resource Sharing : YES
Asynchronous To Synchronous : NO
Shift Register Minimum Size : 2
Use DSP Block : Auto
Automatic Register Balancing : No

---- Target Options

LUT Combining : Auto
Reduce Control Sets : Auto
Add IO Buffers : YES
Global Maximum Fanout : 100000
Add Generic Clock Buffer(BUFG) : 16

Register Duplication : YES
Optimize Instantiated Primitives : NO
Use Clock Enable : Auto
Use Synchronous Set : Auto
Use Synchronous Reset : Auto
Pack IO Registers into IOBs : Auto
Equivalent register Removal : YES

---- General Options

Optimization Goal : Speed
Optimization Effort : 1
Power Reduction : NO
Keep Hierarchy : No
Netlist Hierarchy : As_Optimized
RTL Output : Yes
Global Optimization : AllClockNets
Read Cores : YES
Write Timing Constraints : NO
Cross Clock Analysis : NO
Hierarchy Separator : /
Bus Delimiter : <>
Case Specifier : Maintain
Slice Utilization Ratio : 100
BRAM Utilization Ratio : 100
DSP48 Utilization Ratio : 100
Auto BRAM Packing : NO
Slice Utilization Ratio Delta : 5

=====

=====

* HDL Parsing *

=====

Parsing VHDL file "64240429\unary_operators_vhdl_93.vhd" into library work
Parsing entity <reduction_operators>.
Parsing architecture <vhdl_93_process> of entity <reduction_operators>.

=====

* HDL Elaboration *

=====

Elaborating entity <reduction_operators> (architecture <vhdl_93_process>) with
generics from library <work>.

=====

* HDL Synthesis *

=====

Synthesizing Unit <reduction_operators>.
Related source file is "64240429\unary_operators_vhdl_93.vhd".
N = 50
Summary:
inferred 100 Multiplexer(s).
Unit <reduction_operators> synthesized.

=====

HDL Synthesis Report

Macro Statistics

```
# Multiplexers          : 100
 1-bit 2-to-1 multiplexer : 100
# Xors                  : 1
 1-bit xor50            : 1
```

=====

=====

```
*      Advanced HDL Synthesis      *
```

=====

=====

Advanced HDL Synthesis Report

Macro Statistics

```
# Multiplexers          : 100
 1-bit 2-to-1 multiplexer : 100
# Xors                  : 1
 1-bit xor50            : 1
```

=====

=====

```
*      Low Level Synthesis      *
```

=====

Optimizing unit <reduction_operators> ...

Mapping all equations...

Building and optimizing final netlist ...

Found area constraint ratio of 100 (+ 5) on block reduction_operators, actual ratio is 1.

Final Macro Processing ...

=====

Final Register Report

Found no macro

=====

=====

```
*      Partition Report      *
```

=====

Partition Implementation Status

No Partitions were found in this design.

=====

```
*      Design Summary      *
```

=====

Top Level Output File Name : reduction_operators.ngc

Primitive and Black Box Usage:

```
-----
# BELS      : 49
# GND       : 1
# LUT2      : 3
# LUT4      : 1
# LUT6      : 25
# MUXCY     : 18
# VCC       : 1
# IO Buffers : 53
# IBUF      : 50
# OBUF      : 3
```

Device utilization summary:

Selected Device : 6slx4tqg144-3

Slice Logic Utilization:

Number of Slice LUTs: 29 out of 2400 1%
Number used as Logic: 29 out of 2400 1%

Slice Logic Distribution:

Number of LUT Flip Flop pairs used: 29
Number with an unused Flip Flop: 29 out of 29 100%
Number with an unused LUT: 0 out of 29 0%
Number of fully used LUT-FF pairs: 0 out of 29 0%
Number of unique control sets: 0

IO Utilization:

Number of IOs: 53
Number of bonded IOBs: 53 out of 102 51%

Specific Feature Utilization:

Partition Resource Summary:

No Partitions were found in this design.

=====

Timing Report

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.

FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT
GENERATED AFTER PLACE-and-ROUTE.

Clock Information:

No clock signals found in this design

Asynchronous Control Signals Information:

No asynchronous control signals found in this design

Timing Summary:

Speed Grade: -3

Minimum period: No path found
Minimum input arrival time before clock: No path found
Maximum output required time after clock: No path found
Maximum combinational path delay: 7.767ns

Timing Details:

All values displayed in nanoseconds (ns)

=====

Timing constraint: Default path analysis

Total number of paths / destination ports: 150 / 3

Delay: 7.767ns (Levels of Logic = 5)

Source: A<39> (PAD)

Destination: reduced_XOR (PAD)

Data Path: A<39> to reduced_XOR

Gate Net

Cell:in->out fanout Delay Delay Logical Name (Net Name)

IBUF:I->O	3	1.222	1.015	A_39_IBUF	(A_39_IBUF)
LUT6:I0->O	1	0.203	0.944	Mxor_reduced_XOR_xo<0>1	(Mxor_reduced_XOR_xo<0>)
LUT6:I0->O	1	0.203	0.827	Mxor_reduced_XOR_xo<0>7	(Mxor_reduced_XOR_xo<0>6)
LUT4:I0->O	1	0.203	0.579	Mxor_reduced_XOR_xo<0>11	(reduced_XOR_OBUF)
OBUF:I->O	2.571			reduced_XOR_OBUF	(reduced_XOR)

Total 7.767ns (4.402ns logic, 3.365ns route)
(56.7% logic, 43.3% route)

=====

Cross Clock Domains Report:

Total REAL time to Xst completion: 8.00 secs

Total CPU time to Xst completion: 8.69 secs

-->

Total memory usage is 4487516 kilobytes

Number of errors : 0 (0 filtered)

Number of warnings : 0 (0 filtered)

Number of infos : 0 (0 filtered)

64240429>fuse -incremental -o unary_vhdl93_tb_isim_beh.exe -prj

unary_vhdl93_tb.prj -top reduction_operators_tb

Running: C:\Xilinx\14.7\ISE_DS\ISE\bin\nt64\unwrapped\fuse.exe -incremental -o
unary_vhdl93_tb_isim_beh.exe -prj unary_vhdl93_tb.prj -top reduction_operators_tb
ISim P.20131013 (signature 0x7708f090)

Number of CPUs detected in this system: 8

Turning on mult-threading, number of parallel sub-compilation jobs: 16

Determining compilation order of HDL files

Parsing VHDL file "unary_operators_vhdl93.vhd" into library work

```
Parsing VHDL file "unary_operators_vhdl93_IDEAL_tb.vhd" into library work
Starting static elaboration
Completed static elaboration
Compiling package standard
Compiling package std_logic_1164
Compiling package numeric_std
Compiling package textio
Compiling package std_logic_textio
Compiling architecture vhdl_93_process of entity reduction_operators
[\\reduction_operators(3)\\]
Compiling architecture test of entity reduction_operators_tb
Time Resolution for simulation is 1ps.
Waiting for 1 sub-compilation(s) to finish...
Compiled 8 VHDL Units
Built simulation executable unary_vhdl93_tb_isim_beh.exe
Fuse Memory Usage: 36812 KB
Fuse CPU Usage: 811 ms
```

```
64240429>if exist reduction_operators.csv del reduction_operators.csv
```

```
64240429>if exist reduction_operators_64240429.csv del
reduction_operators_64240429.csv
```

```
64240429>unary_vhdl93_tb_isim_beh.exe -tclbatch isim.tcl -wdb
unary_vhdl93_tb_isim_beh.wdb
ISim P.20131013 (signature 0x7708f090)
WARNING: A WEBPACK license was found.
WARNING: Please use Xilinx License Configuration Manager to check out a full ISim
license.
WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for
more information on the differences between the Lite and the Full version.
This is a Lite version of ISim.
Time resolution is 1 ps
Simulator is doing circuit initialization process.
Finished circuit initialization process.
```

```
64240429>rem ren reduction_operators.csv reduction_operators_64240429.csv
```



```
-- *****
-- **** STUDENT: 64240430
-- *****
-- KOMENTARJI K OCENI NALOGE
-- Matej Možek: Ni pripomb
-- *****
```

```
64240430>if not exist "xst" mkdir xst
```

```
64240430>cd XST
```

```
64240430\xst>if not exist "projnav.tmp" mkdir "projnav.tmp"
```

```
64240430\xst>cd ..
```

```
64240430>xst -ifn unary_tree.xst
Release 14.7 - xst P.20131013 (nt64)
Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.
--> Parameter TMPDIR set to xst/projnav.tmp
```

```
Total REAL time to Xst completion: 0.00 secs
```

```
Total CPU time to Xst completion: 0.45 secs
```

```
--> Parameter xsthdpdir set to xst
```

```
Total REAL time to Xst completion: 0.00 secs
```

```
Total CPU time to Xst completion: 0.45 secs
```

```
-->
```

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```
=====
*      Synthesis Options Summary      *
```

----- Source Parameters

```
Input File Name      : "unary_tree.prj"
Ignore Synthesis Constraint File : NO
```

----- Target Parameters

```
Output File Name     : "Unary_Op_Bin_Tree"
```

Output Format : NGC
Target Device : xc6slx4-3-tqg144

----- Source Options

Top Module Name : Unary_Op_Bin_Tree
Automatic FSM Extraction : YES
FSM Encoding Algorithm : Auto
Safe Implementation : No
FSM Style : LUT
RAM Extraction : Yes
RAM Style : Auto
ROM Extraction : Yes
Shift Register Extraction : YES
ROM Style : Auto
Resource Sharing : YES
Asynchronous To Synchronous : NO
Shift Register Minimum Size : 2
Use DSP Block : Auto
Automatic Register Balancing : No

----- Target Options

LUT Combining : Auto
Reduce Control Sets : Auto
Add IO Buffers : YES
Global Maximum Fanout : 100000
Add Generic Clock Buffer(BUFG) : 16
Register Duplication : YES
Optimize Instantiated Primitives : NO
Use Clock Enable : Auto
Use Synchronous Set : Auto
Use Synchronous Reset : Auto
Pack IO Registers into IOBs : Auto
Equivalent register Removal : YES

----- General Options

Optimization Goal : Speed
Optimization Effort : 1
Power Reduction : NO
Keep Hierarchy : No
Netlist Hierarchy : As_Optimized
RTL Output : Yes
Global Optimization : AllClockNets
Read Cores : YES
Write Timing Constraints : NO
Cross Clock Analysis : NO
Hierarchy Separator : /
Bus Delimiter : <>
Case Specifier : Maintain
Slice Utilization Ratio : 100
BRAM Utilization Ratio : 100
DSP48 Utilization Ratio : 100
Auto BRAM Packing : NO
Slice Utilization Ratio Delta : 5

=====

=====

* HDL Parsing *

=====

Parsing VHDL file "64240430\unary_op_xor_tree_lut6.vhd" into library work
Parsing entity <XorTreeStage>.
Parsing architecture <tree_of_xor_lut6> of entity <xortreestage>.
Parsing VHDL file "64240430\unary_op_tree.vhd" into library work
Parsing entity <Unary_Op_Bin_Tree>.
Parsing architecture <t> of entity <unary_op_bin_tree>.

```
=====
*          HDL Elaboration          *
=====
```

Elaborating entity <Unary_Op_Bin_Tree> (architecture <t>) with generics from library <work>.

Elaborating entity <XorTreeStage> (architecture <tree_of_xor_lut6>) with generics from library <work>.

Elaborating entity <XorTreeStage> (architecture <tree_of_xor_lut6>) with generics from library <work>.

Elaborating entity <XorTreeStage> (architecture <tree_of_xor_lut6>) with generics from library <work>.

Elaborating entity <XorTreeStage> (architecture <tree_of_xor_lut6>) with generics from library <work>.

Elaborating entity <XorTreeStage> (architecture <tree_of_xor_lut6>) with generics from library <work>.

Elaborating entity <XorTreeStage> (architecture <tree_of_xor_lut6>) with generics from library <work>.

Elaborating entity <XorTreeStage> (architecture <tree_of_xor_lut6>) with generics from library <work>.

Elaborating entity <XorTreeStage> (architecture <tree_of_xor_lut6>) with generics from library <work>.

Elaborating entity <XorTreeStage> (architecture <tree_of_xor_lut6>) with generics from library <work>.

```
=====
*          HDL Synthesis           *
=====
```

Synthesizing Unit <Unary_Op_Bin_Tree>.
Related source file is "64240430\unary_op_tree.vhd".
N = 4096
Summary:
no macro.
Unit <Unary_Op_Bin_Tree> synthesized.

Synthesizing Unit <XorTreeStage_1>.
Related source file is "64240430\unary_op_xor_tree_lut6.vhd".
N = 4096
Summary:
no macro.
Unit <XorTreeStage_1> synthesized.

Synthesizing Unit <XorTreeStage_2>.
Related source file is "64240430\unary_op_xor_tree_lut6.vhd".
N = 682
Summary:
no macro.
Unit <XorTreeStage_2> synthesized.

Synthesizing Unit <XorTreeStage_3>.
Related source file is "64240430\unary_op_xor_tree_lut6.vhd".
N = 113
Summary:
no macro.
Unit <XorTreeStage_3> synthesized.

Synthesizing Unit <XorTreeStage_4>.
Related source file is "64240430\unary_op_xor_tree_lut6.vhd".
N = 18
Summary:
no macro.
Unit <XorTreeStage_4> synthesized.

Synthesizing Unit <XorTreeStage_5>.
Related source file is "64240430\unary_op_xor_tree_lut6.vhd".
N = 3
Summary:
no macro.
Unit <XorTreeStage_5> synthesized.

Synthesizing Unit <XorTreeStage_6>.
Related source file is "64240430\unary_op_xor_tree_lut6.vhd".
N = 19
Summary:
no macro.
Unit <XorTreeStage_6> synthesized.

Synthesizing Unit <XorTreeStage_7>.
Related source file is "64240430\unary_op_xor_tree_lut6.vhd".
N = 4
Summary:
no macro.
Unit <XorTreeStage_7> synthesized.

Synthesizing Unit <XorTreeStage_8>.
Related source file is "64240430\unary_op_xor_tree_lut6.vhd".
N = 114
Summary:
no macro.
Unit <XorTreeStage_8> synthesized.

Synthesizing Unit <XorTreeStage_9>.
Related source file is "64240430\unary_op_xor_tree_lut6.vhd".
N = 683
Summary:
no macro.
Unit <XorTreeStage_9> synthesized.

=====
HDL Synthesis Report

Found no macro

```
=====
*      Advanced HDL Synthesis      *
=====
```

```
=====
Advanced HDL Synthesis Report
=====
```

Found no macro

```
=====
*      Low Level Synthesis      *
=====
```

Optimizing unit <Unary_Op_Bin_Tree> ...

Mapping all equations...

Building and optimizing final netlist ...

Found area constraint ratio of 100 (+ 5) on block Unary_Op_Bin_Tree, actual ratio is 94.

Final Macro Processing ...

```
=====
Final Register Report
=====
```

Found no macro

```
=====
*      Partition Report      *
=====
```

Partition Implementation Status

No Partitions were found in this design.

```
=====
*      Design Summary      *
=====
```

Top Level Output File Name : Unary_Op_Bin_Tree.ngc

Primitive and Black Box Usage:

# BELS	: 1555
# LUT3	: 1088
# LUT4	: 208
# LUT6	: 259
# IO Buffers	: 4097
# IBUF	: 4096
# OBUF	: 1

Device utilization summary:

Selected Device : 6slx4tqg144-3

Slice Logic Utilization:

Number of Slice LUTs: 1555 out of 2400 64%
Number used as Logic: 1555 out of 2400 64%

Slice Logic Distribution:

Number of LUT Flip Flop pairs used: 1555
Number with an unused Flip Flop: 1555 out of 1555 100%
Number with an unused LUT: 0 out of 1555 0%
Number of fully used LUT-FF pairs: 0 out of 1555 0%
Number of unique control sets: 0

IO Utilization:

Number of IOs: 4097
Number of bonded IOBs: 4097 out of 102 4016% (*)

Specific Feature Utilization:

WARNING:Xst:1336 - (*) More than 100% of Device resources are used

Partition Resource Summary:

No Partitions were found in this design.

=====

Timing Report

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.
FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT
GENERATED AFTER PLACE-and-ROUTE.

Clock Information:

No clock signals found in this design

Asynchronous Control Signals Information:

No asynchronous control signals found in this design

Timing Summary:

Speed Grade: -3

Minimum period: No path found
Minimum input arrival time before clock: No path found
Maximum output required time after clock: No path found
Maximum combinational path delay: 10.106ns

Timing Details:

All values displayed in nanoseconds (ns)

```

=====
Timing constraint: Default path analysis
Total number of paths / destination ports: 4096 / 1
-----
Delay: 10.106ns (Levels of Logic = 7)
Source: I<0> (PAD)
Destination: O_Xor (PAD)

Data Path: I<0> to O_Xor
Gate Net
Cell:in->out fanout Delay Delay Logical Name (Net Name)
-----
IBUF:I->O 1 1.222 0.808 I_0_IBUF (I_0_IBUF)
LUT3:I0->O 1 0.339 0.944
U_Xor/Stages.xor_tree1/Stages.xor_tree1/Stages.xor_tree1/Stage_xo
r_3.XOR3_LUT
(U_Xor/Stages.xor_tree1/Stages.xor_tree1/Stages.xor_tree1/Stages.Sixth1_out)
LUT6:I0->O 1 0.203 0.944
U_Xor/Stages.xor_tree1/Stages.xor_tree1/Stages.xor_tree1/Stages.XOR6_LUT
(U_Xor/Stages.xor_tree1/Stages.xor_tree1/Stages.Sixth1_out)
LUT6:I0->O 1 0.203 0.944
U_Xor/Stages.xor_tree1/Stages.xor_tree1/Stages.XOR6_LUT
(U_Xor/Stages.xor_tree1/Stages.Sixth1_out)
LUT6:I0->O 1 0.203 0.944 U_Xor/Stages.xor_tree1/Stages.XOR6_LUT
(U_Xor/Stages.Sixth1_out)
LUT6:I0->O 1 0.203 0.579 U_Xor/Stages.XOR6_LUT (O_Xor_OBUF)
OBUF:I->O 2.571 O_Xor_OBUF (O_Xor)
-----
Total 10.106ns (4.944ns logic, 5.162ns route)
(48.9% logic, 51.1% route)
=====

```

Cross Clock Domains Report:

```

-----
Total REAL time to Xst completion: 17.00 secs
Total CPU time to Xst completion: 17.16 secs

```

-->

Total memory usage is 4538332 kilobytes

```

Number of errors : 0 ( 0 filtered)
Number of warnings : 1 ( 0 filtered)
Number of infos : 0 ( 0 filtered)

```

```

64240430>fuse -incremental -o unary_tree_tb_isim_beh.exe -prj unary_tree_tb.prj -
top Unary_Op_Bin_Tree_tb
Running: C:\Xilinx\14.7\ISE_DS\ISE\bin\nt64\unwrapped\fuse.exe -incremental -o
unary_tree_tb_isim_beh.exe -prj unary_tree_tb.prj -top Unary_Op_Bin_Tree_tb
ISim P.20131013 (signature 0x7708f090)
Number of CPUs detected in this system: 8
Turning on mult-threading, number of parallel sub-compilation jobs: 16
Determining compilation order of HDL files
Parsing VHDL file "slv_image_pkg.vhd" into library work

```

```
Parsing VHDL file "unary_op_xor_tree_lut6.vhd" into library work
Parsing VHDL file "unary_op_tree.vhd" into library work
Parsing VHDL file "unary_op_tree_IDEAL_tb.vhd" into library work
Starting static elaboration
Completed static elaboration
Compiling package standard
Compiling package std_logic_1164
Compiling package numeric_std
Compiling package textio
Compiling package std_logic_textio
Compiling package slv_image_pkg
Compiling package vcomponents
Compiling package vital_timing
Compiling package vital_primitives
Compiling package vpkg
Compiling architecture tree_of_xor_lut6 of entity XorTreeStage [\XorTreeStage(2)\]
Compiling architecture lut3_v of entity LUT3 [\LUT3("10010110")(0,7)\]
Compiling architecture tree_of_xor_lut6 of entity XorTreeStage [\XorTreeStage(3)\]
Compiling architecture lut6_v of entity LUT6 [\LUT6("0110100110010110100101100...")
Compiling architecture tree_of_xor_lut6 of entity XorTreeStage
[\XorTreeStage(16)\]
Compiling architecture t of entity Unary_Op_Bin_Tree [\Unary_Op_Bin_Tree(16)\]
Compiling architecture test of entity unary_op_bin_tree_tb
Time Resolution for simulation is 1ps.
Waiting for 1 sub-compilation(s) to finish...
Compiled 23 VHDL Units
Built simulation executable unary_tree_tb_isim_beh.exe
Fuse Memory Usage: 59908 KB
Fuse CPU Usage: 1311 ms
```

```
64240430>if exist Unary_Op_Bin_Tree.csv del Unary_Op_Bin_Tree.csv
```

```
64240430>if exist Unary_Op_Bin_Tree_64240430.csv del
Unary_Op_Bin_Tree_64240430.csv
```

```
64240430>unary_tree_tb_isim_beh.exe -tclbatch isim.tcl -wdb
unary_tree_tb_isim_beh.wdb
ISim P.20131013 (signature 0x7708f090)
WARNING: A WEBPACK license was found.
WARNING: Please use Xilinx License Configuration Manager to check out a full ISim
license.
WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for
more information on the differences between the Lite and the Full version.
This is a Lite version of ISim.
Time resolution is 1 ps
Simulator is doing circuit initialization process.
Finished circuit initialization process.
```

```
64240430>rem ren Unary_Op_Bin_Tree.csv Unary_Op_Bin_Tree_64240430.csv
```

```
64240430>xst -ifn unary_vhdl93.xst
Release 14.7 - xst P.20131013 (nt64)
Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.
--> Parameter TMPDIR set to xst/projnav.tmp
```

```
Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.24 secs
```

```
--> Parameter xsthdpdir set to xst
```


Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.24 secs

-->

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```
=====
*      Synthesis Options Summary      *
=====
```

---- Source Parameters

Input File Name : "./unary_vhdl93.prj"
Ignore Synthesis Constraint File : NO

---- Target Parameters

Output File Name : "reduction_operators"
Output Format : NGC
Target Device : xc6slx4-3-tqg144

---- Source Options

Top Module Name : reduction_operators
Automatic FSM Extraction : YES
FSM Encoding Algorithm : Auto
Safe Implementation : No
FSM Style : LUT
RAM Extraction : Yes
RAM Style : Auto
ROM Extraction : Yes
Shift Register Extraction : YES
ROM Style : Auto
Resource Sharing : YES
Asynchronous To Synchronous : NO
Shift Register Minimum Size : 2
Use DSP Block : Auto
Automatic Register Balancing : No

---- Target Options

LUT Combining : Auto
Reduce Control Sets : Auto
Add IO Buffers : YES

Global Maximum Fanout : 100000
Add Generic Clock Buffer(BUFG) : 16
Register Duplication : YES
Optimize Instantiated Primitives : NO
Use Clock Enable : Auto
Use Synchronous Set : Auto
Use Synchronous Reset : Auto
Pack IO Registers into IOBs : Auto
Equivalent register Removal : YES

---- General Options

Optimization Goal : Speed
Optimization Effort : 1
Power Reduction : NO
Keep Hierarchy : No
Netlist Hierarchy : As_Optimized
RTL Output : Yes
Global Optimization : AllClockNets
Read Cores : YES
Write Timing Constraints : NO
Cross Clock Analysis : NO
Hierarchy Separator : /
Bus Delimiter : <>
Case Specifier : Maintain
Slice Utilization Ratio : 100
BRAM Utilization Ratio : 100
DSP48 Utilization Ratio : 100
Auto BRAM Packing : NO
Slice Utilization Ratio Delta : 5

=====

=====

* HDL Parsing *

=====

Parsing VHDL file "64240430\unary_operators_vhdl_93.vhd" into library work
Parsing entity <reduction_operators>.
Parsing architecture <vhdl_93_process> of entity <reduction_operators>.

=====

* HDL Elaboration *

=====

Elaborating entity <reduction_operators> (architecture <vhdl_93_process>) with
generics from library <work>.

=====

* HDL Synthesis *

=====

Synthesizing Unit <reduction_operators>.
Related source file is "64240430\unary_operators_vhdl_93.vhd".
N = 10
Summary:
inferred 20 Multiplexer(s).
Unit <reduction_operators> synthesized.

=====

HDL Synthesis Report

Macro Statistics

Multiplexers : 20
1-bit 2-to-1 multiplexer : 20
Xors : 1
1-bit xor10 : 1

=====

* Advanced HDL Synthesis *

=====

Advanced HDL Synthesis Report

Macro Statistics

Multiplexers : 20
1-bit 2-to-1 multiplexer : 20
Xors : 1
1-bit xor10 : 1

=====

* Low Level Synthesis *

=====

Optimizing unit <reduction_operators> ...

Mapping all equations...

Building and optimizing final netlist ...

Found area constraint ratio of 100 (+ 5) on block reduction_operators, actual ratio is 0.

Final Macro Processing ...

=====

Final Register Report

Found no macro

=====

* Partition Report *

=====

Partition Implementation Status

No Partitions were found in this design.

=====

* Design Summary *

=====

Top Level Output File Name : reduction_operators.ngc

Primitive and Black Box Usage:

```
-----  
# BELS           : 6  
# LUT5           : 3  
# LUT6           : 3  
# IO Buffers     : 13  
# IBUF           : 10  
# OBUF           : 3
```

Device utilization summary:

Selected Device : 6slx4tqg144-3

Slice Logic Utilization:

Number of Slice LUTs: 6 out of 2400 0%
Number used as Logic: 6 out of 2400 0%

Slice Logic Distribution:

Number of LUT Flip Flop pairs used: 6
Number with an unused Flip Flop: 6 out of 6 100%
Number with an unused LUT: 0 out of 6 0%
Number of fully used LUT-FF pairs: 0 out of 6 0%
Number of unique control sets: 0

IO Utilization:

Number of IOs: 13
Number of bonded IOBs: 13 out of 102 12%

Specific Feature Utilization:

Partition Resource Summary:

No Partitions were found in this design.

=====
Timing Report

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.
FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT
GENERATED AFTER PLACE-and-ROUTE.

Clock Information:

No clock signals found in this design

Asynchronous Control Signals Information:

No asynchronous control signals found in this design

Timing Summary:

Speed Grade: -3

Minimum period: No path found
Minimum input arrival time before clock: No path found
Maximum output required time after clock: No path found
Maximum combinational path delay: 6.355ns

Timing Details:

All values displayed in nanoseconds (ns)

Timing constraint: Default path analysis

Total number of paths / destination ports: 30 / 3

Delay: 6.355ns (Levels of Logic = 4)

Source: A<4> (PAD)

Destination: reduced_OR (PAD)

Data Path: A<4> to reduced_OR

Gate Net

Cell:in->out fanout Delay Delay Logical Name (Net Name)

IBUF:I->O	3	1.222	0.995	A_4_IBUF	(A_4_IBUF)
LUT5:I0->O	1	0.203	0.580	Mxor_reduced_XOR_xo<0>_SW0	(N01)
LUT6:I5->O	1	0.205	0.579	Mxor_reduced_XOR_xo<0>	(reduced_XOR_OBUF)
OBUF:I->O		2.571		reduced_XOR_OBUF	(reduced_XOR)

Total 6.355ns (4.201ns logic, 2.154ns route)
(66.1% logic, 33.9% route)

Cross Clock Domains Report:

Total REAL time to Xst completion: 8.00 secs

Total CPU time to Xst completion: 7.87 secs

-->

Total memory usage is 4487516 kilobytes

Number of errors : 0 (0 filtered)

Number of warnings : 0 (0 filtered)

Number of infos : 0 (0 filtered)

64240430>fuse -incremental -o unary_vhdl93_tb_isim_beh.exe -prj

unary_vhdl93_tb.prj -top reduction_operators_tb

Running: C:\Xilinx\14.7\ISE_DS\ISE\bin\nt64\unwrapped\fuse.exe -incremental -o
unary_vhdl93_tb_isim_beh.exe -prj unary_vhdl93_tb.prj -top reduction_operators_tb

ISim P.20131013 (signature 0x7708f090)

Number of CPUs detected in this system: 8

Turning on mult-threading, number of parallel sub-compilation jobs: 16

Determining compilation order of HDL files

Parsing VHDL file "unary_operators_vhdl_93.vhd" into library work

Parsing VHDL file "unary_operators_vhdl93_IDEAL_tb.vhd" into library work

Starting static elaboration

Completed static elaboration

```
Compiling package standard
Compiling package std_logic_1164
Compiling package numeric_std
Compiling package textio
Compiling package std_logic_textio
Compiling architecture vhd1_93_process of entity reduction_operators
[\\reduction_operators(3)\\]
Compiling architecture test of entity reduction_operators_tb
Time Resolution for simulation is 1ps.
Waiting for 1 sub-compilation(s) to finish...
Compiled 8 VHDL Units
Built simulation executable unary_vhdl93_tb_isim_beh.exe
Fuse Memory Usage: 36788 KB
Fuse CPU Usage: 874 ms
```

```
64240430>if exist reduction_operators.csv del reduction_operators.csv
```

```
64240430>if exist reduction_operators_64240430.csv del
reduction_operators_64240430.csv
```

```
64240430>unary_vhdl93_tb_isim_beh.exe -tclbatch isim.tcl -wdb
unary_vhdl93_tb_isim_beh.wdb
ISim P.20131013 (signature 0x7708f090)
WARNING: A WEBPACK license was found.
WARNING: Please use Xilinx License Configuration Manager to check out a full ISim
license.
WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for
more information on the differences between the Lite and the Full version.
This is a Lite version of ISim.
Time resolution is 1 ps
Simulator is doing circuit initialization process.
Finished circuit initialization process.
```

```
64240430>ren ren reduction_operators.csv reduction_operators_64240430.csv
```

```
-- *****
-- **** STUDENT: IDEAL
-- *****
-- KOMENTARJI K OCENI NALOGE
-- Matej Možek: Ni pripomb
-- *****
```

```
IDEAL>if not exist "xst" mkdir xst
```

```
IDEAL>cd XST
```

```
IDEAL\xst>if not exist "projnav.tmp" mkdir "projnav.tmp"
```

```
IDEAL\xst>cd ..
```

```
IDEAL>xst -ifn unary_tree.xst
Release 14.7 - xst P.20131013 (nt64)
Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.
--> Parameter TMPDIR set to xst/projnav.tmp
```

```
Total REAL time to Xst completion: 8.00 secs
Total CPU time to Xst completion: 7.84 secs
```

```
--> Parameter xsthdpdir set to xst
```

```
Total REAL time to Xst completion: 8.00 secs
Total CPU time to Xst completion: 7.85 secs
```

```
-->
```

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 - 8.4.5) Cross Clock Domains Report

```
=====
*      Synthesis Options Summary      *
=====
```

---- Source Parameters

```
Input File Name      : "unary_tree.prj"
Ignore Synthesis Constraint File : NO
```

---- Target Parameters

```
Output File Name     : "Unary_Op_Bin_Tree"
```

Output Format : NGC
Target Device : xc6slx4-3-tqg144

----- Source Options

Top Module Name : Unary_Op_Bin_Tree
Automatic FSM Extraction : YES
FSM Encoding Algorithm : Auto
Safe Implementation : No
FSM Style : LUT
RAM Extraction : Yes
RAM Style : Auto
ROM Extraction : Yes
Shift Register Extraction : YES
ROM Style : Auto
Resource Sharing : YES
Asynchronous To Synchronous : NO
Shift Register Minimum Size : 2
Use DSP Block : Auto
Automatic Register Balancing : No

----- Target Options

LUT Combining : Auto
Reduce Control Sets : Auto
Add IO Buffers : YES
Global Maximum Fanout : 100000
Add Generic Clock Buffer(BUFG) : 16
Register Duplication : YES
Optimize Instantiated Primitives : NO
Use Clock Enable : Auto
Use Synchronous Set : Auto
Use Synchronous Reset : Auto
Pack IO Registers into IOBs : Auto
Equivalent register Removal : YES

----- General Options

Optimization Goal : Speed
Optimization Effort : 1
Power Reduction : NO
Keep Hierarchy : No
Netlist Hierarchy : As_Optimized
RTL Output : Yes
Global Optimization : AllClockNets
Read Cores : YES
Write Timing Constraints : NO
Cross Clock Analysis : NO
Hierarchy Separator : /
Bus Delimiter : <>
Case Specifier : Maintain
Slice Utilization Ratio : 100
BRAM Utilization Ratio : 100
DSP48 Utilization Ratio : 100
Auto BRAM Packing : NO
Slice Utilization Ratio Delta : 5

=====

=====

* HDL Parsing *

=====

Parsing VHDL file "IDEAL\unary_op_xor_tree_lut6.vhd" into library work
Parsing entity <XorTreeStage>.
Parsing architecture <tree_of_xor_lut6> of entity <xortreestage>.
Parsing VHDL file "IDEAL\unary_op_tree.vhd" into library work
Parsing entity <Unary_Op_Bin_Tree>.
Parsing architecture <t> of entity <unary_op_bin_tree>.

```
=====
*          HDL Elaboration          *
=====
```

Elaborating entity <Unary_Op_Bin_Tree> (architecture <t>) with generics from library <work>.

Elaborating entity <XorTreeStage> (architecture <tree_of_xor_lut6>) with generics from library <work>.

Elaborating entity <XorTreeStage> (architecture <tree_of_xor_lut6>) with generics from library <work>.

Elaborating entity <XorTreeStage> (architecture <tree_of_xor_lut6>) with generics from library <work>.

Elaborating entity <XorTreeStage> (architecture <tree_of_xor_lut6>) with generics from library <work>.

Elaborating entity <XorTreeStage> (architecture <tree_of_xor_lut6>) with generics from library <work>.

Elaborating entity <XorTreeStage> (architecture <tree_of_xor_lut6>) with generics from library <work>.

Elaborating entity <XorTreeStage> (architecture <tree_of_xor_lut6>) with generics from library <work>.

Elaborating entity <XorTreeStage> (architecture <tree_of_xor_lut6>) with generics from library <work>.

Elaborating entity <XorTreeStage> (architecture <tree_of_xor_lut6>) with generics from library <work>.

```
=====
*          HDL Synthesis            *
=====
```

Synthesizing Unit <Unary_Op_Bin_Tree>.
Related source file is "IDEAL\unary_op_tree.vhd".
N = 4096
Summary:
no macro.
Unit <Unary_Op_Bin_Tree> synthesized.

Synthesizing Unit <XorTreeStage_1>.
Related source file is "IDEAL\unary_op_xor_tree_lut6.vhd".
N = 4096
Summary:
no macro.
Unit <XorTreeStage_1> synthesized.

Synthesizing Unit <XorTreeStage_2>.
Related source file is "IDEAL\unary_op_xor_tree_lut6.vhd".
N = 682
Summary:
no macro.
Unit <XorTreeStage_2> synthesized.

Synthesizing Unit <XorTreeStage_3>.
Related source file is "IDEAL\unary_op_xor_tree_lut6.vhd".
N = 113
Summary:
no macro.
Unit <XorTreeStage_3> synthesized.

Synthesizing Unit <XorTreeStage_4>.
Related source file is "IDEAL\unary_op_xor_tree_lut6.vhd".
N = 18
Summary:
no macro.
Unit <XorTreeStage_4> synthesized.

Synthesizing Unit <XorTreeStage_5>.
Related source file is "IDEAL\unary_op_xor_tree_lut6.vhd".
N = 3
Summary:
no macro.
Unit <XorTreeStage_5> synthesized.

Synthesizing Unit <XorTreeStage_6>.
Related source file is "IDEAL\unary_op_xor_tree_lut6.vhd".
N = 19
Summary:
no macro.
Unit <XorTreeStage_6> synthesized.

Synthesizing Unit <XorTreeStage_7>.
Related source file is "IDEAL\unary_op_xor_tree_lut6.vhd".
N = 4
Summary:
no macro.
Unit <XorTreeStage_7> synthesized.

Synthesizing Unit <XorTreeStage_8>.
Related source file is "IDEAL\unary_op_xor_tree_lut6.vhd".
N = 114
Summary:
no macro.
Unit <XorTreeStage_8> synthesized.

Synthesizing Unit <XorTreeStage_9>.
Related source file is "IDEAL\unary_op_xor_tree_lut6.vhd".
N = 683
Summary:
no macro.
Unit <XorTreeStage_9> synthesized.

=====
HDL Synthesis Report

Found no macro

```
=====
*      Advanced HDL Synthesis      *
```

```
=====
Advanced HDL Synthesis Report
```

Found no macro

```
=====
*      Low Level Synthesis      *
```

Optimizing unit <Unary_Op_Bin_Tree> ...

Mapping all equations...

Building and optimizing final netlist ...

Found area constraint ratio of 100 (+ 5) on block Unary_Op_Bin_Tree, actual ratio is 94.

Final Macro Processing ...

```
=====
Final Register Report
```

Found no macro

```
=====
*      Partition Report      *
```

Partition Implementation Status

No Partitions were found in this design.

```
=====
*      Design Summary      *
```

Top Level Output File Name : Unary_Op_Bin_Tree.ngc

Primitive and Black Box Usage:

# BELS	: 1555
# LUT3	: 1088
# LUT4	: 208
# LUT6	: 259
# IO Buffers	: 4097
# IBUF	: 4096
# OBUF	: 1

Device utilization summary:

Selected Device : 6slx4tqg144-3

Slice Logic Utilization:

Number of Slice LUTs: 1555 out of 2400 64%
Number used as Logic: 1555 out of 2400 64%

Slice Logic Distribution:

Number of LUT Flip Flop pairs used: 1555
Number with an unused Flip Flop: 1555 out of 1555 100%
Number with an unused LUT: 0 out of 1555 0%
Number of fully used LUT-FF pairs: 0 out of 1555 0%
Number of unique control sets: 0

IO Utilization:

Number of IOs: 4097
Number of bonded IOBs: 4097 out of 102 4016% (*)

Specific Feature Utilization:

WARNING:Xst:1336 - (*) More than 100% of Device resources are used

Partition Resource Summary:

No Partitions were found in this design.

=====

Timing Report

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.
FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT
GENERATED AFTER PLACE-and-ROUTE.

Clock Information:

No clock signals found in this design

Asynchronous Control Signals Information:

No asynchronous control signals found in this design

Timing Summary:

Speed Grade: -3

Minimum period: No path found
Minimum input arrival time before clock: No path found
Maximum output required time after clock: No path found
Maximum combinational path delay: 10.106ns

Timing Details:

All values displayed in nanoseconds (ns)

```

=====
Timing constraint: Default path analysis
Total number of paths / destination ports: 4096 / 1
-----
Delay: 10.106ns (Levels of Logic = 7)
Source: I<0> (PAD)
Destination: O_Xor (PAD)

Data Path: I<0> to O_Xor
Gate Net
Cell:in->out fanout Delay Delay Logical Name (Net Name)
-----
IBUF:I->O 1 1.222 0.808 I_0_IBUF (I_0_IBUF)
LUT3:I0->O 1 0.339 0.944
U_Xor/Stages.Sixth1_Tree/Stages.Sixth1_Tree/Stages.Sixth1_Tree/Stages.Sixth1_Tree/
Stage_xor_3.XOR3_LUT
(U_Xor/Stages.Sixth1_Tree/Stages.Sixth1_Tree/Stages.Sixth1_Tree/Stages.Sixth1_out)
LUT6:I0->O 1 0.203 0.944
U_Xor/Stages.Sixth1_Tree/Stages.Sixth1_Tree/Stages.Sixth1_Tree/Stages.XOR6_LUT
(U_Xor/Stages.Sixth1_Tree/Stages.Sixth1_Tree/Stages.Sixth1_out)
LUT6:I0->O 1 0.203 0.944
U_Xor/Stages.Sixth1_Tree/Stages.Sixth1_Tree/Stages.XOR6_LUT
(U_Xor/Stages.Sixth1_Tree/Stages.Sixth1_out)
LUT6:I0->O 1 0.203 0.944 U_Xor/Stages.Sixth1_Tree/Stages.XOR6_LUT
(U_Xor/Stages.Sixth1_out)
LUT6:I0->O 1 0.203 0.579 U_Xor/Stages.XOR6_LUT (O_Xor_OBUF)
OBUF:I->O 2.571 O_Xor_OBUF (O_Xor)
-----
Total 10.106ns (4.944ns logic, 5.162ns route)
(48.9% logic, 51.1% route)
=====

```

Cross Clock Domains Report:

```

=====
Total REAL time to Xst completion: 31.00 secs
Total CPU time to Xst completion: 31.03 secs

```

-->

Total memory usage is 4569728 kilobytes

```

Number of errors : 0 ( 0 filtered)
Number of warnings : 1 ( 0 filtered)
Number of infos : 0 ( 0 filtered)

```

```

IDEAL>fuse -incremental -o unary_tree_tb_isim_beh.exe -prj unary_tree_tb.prj -top
Unary_Op_Bin_Tree_tb
Running: C:\Xilinx\14.7\ISE_DS\ISE\bin\nt64\unwrapped\fuse.exe -incremental -o
unary_tree_tb_isim_beh.exe -prj unary_tree_tb.prj -top Unary_Op_Bin_Tree_tb
ISim P.20131013 (signature 0x7708f090)
Number of CPUs detected in this system: 8
Turning on mult-threading, number of parallel sub-compilation jobs: 16
Determining compilation order of HDL files
Parsing VHDL file "slv_image_pkg.vhd" into library work

```

```

Parsing VHDL file "unary_op_xor_tree_lut6.vhd" into library work
Parsing VHDL file "unary_op_tree.vhd" into library work
Parsing VHDL file "unary_op_tree_IDEAL_tb.vhd" into library work
Starting static elaboration
Completed static elaboration
Compiling package standard
Compiling package std_logic_1164
Compiling package numeric_std
Compiling package textio
Compiling package std_logic_textio
Compiling package slv_image_pkg
Compiling package vcomponents
Compiling package vital_timing
Compiling package vital_primitives
Compiling package vpkg
Compiling architecture lut2_v of entity LUT2 [\LUT2("0110")(0,3)\]
Compiling architecture tree_of_xor_lut6 of entity XorTreeStage [\XorTreeStage(2)\]
Compiling architecture lut3_v of entity LUT3 [\LUT3("10010110")(0,7)\]
Compiling architecture tree_of_xor_lut6 of entity XorTreeStage [\XorTreeStage(3)\]
Compiling architecture lut6_v of entity LUT6 [\LUT6("01101001100101100100101100...)]
Compiling architecture tree_of_xor_lut6 of entity XorTreeStage
[\XorTreeStage(16)\]
Compiling architecture t of entity Unary_Op_Bin_Tree [\Unary_Op_Bin_Tree(16)\]
Compiling architecture test of entity unary_op_bin_tree_tb
Time Resolution for simulation is 1ps.
Waiting for 2 sub-compilation(s) to finish...
Compiled 25 VHDL Units
Built simulation executable unary_tree_tb_isim_beh.exe
Fuse Memory Usage: 59944 KB
Fuse CPU Usage: 1280 ms

```

```

IDEAL>if exist Unary_Op_Bin_Tree.csv del Unary_Op_Bin_Tree.csv

```

```

IDEAL>if exist Unary_Op_Bin_Tree_IDEAL.csv del Unary_Op_Bin_Tree_IDEAL.csv

```

```

IDEAL>unary_tree_tb_isim_beh.exe -tclbatch isim.tcl -wdb
unary_tree_tb_isim_beh.wdb
ISim P.20131013 (signature 0x7708f090)
WARNING: A WEBPACK license was found.
WARNING: Please use Xilinx License Configuration Manager to check out a full ISim
license.
WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for
more information on the differences between the Lite and the Full version.
This is a Lite version of ISim.
Time resolution is 1 ps
Simulator is doing circuit initialization process.
Finished circuit initialization process.

```

```

IDEAL>rem ren Unary_Op_Bin_Tree.csv Unary_Op_Bin_Tree_IDEAL.csv

```

```

IDEAL>xst -ifn unary_vhdl93.xst
Release 14.7 - xst P.20131013 (nt64)
Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.
--> Parameter TMPDIR set to xst/projnav.tmp

```

```

Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.23 secs

```

```

--> Parameter xsthdpdir set to xst

```

Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.23 secs

-->

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 - 8.4.3) Timing Summary
 - 8.4.4) Timing Details
 - 8.4.5) Cross Clock Domains Report

```
=====
*      Synthesis Options Summary      *
=====
```

---- Source Parameters

Input File Name : "./unary_vhdl93.prj"
Ignore Synthesis Constraint File : NO

---- Target Parameters

Output File Name : "reduction_operators"
Output Format : NGC
Target Device : xc6slx4-3-tqg144

---- Source Options

Top Module Name : reduction_operators
Automatic FSM Extraction : YES
FSM Encoding Algorithm : Auto
Safe Implementation : No
FSM Style : LUT
RAM Extraction : Yes
RAM Style : Auto
ROM Extraction : Yes
Shift Register Extraction : YES
ROM Style : Auto
Resource Sharing : YES
Asynchronous To Synchronous : NO
Shift Register Minimum Size : 2
Use DSP Block : Auto
Automatic Register Balancing : No

---- Target Options

LUT Combining : Auto
Reduce Control Sets : Auto
Add IO Buffers : YES

Global Maximum Fanout : 100000
Add Generic Clock Buffer(BUFG) : 16
Register Duplication : YES
Optimize Instantiated Primitives : NO
Use Clock Enable : Auto
Use Synchronous Set : Auto
Use Synchronous Reset : Auto
Pack IO Registers into IOBs : Auto
Equivalent register Removal : YES

---- General Options

Optimization Goal : Speed
Optimization Effort : 1
Power Reduction : NO
Keep Hierarchy : No
Netlist Hierarchy : As_Optimized
RTL Output : Yes
Global Optimization : AllClockNets
Read Cores : YES
Write Timing Constraints : NO
Cross Clock Analysis : NO
Hierarchy Separator : /
Bus Delimiter : <>
Case Specifier : Maintain
Slice Utilization Ratio : 100
BRAM Utilization Ratio : 100
DSP48 Utilization Ratio : 100
Auto BRAM Packing : NO
Slice Utilization Ratio Delta : 5

=====

=====

* HDL Parsing *

=====

Parsing VHDL file "IDEAL\unary_operators_vhdl_93.vhd" into library work
Parsing entity <reduction_operators>.
Parsing architecture <vhdl_93_comb> of entity <reduction_operators>.
Parsing architecture <vhdl_93_process> of entity <reduction_operators>.

=====

* HDL Elaboration *

=====

Elaborating entity <reduction_operators> (architecture <vhdl_93_process>) with
generics from library <work>.

=====

* HDL Synthesis *

=====

Synthesizing Unit <reduction_operators>.
Related source file is "IDEAL\unary_operators_vhdl_93.vhd".
N = 64
Summary:
inferred 128 Multiplexer(s).
Unit <reduction_operators> synthesized.

=====

HDL Synthesis Report

Macro Statistics

Multiplexers : 128
1-bit 2-to-1 multiplexer : 128
Xors : 1
1-bit xor64 : 1

* Advanced HDL Synthesis *

Advanced HDL Synthesis Report

Macro Statistics

Multiplexers : 128
1-bit 2-to-1 multiplexer : 128
Xors : 1
1-bit xor64 : 1

* Low Level Synthesis *

Optimizing unit <reduction_operators> ...

Mapping all equations...

Building and optimizing final netlist ...

Found area constraint ratio of 100 (+ 5) on block reduction_operators, actual ratio is 1.

Final Macro Processing ...

Final Register Report

Found no macro

* Partition Report *

Partition Implementation Status

No Partitions were found in this design.

* Design Summary *

Top Level Output File Name : reduction_operators.ngc

Primitive and Black Box Usage:

```
-----  
# BELS      : 59  
# GND       : 1  
# LUT4      : 3  
# LUT6      : 32  
# MUXCY     : 22  
# VCC       : 1  
# IO Buffers : 67  
# IBUF      : 64  
# OBUF      : 3
```

Device utilization summary:

Selected Device : 6slx4tqg144-3

Slice Logic Utilization:

Number of Slice LUTs: 35 out of 2400 1%
Number used as Logic: 35 out of 2400 1%

Slice Logic Distribution:

Number of LUT Flip Flop pairs used: 35
Number with an unused Flip Flop: 35 out of 35 100%
Number with an unused LUT: 0 out of 35 0%
Number of fully used LUT-FF pairs: 0 out of 35 0%
Number of unique control sets: 0

IO Utilization:

Number of IOs: 67
Number of bonded IOBs: 67 out of 102 65%

Specific Feature Utilization:

Partition Resource Summary:

No Partitions were found in this design.

=====

Timing Report

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.

FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT
GENERATED AFTER PLACE-and-ROUTE.

Clock Information:

No clock signals found in this design

Asynchronous Control Signals Information:

No asynchronous control signals found in this design

Timing Summary:

Speed Grade: -3

Minimum period: No path found

Minimum input arrival time before clock: No path found

Maximum output required time after clock: No path found

Maximum combinational path delay: 7.522ns

Timing Details:

All values displayed in nanoseconds (ns)

Timing constraint: Default path analysis

Total number of paths / destination ports: 192 / 3

Delay: 7.522ns (Levels of Logic = 5)

Source: A<22> (PAD)

Destination: reduced_XOR (PAD)

Data Path: A<22> to reduced_XOR

Gate Net

Cell:in->out fanout Delay Delay Logical Name (Net Name)

IBUF:I->O	3	1.222	1.015	A_22_IBUF	(A_22_IBUF)
LUT6:I0->O	1	0.203	0.944	Mxor_reduced_XOR_xo<0>3	(Mxor_reduced_XOR_xo<0>2)
LUT6:I0->O	1	0.203	0.580	Mxor_reduced_XOR_xo<0>14_SW0	(N01)
LUT6:I5->O	1	0.205	0.579	Mxor_reduced_XOR_xo<0>14	(reduced_XOR_OBUF)
OBUF:I->O	2.571			reduced_XOR_OBUF	(reduced_XOR)

Total 7.522ns (4.404ns logic, 3.118ns route)
(58.5% logic, 41.5% route)

Cross Clock Domains Report:

Total REAL time to Xst completion: 10.00 secs

Total CPU time to Xst completion: 10.29 secs

-->

Total memory usage is 4487516 kilobytes

Number of errors : 0 (0 filtered)

Number of warnings : 0 (0 filtered)

Number of infos : 0 (0 filtered)

IDEAL>fuse -incremental -o unary_vhdl93_tb_isim_beh.exe -prj unary_vhdl93_tb.prj -top reduction_operators_tb

Running: C:\Xilinx\14.7\ISE_DS\ISE\bin\nt64\unwrapped\fuse.exe -incremental -o unary_vhdl93_tb_isim_beh.exe -prj unary_vhdl93_tb.prj -top reduction_operators_tb
ISim P.20131013 (signature 0x7708f090)

Number of CPUs detected in this system: 8

Turning on mult-threading, number of parallel sub-compilation jobs: 16

```
Determining compilation order of HDL files
Parsing VHDL file "unary_operators_vhdl_93.vhd" into library work
Parsing VHDL file "unary_operators_vhdl93_IDEAL_tb.vhd" into library work
Starting static elaboration
Completed static elaboration
Compiling package standard
Compiling package std_logic_1164
Compiling package numeric_std
Compiling package textio
Compiling package std_logic_textio
Compiling architecture vhdl_93_process of entity reduction_operators
[\\reduction_operators(3)\\]
Compiling architecture test of entity reduction_operators_tb
Time Resolution for simulation is 1ps.
Waiting for 1 sub-compilation(s) to finish...
Compiled 8 VHDL Units
Built simulation executable unary_vhdl93_tb_isim_beh.exe
Fuse Memory Usage: 36784 KB
Fuse CPU Usage: 859 ms

IDEAL>if exist reduction_operators.csv del reduction_operators.csv

IDEAL>if exist reduction_operators_IDEAL.csv del reduction_operators_IDEAL.csv

IDEAL>unary_vhdl93_tb_isim_beh.exe -tclbatch isim.tcl -wdb
unary_vhdl93_tb_isim_beh.wdb
ISim P.20131013 (signature 0x7708f090)
WARNING: A WEBPACK license was found.
WARNING: Please use Xilinx License Configuration Manager to check out a full ISim
license.
WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for
more information on the differences between the Lite and the Full version.
This is a Lite version of ISim.
Time resolution is 1 ps
Simulator is doing circuit initialization process.
Finished circuit initialization process.

IDEAL>rem ren reduction_operators.csv reduction_operators_IDEAL.csv
```

