







--if not exists "tbl" create tbl		--if not exists "tbl" create tbl	
--add EXT		--add EXT	
--if not exists "synops.tbl" create "synops.tbl"		--if not exists "synops.tbl" create "synops.tbl"	
--set col		--set col	
--set: 40: user, time, net		--set: 40: user, time, net	
Release 14.7 - sat P.20131013 (r64)		Release 14.7 - sat P.20131013 (r64)	
Copyright (c) 1995-2013 Synopsys, Inc. All rights reserved.		Copyright (c) 1995-2013 Synopsys, Inc. All rights reserved.	
-- Parameter: TAPCORN not to verify synops.tbl		-- Parameter: TAPCORN not to verify synops.tbl	
Total HSA, time to 1st completion: 5.00 secs		Total HSA, time to 1st completion: 5.00 secs	
Total CPU time to 1st completion: 6.29 secs		Total CPU time to 1st completion: 7.84 secs	
-- Parameter: xrtzip not to zip		-- Parameter: xrtzip not to zip	
Total HSA, time to 1st completion: 6.00 secs		Total HSA, time to 1st completion: 6.00 secs	
Total CPU time to 1st completion: 6.33 secs		Total CPU time to 1st completion: 7.80 secs	
--		--	
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-- Synthesis Options Summary		-- Synthesis Options Summary	
-- Source Parameters		-- Source Parameters	
Input File Name: "user1_1000.prj"		Input File Name: "user1_1000.prj"	
Source Synthesis Constraint File: "NO"		Source Synthesis Constraint File: "NO"	
-- Target Parameters		-- Target Parameters	
Output File Name: "user1_Csp_Bin_Tier"		Output File Name: "user1_Csp_Bin_Tier"	
Output Format: "HCL"		Output Format: "HCL"	
Target Device: "xc7a100t-3-sg144"		Target Device: "xc7a100t-3-sg144"	
-- Source Options		-- Source Options	
Top Module Name: "user1_Csp_Bin_Tier"		Top Module Name: "user1_Csp_Bin_Tier"	
Automatic FSM Extraction: "YES"		Automatic FSM Extraction: "YES"	
FSM Encoding Algorithm: "Auto"		FSM Encoding Algorithm: "Auto"	
FSM Implementation: "No"		FSM Implementation: "No"	
FSM Style: "LUT"		FSM Style: "LUT"	
ROM Extraction: "Yes"		ROM Extraction: "Yes"	
ROM Style: "Auto"		ROM Style: "Auto"	
ROM Extraction: "Yes"		ROM Extraction: "Yes"	
Shift Register Extraction: "YES"		Shift Register Extraction: "YES"	
ROM Style: "Auto"		ROM Style: "Auto"	
Resource Sharing: "YES"		Resource Sharing: "YES"	
Asynchronous To Synchronous: "NO"		Asynchronous To Synchronous: "NO"	
Shift Register Minimum Size: "2"		Shift Register Minimum Size: "2"	
Use DSP Block: "Auto"		Use DSP Block: "Auto"	
Automatic Register Balancing: "No"		Automatic Register Balancing: "No"	
-- Target Options		-- Target Options	
LUT Combining: "Auto"		LUT Combining: "Auto"	
Device Control Bits: "Auto"		Device Control Bits: "Auto"	
Add IO Buffers: "YES"		Add IO Buffers: "YES"	
Global Memory Format: "100000"		Global Memory Format: "100000"	
Add Generic Check Buffer(BUFF0): "16"		Add Generic Check Buffer(BUFF0): "16"	





















if not exist "%x%" mkdir %x%	if not exist "%x%" mkdir %x%
cd %XST%	cd %XST%
del /f /q %xst%\loggen.log" mkdir "%loggen.log"	del /f /q %xst%\loggen.log" mkdir "%loggen.log"
setlocal	setlocal
%xst% && %xst% %xst% %xst%	%xst% && %xst% %xst% %xst%
Release: 18.7.1.180.20181013.0061	Release: 18.7.1.180.20181013.0061
Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.	Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.
-- Parameter: TARGET not to synthesise log	-- Parameter: TARGET not to synthesise log
Total PRAI time to Xst completion: 0.00 secs	Total PRAI time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.23 secs	Total CPU time to Xst completion: 0.23 secs
-- Parameter: autohelp not set	-- Parameter: autohelp not set
Total PRAI time to Xst completion: 0.00 secs	Total PRAI time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.23 secs	Total CPU time to Xst completion: 0.23 secs
--	--
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-- Synthesis Options Summary --	-- Synthesis Options Summary --
-- Source Parameters --	-- Source Parameters --
Input File Name: "xstgen_test.vf"	Input File Name: "xstgen_test.vf"
Usage Synthesis Constraints File: NO	Usage Synthesis Constraints File: NO
-- Target Parameters --	-- Target Parameters --
Output File Name: "xstgen_Op_Bin_Tim"	Output File Name: "xstgen_Op_Bin_Tim"
Output Format: NGC	Output Format: NGC
Target Device: xc6sxc100-3-qsg144	Target Device: xc6sxc100-3-qsg144
-- Block Options --	-- Block Options --
Top Module Name: User: Op_Bin_Tree	Top Module Name: User: Op_Bin_Tree
Automatic FSM Extraction: YES	Automatic FSM Extraction: YES
FSM Encoding Algorithm: Auto	FSM Encoding Algorithm: Auto
Safe Implementation: No	Safe Implementation: No
FSM Style: LUT	FSM Style: LUT
RAM Extraction: Yes	RAM Extraction: Yes
RAM Style: Auto	RAM Style: Auto
ROM Extraction: Yes	ROM Extraction: Yes
Shift Register Extraction: YES	Shift Register Extraction: YES
ROM Style: Auto	ROM Style: Auto
Resource Sharing: YES	Resource Sharing: YES
Asynchronous To Synchronous: NO	Asynchronous To Synchronous: NO
Shift Register Minimum Size: 2	Shift Register Minimum Size: 2
Use DSE Block: Auto	Use DSE Block: Auto
Automatic Register Balancing: No	Automatic Register Balancing: No
-- Target Options --	-- Target Options --
LUT Concurrency: Auto	LUT Concurrency: Auto
Reduce Control Bits: Auto	Reduce Control Bits: Auto
Asic IO Buffers: YES	Asic IO Buffers: YES
Global Maximum Fanout: 100000	Global Maximum Fanout: 100000
Asic General Clock Buffers(Buffers) : 18	Asic General Clock Buffers(Buffers) : 18













```
>if not exist "xst" mkdir xst
>cd XST
\xst>if not exist "projnav.tmp" mkdir "projnav.tmp"
\xst>cd ..
>xst -ifn unary_tree.xst
Release 14.7 - xst P.20131013 (nt64)
Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.
--> Parameter TMPDIR set to xst/projnav.tmp
Total REAL time to Xst completion: 8.00 secs
Total CPU time to Xst completion: 7.84 secs
```

```
--> Parameter xsthdmdir set to xst
Total REAL time to Xst completion: 8.00 secs
Total CPU time to Xst completion: 7.85 secs
```

-->

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\* Synthesis Options Summary \*

### ---- Source Parameters

Input File Name : "unary\_tree.prj"  
Ignore Synthesis Constraint File : NO

### ---- Target Parameters

Output File Name : "Unary\_Op\_Bin\_Tree"  
Output Format : NGC  
Target Device : xc6slx4-3-tqg144

### ---- Source Options

Top Module Name : Unary\_Op\_Bin\_Tree  
Automatic FSM Extraction : YES  
FSM Encoding Algorithm : Auto  
Safe Implementation : No  
FSM Style : LUT  
RAM Extraction : Yes  
RAM Style : Auto  
ROM Extraction : Yes  
Shift Register Extraction : YES  
ROM Style : Auto  
Resource Sharing : YES  
Asynchronous To Synchronous : NO  
Shift Register Minimum Size : 2

```

Use DSP Block           : Auto
Automatic Register Balancing : No
---- Target Options
LUT Combining           : Auto
Reduce Control Sets     : Auto
Add IO Buffers          : YES
Global Maximum Fanout   : 100000
Add Generic Clock Buffer(BUFG) : 16
Register Duplication    : YES
Optimize Instantiated Primitives : NO
Use Clock Enable        : Auto
Use Synchronous Set     : Auto
Use Synchronous Reset   : Auto
Pack IO Registers into IOBs : Auto
Equivalent register Removal : YES
---- General Options
Optimization Goal       : Speed
Optimization Effort     : 1
Power Reduction        : NO
Keep Hierarchy         : No
Netlist Hierarchy      : As_Optimized
RTL Output             : Yes
Global Optimization     : AllClockNets
Read Cores             : YES
Write Timing Constraints : NO
Cross Clock Analysis    : NO
Hierarchy Separator     : /
Bus Delimiter          : <>
Case Specifier         : Maintain
Slice Utilization Ratio : 100
BRAM Utilization Ratio  : 100
DSP48 Utilization Ratio : 100
Auto BRAM Packing       : NO
Slice Utilization Ratio Delta : 5
*           HDL Parsing           *
Parsing VHDL file "unary_op_xor_tree_lut6.vhd" into library work
Parsing entity <XorTreeStage>.
Parsing architecture <tree_of_xor_lut6> of entity <xortreestage>.
Parsing VHDL file "unary_op_tree.vhd" into library work
Parsing entity <Unary_Op_Bin_Tree>.
Parsing architecture <t> of entity <unary_op_bin_tree>.
*           HDL Elaboration        *
Elaborating entity <Unary_Op_Bin_Tree> (architecture <t>) with generics from library <work>.
Elaborating entity <XorTreeStage> (architecture <tree_of_xor_lut6>) with generics from library <work>.
Elaborating entity <XorTreeStage> (architecture <tree_of_xor_lut6>) with generics from library <work>.
Elaborating entity <XorTreeStage> (architecture <tree_of_xor_lut6>) with generics from library <work>.
Elaborating entity <XorTreeStage> (architecture <tree_of_xor_lut6>) with generics from library <work>.
Elaborating entity <XorTreeStage> (architecture <tree_of_xor_lut6>) with generics from library <work>.
Elaborating entity <XorTreeStage> (architecture <tree_of_xor_lut6>) with generics from library <work>.
Elaborating entity <XorTreeStage> (architecture <tree_of_xor_lut6>) with generics from library <work>.
Elaborating entity <XorTreeStage> (architecture <tree_of_xor_lut6>) with generics from library <work>.
Elaborating entity <XorTreeStage> (architecture <tree_of_xor_lut6>) with generics from library <work>.
*           HDL Synthesis          *
Synthesizing Unit <Unary_Op_Bin_Tree>.
  Related source file is "unary_op_tree.vhd".
  N = 4096
  Summary:
no macro.
Unit <Unary_Op_Bin_Tree> synthesized.

```

Synthesizing Unit <XorTreeStage\_1>.  
 Related source file is "\unary\_op\_xor\_tree\_lut6.vhd".  
 N = 4096  
 Summary:  
 no macro.  
 Unit <XorTreeStage\_1> synthesized.  
 Synthesizing Unit <XorTreeStage\_2>.  
 Related source file is "\unary\_op\_xor\_tree\_lut6.vhd".  
 N = 682  
 Summary:  
 no macro.  
 Unit <XorTreeStage\_2> synthesized.  
 Synthesizing Unit <XorTreeStage\_3>.  
 Related source file is "\unary\_op\_xor\_tree\_lut6.vhd".  
 N = 113  
 Summary:  
 no macro.  
 Unit <XorTreeStage\_3> synthesized.  
 Synthesizing Unit <XorTreeStage\_4>.  
 Related source file is "\unary\_op\_xor\_tree\_lut6.vhd".  
 N = 18  
 Summary:  
 no macro.  
 Unit <XorTreeStage\_4> synthesized.  
 Synthesizing Unit <XorTreeStage\_5>.  
 Related source file is "\unary\_op\_xor\_tree\_lut6.vhd".  
 N = 3  
 Summary:  
 no macro.  
 Unit <XorTreeStage\_5> synthesized.  
 Synthesizing Unit <XorTreeStage\_6>.  
 Related source file is "\unary\_op\_xor\_tree\_lut6.vhd".  
 N = 19  
 Summary:  
 no macro.  
 Unit <XorTreeStage\_6> synthesized.  
 Synthesizing Unit <XorTreeStage\_7>.  
 Related source file is "\unary\_op\_xor\_tree\_lut6.vhd".  
 N = 4  
 Summary:  
 no macro.  
 Unit <XorTreeStage\_7> synthesized.  
 Synthesizing Unit <XorTreeStage\_8>.  
 Related source file is "\unary\_op\_xor\_tree\_lut6.vhd".  
 N = 114  
 Summary:  
 no macro.  
 Unit <XorTreeStage\_8> synthesized.  
 Synthesizing Unit <XorTreeStage\_9>.  
 Related source file is "\unary\_op\_xor\_tree\_lut6.vhd".  
 N = 683  
 Summary:  
 no macro.  
 Unit <XorTreeStage\_9> synthesized.  
 HDL Synthesis Report  
 Found no macro  
 \*                    Advanced HDL Synthesis                    \*  
 Advanced HDL Synthesis Report  
 Found no macro

\* Low Level Synthesis \*

Optimizing unit <Unary\_Op\_Bin\_Tree> ...  
Mapping all equations...  
Building and optimizing final netlist ...  
Found area constraint ratio of 100 (+ 5) on block Unary\_Op\_Bin\_Tree, actual ratio is 94.  
Final Macro Processing ...  
Final Register Report  
Found no macro

\* Partition Report \*

Partition Implementation Status

-----  
No Partitions were found in this design.  
-----

\* Design Summary \*

Top Level Output File Name : Unary\_Op\_Bin\_Tree.ngc  
Primitive and Black Box Usage:

-----

# BELS	: 1555
# LUT3	: 1088
# LUT4	: 208
# LUT6	: 259
# IO Buffers	: 4097
# IBUF	: 4096
# OBUF	: 1

Device utilization summary:

-----  
Selected Device : 6slx4tqg144-3

Slice Logic Utilization:

Number of Slice LUTs:	1555	out of	2400	64%
Number used as Logic:	1555	out of	2400	64%

Slice Logic Distribution:

Number of LUT Flip Flop pairs used:	1555
Number with an unused Flip Flop:	1555 out of 1555 100%
Number with an unused LUT:	0 out of 1555 0%
Number of fully used LUT-FF pairs:	0 out of 1555 0%
Number of unique control sets:	0

IO Utilization:

Number of IOs:	4097
Number of bonded IOBs:	4097 out of 102 4016% (*)

Specific Feature Utilization:

WARNING:Xst:1336 - (\*) More than 100% of Device resources are used

-----  
Partition Resource Summary:

-----  
No Partitions were found in this design.  
-----

Timing Report

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.

FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT  
GENERATED AFTER PLACE-and-ROUTE.

Clock Information:

-----  
No clock signals found in this design

Asynchronous Control Signals Information:

-----  
No asynchronous control signals found in this design

Timing Summary:

-----  
Speed Grade: -3

Minimum period: No path found  
Minimum input arrival time before clock: No path found  
Maximum output required time after clock: No path found  
Maximum combinational path delay: 10.106ns

Timing Details:

-----

All values displayed in nanoseconds (ns)

Timing constraint: Default path analysis

Total number of paths / destination ports: 4096 / 1

-----  
Delay: 10.106ns (Levels of Logic = 7)

Source: I<0> (PAD)

Destination: O\_Xor (PAD)

Data Path: I<0> to O\_Xor

	Gate	Net			
Cell:in->out	fanout	Delay	Delay	Logical Name (Net Name)	
-----					
IBUF:I->O	1	1.222	0.808	I_0_IBUF (I_0_IBUF)	
LUT3:I0->O	1	0.339	0.944	U_Xor/Stages.Sixth1_Tree/Stages.Sixth1_Tree/Stages.Sixth1_Tree	
LUT6:I0->O	1	0.203	0.944	U_Xor/Stages.Sixth1_Tree/Stages.Sixth1_Tree/Stages.Sixth1_Tree	
LUT6:I0->O	1	0.203	0.944	U_Xor/Stages.Sixth1_Tree/Stages.Sixth1_Tree/Stages.XOR6_LUT	
LUT6:I0->O	1	0.203	0.944	U_Xor/Stages.Sixth1_Tree/Stages.XOR6_LUT (U_Xor/Stages.Sixth1_Tree)	
LUT6:I0->O	1	0.203	0.579	U_Xor/Stages.XOR6_LUT (O_Xor_OBUF)	
OBUF:I->O		2.571		O_Xor_OBUF (O_Xor)	

-----  
Total 10.106ns (4.944ns logic, 5.162ns route)  
(48.9% logic, 51.1% route)

Cross Clock Domains Report:

-----

Total REAL time to Xst completion: 31.00 secs

Total CPU time to Xst completion: 31.03 secs

-->

Total memory usage is 4569728 kilobytes

Number of errors : 0 ( 0 filtered)

Number of warnings : 1 ( 0 filtered)

Number of infos : 0 ( 0 filtered)

>fuse -incremental -o unary\_tree\_tb\_isim\_beh.exe -prj unary\_tree\_tb.prj -top Unary\_Op\_Bin\_Tree\_tb

ISim P.20131013 (signature 0x7708f090)

Number of CPUs detected in this system: 8

Turning on mult-threading, number of parallel sub-compilation jobs: 16

Determining compilation order of HDL files

Parsing VHDL file "slv\_image\_pkg.vhd" into library work

Parsing VHDL file "unary\_op\_xor\_tree\_lut6.vhd" into library work

Parsing VHDL file "unary\_op\_tree.vhd" into library work

Parsing VHDL file "unary\_op\_tree\_\_tb.vhd" into library work

Starting static elaboration

Completed static elaboration

Compiling package standard

Compiling package std\_logic\_1164

Compiling package numeric\_std

Compiling package textio

Compiling package std\_logic\_textio

Compiling package slv\_image\_pkg

Compiling package vcomponents

Compiling package vital\_timing

Compiling package vital\_primitives

Compiling package vpkg

Compiling architecture lut2\_v of entity LUT2 [LUT2("0110")(0,3)]



```

Compiling architecture tree_of_xor_lut6 of entity XorTreeStage [\XorTreeStage(2)]
Compiling architecture lut3_v of entity LUT3 [\LUT3("10010110")(0,7)]
Compiling architecture tree_of_xor_lut6 of entity XorTreeStage [\XorTreeStage(3)]
Compiling architecture lut6_v of entity LUT6 [\LUT6("0110100110010110100101100...)]
Compiling architecture tree_of_xor_lut6 of entity XorTreeStage [\XorTreeStage(16)]
Compiling architecture t of entity Unary_Op_Bin_Tree [\Unary_Op_Bin_Tree(16)]
Compiling architecture test of entity unary_op_bin_tree_tb
Time Resolution for simulation is 1ps.
Waiting for 2 sub-compilation(s) to finish...
Compiled 25 VHDL Units
Built simulation executable unary_tree_tb_isim_beh.exe
Fuse Memory Usage: 59944 KB
Fuse CPU Usage: 1280 ms
>if exist Unary_Op_Bin_Tree.csv del Unary_Op_Bin_Tree.csv
>if exist Unary_Op_Bin_Tree_.csv del Unary_Op_Bin_Tree_.csv
>unary_tree_tb_isim_beh.exe -tclbatch isim.tcl -wdb unary_tree_tb_isim_beh.wdb
ISim P.20131013 (signature 0x7708f090)
WARNING: A WEBPACK license was found.
WARNING: Please use Xilinx License Configuration Manager to check out a full ISim license.
WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for more information on t
This is a Lite version of ISim.
Time resolution is 1 ps
Simulator is doing circuit initialization process.
Finished circuit initialization process.
>rem ren Unary_Op_Bin_Tree.csv Unary_Op_Bin_Tree_.csv
>xst -ifn unary_vhdl93.xst
Release 14.7 - xst P.20131013 (nt64)
Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.
--> Parameter TMPDIR set to xst/projnav.tmp
Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.23 secs

--> Parameter xsthdpdir set to xst
Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.23 secs

```

-->

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*               Synthesis Options Summary               *	
---- Source Parameters	

```

Input File Name           : "/unary_vhdl93.prj"
Ignore Synthesis Constraint File : NO
---- Target Parameters
Output File Name          : "reduction_operators"
Output Format              : NGC
Target Device              : xc6slx4-3-tqg144
---- Source Options
Top Module Name           : reduction_operators
Automatic FSM Extraction   : YES
FSM Encoding Algorithm     : Auto
Safe Implementation       : No
FSM Style                  : LUT
RAM Extraction             : Yes
RAM Style                  : Auto
ROM Extraction             : Yes
Shift Register Extraction  : YES
ROM Style                  : Auto
Resource Sharing           : YES
Asynchronous To Synchronous : NO
Shift Register Minimum Size : 2
Use DSP Block              : Auto
Automatic Register Balancing : No
---- Target Options
LUT Combining             : Auto
Reduce Control Sets       : Auto
Add IO Buffers            : YES
Global Maximum Fanout     : 100000
Add Generic Clock Buffer(BUFG) : 16
Register Duplication      : YES
Optimize Instantiated Primitives : NO
Use Clock Enable          : Auto
Use Synchronous Set       : Auto
Use Synchronous Reset     : Auto
Pack IO Registers into IOBs : Auto
Equivalent register Removal : YES
---- General Options
Optimization Goal         : Speed
Optimization Effort       : 1
Power Reduction           : NO
Keep Hierarchy            : No
Netlist Hierarchy         : As_Optimized
RTL Output                : Yes
Global Optimization       : AllClockNets
Read Cores                : YES
Write Timing Constraints   : NO
Cross Clock Analysis      : NO
Hierarchy Separator       : /
Bus Delimiter             : <>
Case Specifier            : Maintain
Slice Utilization Ratio   : 100
BRAM Utilization Ratio    : 100
DSP48 Utilization Ratio   : 100
Auto BRAM Packing         : NO
Slice Utilization Ratio Delta : 5
*                           HDL Parsing                           *
Parsing VHDL file "unary_operators_vhdl_93.vhd" into library work
Parsing entity <reduction_operators>.
Parsing architecture <vhdl_93_comb> of entity <reduction_operators>.
Parsing architecture <vhdl_93_process> of entity <reduction_operators>.

```

```

*                      HDL Elaboration                      *
Elaborating entity <reduction_operators> (architecture <vhdl_93_process>) with generics from library <
*                      HDL Synthesis                        *
Synthesizing Unit <reduction_operators>.
  Related source file is "\unary_operators_vhdl_93.vhd".
  N = 64
  Summary:
inferred 128 Multiplexer(s).
Unit <reduction_operators> synthesized.
HDL Synthesis Report
Macro Statistics
# Multiplexers                : 128
  1-bit 2-to-1 multiplexer    : 128
# Xors                        : 1
  1-bit xor64                 : 1
*                      Advanced HDL Synthesis                *
Advanced HDL Synthesis Report
Macro Statistics
# Multiplexers                : 128
  1-bit 2-to-1 multiplexer    : 128
# Xors                        : 1
  1-bit xor64                 : 1
*                      Low Level Synthesis                   *
Optimizing unit <reduction_operators> ...
Mapping all equations...
Building and optimizing final netlist ...
Found area constraint ratio of 100 (+ 5) on block reduction_operators, actual ratio is 1.
Final Macro Processing ...
Final Register Report
Found no macro
*                      Partition Report                      *
Partition Implementation Status
-----
  No Partitions were found in this design.
-----
*                      Design Summary                        *
Top Level Output File Name    : reduction_operators.ngc
Primitive and Black Box Usage:
-----
# BELS                : 59
#  GND                : 1
#  LUT4                : 3
#  LUT6                : 32
#  MUXCY               : 22
#  VCC                : 1
# IO Buffers          : 67
#  IBUF               : 64
#  OBUF               : 3
Device utilization summary:
-----
Selected Device : 6slx4tqg144-3
Slice Logic Utilization:
Number of Slice LUTs:          35 out of 2400   1%
  Number used as Logic:        35 out of 2400   1%
Slice Logic Distribution:
Number of LUT Flip Flop pairs used: 35
  Number with an unused Flip Flop: 35 out of 35 100%
  Number with an unused LUT:      0 out of 35  0%
  Number of fully used LUT-FF pairs: 0 out of 35  0%

```

Number of unique control sets: 0  
IO Utilization:  
Number of IOs: 67  
Number of bonded IOBs: 67 out of 102 65%  
Specific Feature Utilization:

-----  
Partition Resource Summary:

-----  
No Partitions were found in this design.

-----  
Timing Report

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.

FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT  
GENERATED AFTER PLACE-and-ROUTE.

Clock Information:

-----  
No clock signals found in this design

Asynchronous Control Signals Information:

-----  
No asynchronous control signals found in this design

Timing Summary:

-----  
Speed Grade: -3

Minimum period: No path found

Minimum input arrival time before clock: No path found

Maximum output required time after clock: No path found

Maximum combinational path delay: 7.522ns

Timing Details:

-----  
All values displayed in nanoseconds (ns)

Timing constraint: Default path analysis

Total number of paths / destination ports: 192 / 3

-----  
Delay: 7.522ns (Levels of Logic = 5)

Source: A<22> (PAD)

Destination: reduced\_XOR (PAD)

Data Path: A<22> to reduced\_XOR

	Gate	Net		
Cell:in->out	fanout	Delay	Delay	Logical Name (Net Name)

IBUF:I->O	3	1.222	1.015	A_22_IBUF (A_22_IBUF)
LUT6:I0->O	1	0.203	0.944	Mxor_reduced_XOR_xo<0>3 (Mxor_reduced_XOR_xo<0>2)
LUT6:I0->O	1	0.203	0.580	Mxor_reduced_XOR_xo<0>14_SW0 (N01)
LUT6:I5->O	1	0.205	0.579	Mxor_reduced_XOR_xo<0>14 (reduced_XOR_OBUF)
OBUF:I->O		2.571		reduced_XOR_OBUF (reduced_XOR)

-----  
Total 7.522ns (4.404ns logic, 3.118ns route)  
(58.5% logic, 41.5% route)

Cross Clock Domains Report:

-----  
Total REAL time to Xst completion: 10.00 secs

Total CPU time to Xst completion: 10.29 secs

-->

Total memory usage is 4487516 kilobytes

Number of errors : 0 ( 0 filtered)

Number of warnings : 0 ( 0 filtered)

Number of infos : 0 ( 0 filtered)

>fuse -incremental -o unary\_vhdl93\_tb\_isim\_beh.exe -prj unary\_vhdl93\_tb.prj -top reduction\_operators\_

ISim P.20131013 (signature 0x7708f090)  
Number of CPUs detected in this system: 8  
Turning on mult-threading, number of parallel sub-compilation jobs: 16  
Determining compilation order of HDL files  
Parsing VHDL file "unary\_operators\_vhdl\_93.vhd" into library work  
Parsing VHDL file "unary\_operators\_vhdl93\_\_tb.vhd" into library work  
Starting static elaboration  
Completed static elaboration  
Compiling package standard  
Compiling package std\_logic\_1164  
Compiling package numeric\_std  
Compiling package textio  
Compiling package std\_logic\_textio  
Compiling architecture vhdl\_93\_process of entity reduction\_operators [reduction\_operators(3)]  
Compiling architecture test of entity reduction\_operators\_tb  
Time Resolution for simulation is 1ps.  
Waiting for 1 sub-compilation(s) to finish...  
Compiled 8 VHDL Units  
Built simulation executable unary\_vhdl93\_tb\_isim\_beh.exe  
Fuse Memory Usage: 36784 KB  
Fuse CPU Usage: 859 ms  
>if exist reduction\_operators.csv del reduction\_operators.csv  
>if exist reduction\_operators\_.csv del reduction\_operators\_.csv  
>unary\_vhdl93\_tb\_isim\_beh.exe -tclbatch isim.tcl -wdb unary\_vhdl93\_tb\_isim\_beh.wdb  
ISim P.20131013 (signature 0x7708f090)  
WARNING: A WEBPACK license was found.  
WARNING: Please use Xilinx License Configuration Manager to check out a full ISim license.  
WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for more information on t  
This is a Lite version of ISim.  
Time resolution is 1 ps  
Simulator is doing circuit initialization process.  
Finished circuit initialization process.  
>rem ren reduction\_operators.csv reduction\_operators\_.csv











.Tree/Stages.Sixth1\_Tree/Stage\_xor\_3.XOR3\_LUT (U\_Xor/Stages.Sixth1\_Tree/Stages.Sixth1\_Tree/Stages.XOR6\_LUT (U\_Xor/Stages.Sixth1\_Tree/Stages.Sixth1\_Tree/Stages.Sixth1\_out)  
LUT (U\_Xor/Stages.Sixth1\_Tree/Stages.Sixth1\_out)  
Sixth1\_out)

the differences between the Lite and the Full version.



work>.



.he differences between the Lite and the Full version.











ages.Sixth1\_Tree/Stages.Sixth1\_out)