

[illegible]

WARNING:HDLParasers:3607 - Unit work/muxnto1\_bus is now defined in a different file. It was defined  
WARNING:HDLParasers:3607 - Unit work/muxnto1\_bus/ideal is now defined in a different file. It was de

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in "IDEAL/muxnto1\_bus\_IDEAL.vhd", and is now defined in "IDEAL/muxnto1\_bus.vhd".  
defined in "IDEAL/muxnto1\_bus\_IDEAL.vhd", and is now defined in "IDEAL/muxnto1\_bus.vhd".

<pre> &gt; xst -dn reg_file.using IDEAL_mux_n to 1 bus.vst Release 14.7 - xst P 20131013 (m64) Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved. =&gt; Parameter THRESHOLD set to: 10000000000 Total REAL time to Xst completion: 0.00 secs Total CPU time to Xst completion: 0.23 secs -&gt; WARNING:Xst-3164 - Option "debug" found multiple times in the command line. Only the first occurrence is considered. </pre>	<pre> &gt; xst -dn reg_file.using mux_n to 1 bus.vst Release 14.7 - xst P 20131013 (m64) Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved. =&gt; Parameter THRESHOLD set to: 10000000000 Total REAL time to Xst completion: 1.00 secs Total CPU time to Xst completion: 0.22 secs -&gt; WARNING:Xst-3164 - Option "debug" found multiple times in the command line. Only the first occurrence is considered. </pre>
<pre> 1 HDL Compilation WARNING:HDLParameters2097: Unit work/muxout1_bus is now defined in a different file. It was defined in "muxout1_bus.vhd", and is now defined in "muxout1_bus IDEAL.vhd" Compiling vhdl file "muxout1.vhd" in Library work. Architecture ideal of Entity muxout1 is up to date. Compiling vhdl file "off.vhd" in Library work. Architecture ideal of Entity off is up to date. Compiling vhdl file "muxoff.vhd" in Library work. Architecture ideal of Entity muxoff is up to date. Compiling vhdl file "reg_file.functions.vhd" in Library work. Architecture reg_file.functions of Entity reg_file.functions is up to date. Compiling vhdl file "dmuxout1.vhd" in Library work. Architecture ideal of Entity dmuxout1 is up to date. Compiling vhdl file "muxout1_bus IDEAL.vhd" in Library work. Architecture ideal of Entity muxout1_bus is up to date. Compiling vhdl file "shift_reg.vhd" in Library work. Architecture ideal of Entity shift_reg is up to date. Compiling vhdl file "reg_file.vhd" in Library work. Architecture ndv of Entity reg_file is up to date. Total REAL time to Xst completion: 0.00 secs Total CPU time to Xst completion: 0.38 secs </pre>	<pre> 1 HDL Compilation Compiling vhdl file "muxout1.vhd" in Library work. Entity muxout1 to (Architecture &lt;+&gt;) compiled. Compiling vhdl file "off.vhd" in Library work. Entity off to compiled. Entity &lt;+P&gt; Architecture &lt;+&gt; compiled. Compiling vhdl file "muxoff.vhd" in Library work. Entity muxoff to compiled. Entity &lt;+muxoff&gt; compiled. Entity &lt;+muxoff&gt; (Architecture &lt;+&gt;) compiled. Compiling vhdl file "reg_file.functions.vhd" in Library work. Package &lt;reg_file.functions&gt; compiled. Package body &lt;reg_file.functions&gt; compiled. Compiling vhdl file "dmuxout1.vhd" in Library work. Entity &lt;dmuxout1&gt; compiled. Entity &lt;dmuxout1&gt; (Architecture &lt;+&gt;) compiled. Compiling vhdl file "muxout1_bus.vhd" in Library work. Entity muxout1_bus to compiled. Entity &lt;muxout1_bus&gt; (Architecture &lt;+&gt;) compiled. Compiling vhdl file "shift_reg.vhd" in Library work. Entity shift_reg to compiled. Entity &lt;shift_reg&gt; (Architecture &lt;+&gt;) compiled. Compiling vhdl file "reg_file.vhd" in Library work. Entity reg_file to compiled. Entity &lt;reg_file&gt; (Architecture &lt;NDV&gt;) compiled. Total REAL time to Xst completion: 2.00 secs Total CPU time to Xst completion: 1.51 secs </pre>
<pre> -&gt; Total memory usage is 4477124 kilobytes Number of errors : 0 ( 0 filtered) Number of warnings : 2 ( 0 filtered) Number of infos : 0 ( 0 filtered) Run P 20131013 (architecture 647708060) Number of CPUs detected in this system: 8 Turning on multi-threading, number of parallel sub-compilation jobs: 16 Determining compilation order of HDL files Parsing VHDL file "muxout1.vhd" into library work Parsing VHDL file "off.vhd" into library work Parsing VHDL file "reg_file.functions.vhd" into library work Parsing VHDL file "muxoff.vhd" into library work Parsing VHDL file "shift_reg.vhd" into library work Parsing VHDL file "muxout1_bus IDEAL.vhd" into library work Parsing VHDL file "dmuxout1.vhd" into library work Parsing VHDL file "reg_file.vhd" into library work Starting static elaboration Completed static elaboration Compiling package standard Compiling package std_logic_1164 Compiling package reg_file.functions Compiling package math_real Compiling package numeric_std Compiling architecture ideal of entity dmuxout1 fdmuxout1(120) Compiling architecture ideal of entity muxout1 fmuxout1(140) Compiling architecture ideal of entity muxout1_bus fmuxout1_bus(2 81) Compiling architecture ideal of entity off foff_default Compiling architecture ideal of entity muxoff fmuxoff(21) Compiling architecture ideal of entity shift_reg fshift_reg(81) Compiling architecture ndv of entity reg_file Time Resolution for simulation is 1ps Waiting for 1 sub-compilation(s) to finish... Completed 14 VHDL Units Built simulation executable reg_file.using IDEAL_mux_n to 1 bus isim behavio Fuses Memory Usage: 37366 KB </pre>	<pre> Total memory usage is 4477112 kilobytes Number of errors : 0 ( 0 filtered) Number of warnings : 1 ( 0 filtered) Number of infos : 0 ( 0 filtered) -&gt;Use incremental compilation. Run P 20131013 (architecture 647708060) Number of CPUs detected in this system: 8 Turning on multi-threading, number of parallel sub-compilation jobs: 16 Determining compilation order of HDL files Parsing VHDL file "muxout1.vhd" into library work Parsing VHDL file "off.vhd" into library work Parsing VHDL file "reg_file.functions.vhd" into library work Parsing VHDL file "muxoff.vhd" into library work Parsing VHDL file "shift_reg.vhd" into library work Parsing VHDL file "muxout1_bus.vhd" into library work Parsing VHDL file "dmuxout1.vhd" into library work Parsing VHDL file "reg_file.vhd" into library work Starting static elaboration Completed static elaboration Compiling package standard Compiling package std_logic_1164 Compiling package reg_file.functions Compiling package math_real Compiling package numeric_std Compiling architecture of entity dmuxout1 fdmuxout1(120) Compiling architecture of entity muxout1 fmuxout1(120) Compiling architecture of entity muxout1_bus fmuxout1_bus(2 81) Compiling architecture of entity off foff_default Compiling architecture of entity muxoff fmuxoff(21) </pre>

<pre> &gt; xst -dlm rep file usinfo IDEAL_mux_n.to.1.bus.vst Release 14.7 - xst P 20131013 (m64) Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved. =&gt; Parameter THPDR set to: jasthompson.mps Total REAL time to Xst completion: 0.00 secs Total CPU time to Xst completion: 0.22 secs  -&gt; WARNING:Xst-3164 - Option "debug" found multiple times in the command line. Only the first occurrence is considered. * HDL Compilation Compiling vhdl file "muento1.vhd" in Library work Entity &lt;muento1&gt; (Architecture &lt;ideast&gt;) compiled. Compiling vhdl file "off.vhd" in Library work Entity &lt;off&gt; compiled. Entity &lt;off&gt; (Architecture &lt;ideast&gt;) compiled. Compiling vhdl file "muxoff.vhd" in Library work Entity &lt;muxoff&gt; compiled. Entity &lt;muxoff&gt; (Architecture &lt;ideast&gt;) compiled. Compiling vhdl file "req file functions.vhd" in Library work Package &lt;req file functions&gt; compiled. Package body &lt;req file functions&gt; compiled. Compiling vhdl file "idmuento1.vhd" in Library work Entity &lt;idmuento1&gt; compiled. Entity &lt;idmuento1&gt; (Architecture &lt;ideast&gt;) compiled. Compiling vhdl file "muento1_bus IDEAL.vhd" in Library work Entity &lt;muento1_bus&gt; compiled. Entity &lt;muento1_bus&gt; (Architecture &lt;ideast&gt;) compiled. Compiling vhdl file "tshift_req.vhd" in Library work Entity &lt;tshift_req&gt; compiled. Entity &lt;tshift_req&gt; (Architecture &lt;ideast&gt;) compiled. Entity &lt;shift_req&gt; compiled. Entity &lt;shift_req&gt; (Architecture &lt;ideast&gt;) compiled. Compiling vhdl file "req file.vhd" in Library work Entity &lt;req file&gt; compiled. Entity &lt;req file&gt; (Architecture &lt;NDV&gt;) compiled. Total REAL time to Xst completion: 0.00 secs Total CPU time to Xst completion: 0.38 secs  -&gt; Total memory usage is 4477108 kilobytes Number of errors - 0 ( 0 filtered) Number of warnings - 1 ( 0 filtered) Number of infos - 0 ( 0 filtered) &gt;Wave incremental - rep file usinfo IDEAL_mux_n.to.1.bus.isim both.exe -rt rep file usinfo IDEAL_mux_n.to.1.bus.vst -log rep file Run P-40120112 (signature 6a770876b0) Number of CPUs detected in this system: 8 Turning on multi-threading, number of parallel sub-compilation jobs: 16 Determining compilation order of HDL files Parsing VHDL file "muento1.vhd" into library work Parsing VHDL file "off.vhd" into library work Parsing VHDL file "req file functions.vhd" into library work Parsing VHDL file "muxoff.vhd" into library work Parsing VHDL file "tshift_req.vhd" into library work Parsing VHDL file "idmuento1.vhd" into library work Parsing VHDL file "muento1_bus IDEAL.vhd" into library work Parsing VHDL file "muento1.vhd" into library work Parsing VHDL file "req file.vhd" into library work Starting static elaboration Completed static elaboration Compiling package standard Compiling package std logic 1164 Compiling package req file functions Compiling package math real Compiling package numeric std Compiling architecture ideal of entity dmuento1 fdmuento123) Compiling architecture ideal of entity muento1 fmiento1123) Compiling architecture ideal of entity muento1_bus fmiento1_bus2 83) Compiling architecture ideal of entity off foff default) Compiling architecture ideal of entity muxoff fmuxoff23) </pre>	<pre> &gt; xst -dlm rep file usinfo_mux_n.to.1.bus.vst Release 14.7 - xst P 20131013 (m64) Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved. =&gt; Parameter THPDR set to: jasthompson.mps Total REAL time to Xst completion: 1.00 secs Total CPU time to Xst completion: 0.22 secs  -&gt; WARNING:Xst-3164 - Option "debug" found multiple times in the command line. Only the first occurrence is considered. * HDL Compilation Compiling vhdl file "muento1.vhd" in Library work Entity &lt;muento1&gt; compiled. Entity &lt;muento1&gt; (Architecture &lt;+&gt;) compiled. Compiling vhdl file "off.vhd" in Library work Entity &lt;off&gt; compiled. Entity &lt;off&gt; (Architecture &lt;+&gt;) compiled. Compiling vhdl file "muxoff.vhd" in Library work Entity &lt;muxoff&gt; compiled. Entity &lt;muxoff&gt; (Architecture &lt;+&gt;) compiled. Compiling vhdl file "req file functions.vhd" in Library work Package &lt;req file functions&gt; compiled. Package body &lt;req file functions&gt; compiled. Compiling vhdl file "idmuento1.vhd" in Library work Entity &lt;idmuento1&gt; compiled. Entity &lt;idmuento1&gt; (Architecture &lt;+&gt;) compiled. Compiling vhdl file "muento1_bus.vhd" in Library work Entity &lt;muento1_bus&gt; compiled. Entity &lt;muento1_bus&gt; (Architecture &lt;+&gt;) compiled. Compiling vhdl file "tshift_req.vhd" in Library work Entity &lt;tshift_req&gt; compiled. Entity &lt;tshift_req&gt; (Architecture &lt;+&gt;) compiled. Entity &lt;shift_req&gt; compiled. Entity &lt;shift_req&gt; (Architecture &lt;+&gt;) compiled. Compiling vhdl file "req file.vhd" in Library work Entity &lt;req file&gt; compiled. Entity &lt;req file&gt; (Architecture &lt;NDV&gt;) compiled. Total REAL time to Xst completion: 2.00 secs Total CPU time to Xst completion: 1.51 secs  -&gt; Total memory usage is 4477112 kilobytes Number of errors - 0 ( 0 filtered) Number of warnings - 1 ( 0 filtered) Number of infos - 0 ( 0 filtered) &gt;Wave incremental - rep file usinfo_mux_n.to.1.bus.isim both.exe -rt rep file usinfo_mux_n.to.1.bus.vst -log rep file Run P-40120112 (signature 6a770876b0) Number of CPUs detected in this system: 8 Turning on multi-threading, number of parallel sub-compilation jobs: 16 Determining compilation order of HDL files Parsing VHDL file "muento1.vhd" into library work Parsing VHDL file "off.vhd" into library work Parsing VHDL file "req file functions.vhd" into library work Parsing VHDL file "muxoff.vhd" into library work Parsing VHDL file "tshift_req.vhd" into library work Parsing VHDL file "idmuento1.vhd" into library work Parsing VHDL file "muento1_bus.vhd" into library work Parsing VHDL file "muento1.vhd" into library work Parsing VHDL file "req file.vhd" into library work Starting static elaboration Completed static elaboration Compiling package standard Compiling package std logic 1164 Compiling package req file functions Compiling package math real Compiling package numeric std Compiling architecture of entity dmuento1 fdmuento123) Compiling architecture of entity muento1 fmiento1123) Compiling architecture of entity muento1_bus fmiento1_bus2 83) Compiling architecture of entity off foff default) Compiling architecture of entity muxoff fmuxoff23) </pre>
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<pre> &gt; xst -dlm rep file usinfo IDEAL_mux_n to 1 bus.vst Release 14.7 - xst P 20131013 (m64) Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved. =&gt; Parameter THRESHOLD set to 1astlongest.mio Total REAL time to Xst completion: 1.00 secs Total CPU time to Xst completion: 0.24 secs  -&gt; WARNING:Xst-3164 - Option "debug" found multiple times in the command line. Only the first occurrence is considered. * HDL Compilation Compiling vhdl file "muento1.vhd" in Library work Entity &lt;muento1&gt; (Architecture &lt;ideast&gt;) compiled. Compiling vhdl file "off.vhd" in Library work Entity &lt;off&gt; compiled. Entity &lt;off&gt; (Architecture &lt;ideast&gt;) compiled. Compiling vhdl file "muxoff.vhd" in Library work Entity &lt;muxoff&gt; compiled. Entity &lt;muxoff&gt; (Architecture &lt;ideast&gt;) compiled. Compiling vhdl file "req file functions.vhd" in Library work Package &lt;req file functions&gt; compiled. Package body &lt;req file functions&gt; compiled. Compiling vhdl file "idmuento1.vhd" in Library work Entity &lt;idmuento1&gt; compiled. Entity &lt;idmuento1&gt; (Architecture &lt;ideast&gt;) compiled. Compiling vhdl file "muento1 bus IDEAL.vhd" in Library work Entity &lt;muento1 bus&gt; compiled. Entity &lt;muento1 bus&gt; (Architecture &lt;ideast&gt;) compiled. Compiling vhdl file "shift_req.vhd" in Library work Entity &lt;shift_req&gt; compiled. Entity &lt;shift_req&gt; (Architecture &lt;ideast&gt;) compiled. Compiling vhdl file "req file.vhd" in Library work Entity &lt;req file&gt; compiled. Entity &lt;req file&gt; (Architecture &lt;NDV&gt;) compiled. Total REAL time to Xst completion: 1.00 secs Total CPU time to Xst completion: 0.24 secs  -&gt; Total memory usage is 4477144 kilobytes Number of errors : 0 ( 0 filtered) Number of warnings : 11 ( 0 filtered) Number of infos : 0 ( 0 filtered) &gt;Wave incremental -o rep file usinfo IDEAL_mux_n to 1 bus.isim both.exe -rtl rep file usinfo IDEAL_mux_n to 1 bus.ort -top rep file Run P-40121012 (signature 6a770876b0) Number of CPUs detected in this system: 8 Turning on multi-threading, number of parallel sub-compilation jobs: 16 Determining compilation order of HDL files Parsing VHDL file "muento1.vhd" into library work Parsing VHDL file "off.vhd" into library work Parsing VHDL file "req file functions.vhd" into library work Parsing VHDL file "muxoff.vhd" into library work Parsing VHDL file "shift_req.vhd" into library work Parsing VHDL file "idmuento1.vhd" into library work Parsing VHDL file "muento1 bus IDEAL.vhd" into library work Parsing VHDL file "req file.vhd" into library work Starting static elaboration Completed static elaboration Compiling package standard Compiling package std logic 1164 Compiling package req file functions Compiling package math real Compiling package numeric std Compiling architecture ideal of entity dmuento1 fdmuento123) Compiling architecture ideal of entity muento1 fmiento1123) Compiling architecture ideal of entity muento1 bus fmiento1 bus2 81) Compiling architecture ideal of entity off foff default) Compiling architecture ideal of entity muxoff fmuxoff23) </pre>	<pre> &gt; xst -dlm rep file usinfo_mux_n to 1 bus.vst Release 14.7 - xst P 20131013 (m64) Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved. =&gt; Parameter THRESHOLD set to 1astlongest.mio Total REAL time to Xst completion: 1.00 secs Total CPU time to Xst completion: 0.22 secs  -&gt; WARNING:Xst-3164 - Option "debug" found multiple times in the command line. Only the first occurrence is considered. * HDL Compilation Compiling vhdl file "muento1.vhd" in Library work Entity &lt;muento1&gt; compiled. Entity &lt;muento1&gt; (Architecture &lt;+&gt;) compiled. Compiling vhdl file "off.vhd" in Library work Entity &lt;off&gt; compiled. Entity &lt;off&gt; (Architecture &lt;+&gt;) compiled. Compiling vhdl file "muxoff.vhd" in Library work Entity &lt;muxoff&gt; compiled. Entity &lt;muxoff&gt; (Architecture &lt;+&gt;) compiled. Compiling vhdl file "req file functions.vhd" in Library work Package &lt;req file functions&gt; compiled. Package body &lt;req file functions&gt; compiled. Compiling vhdl file "idmuento1.vhd" in Library work Entity &lt;idmuento1&gt; compiled. Entity &lt;idmuento1&gt; (Architecture &lt;+&gt;) compiled. Compiling vhdl file "muento1 bus .vhd" in Library work Entity &lt;muento1 bus&gt; compiled. Entity &lt;muento1 bus&gt; (Architecture &lt;+&gt;) compiled. Compiling vhdl file "shift_req.vhd" in Library work Entity &lt;shift_req&gt; compiled. Entity &lt;shift_req&gt; (Architecture &lt;+&gt;) compiled. Compiling vhdl file "req file.vhd" in Library work Entity &lt;req file&gt; compiled. Entity &lt;req file&gt; (Architecture &lt;NDV&gt;) compiled. Total REAL time to Xst completion: 2.00 secs Total CPU time to Xst completion: 1.51 secs  -&gt; Total memory usage is 4477112 kilobytes Number of errors : 0 ( 0 filtered) Number of warnings : 11 ( 0 filtered) Number of infos : 0 ( 0 filtered) &gt;Wave incremental -o rep file usinfo_mux_n to 1 bus.isim both.exe -rtl rep file usinfo_mux_n to 1 bus.ort -top rep file Run P-40121012 (signature 6a770876b0) Number of CPUs detected in this system: 8 Turning on multi-threading, number of parallel sub-compilation jobs: 16 Determining compilation order of HDL files Parsing VHDL file "muento1.vhd" into library work Parsing VHDL file "off.vhd" into library work Parsing VHDL file "req file functions.vhd" into library work Parsing VHDL file "muxoff.vhd" into library work Parsing VHDL file "shift_req.vhd" into library work Parsing VHDL file "idmuento1.vhd" into library work Parsing VHDL file "muento1 bus .vhd" into library work Parsing VHDL file "req file.vhd" into library work Starting static elaboration Completed static elaboration Compiling package standard Compiling package std logic 1164 Compiling package req file functions Compiling package math real Compiling package numeric std Compiling architecture of entity dmuento1 fdmuento123) Compiling architecture of entity muento1 fmiento1123) Compiling architecture of entity muento1 bus fmiento1 bus2 81) Compiling architecture of entity off foff default) Compiling architecture of entity muxoff fmuxoff23) </pre>
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<pre> &gt;set -fni rep file usinfo IDEAL_mux.n to 1 bus.vst Release 14.7 - set P 20131013 (m64) Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved. =&gt; Parameter THPDR set to: testonnew.bm Total REAL time to Xst completion: 0.90 secs Total CPU time to Xst completion: 0.24 secs --&gt; WARNING:Xst-3164 - Option "debug" found multiple times in the command line. Only the first occurrence is considered. * HDL Compilation Compiling vhdl file "muento1.vhd" in Library work Entity &lt;muento1&gt; (Architecture &lt;ideast&gt;) compiled. Compiling vhdl file "off.vhd" in Library work Entity &lt;off&gt; compiled. Entity &lt;off&gt; (Architecture &lt;ideast&gt;) compiled. Compiling vhdl file "muxoff.vhd" in Library work Entity &lt;muxoff&gt; compiled. Entity &lt;muxoff&gt; (Architecture &lt;ideast&gt;) compiled. Compiling vhdl file "req file functions.vhd" in Library work Package &lt;req file functions&gt; compiled. Package body &lt;req file functions&gt; compiled. Compiling vhdl file "idmuento1.vhd" in Library work Entity &lt;idmuento1&gt; compiled. Entity &lt;idmuento1&gt; (Architecture &lt;ideast&gt;) compiled. Compiling vhdl file "muento1 bus IDEAL.vhd" in Library work Entity &lt;muento1 bus&gt; compiled. Entity &lt;muento1 bus&gt; (Architecture &lt;ideast&gt;) compiled. Compiling vhdl file "tshift_req.vhd" in Library work Entity &lt;tshift_req&gt; compiled. Entity &lt;tshift_req&gt; (Architecture &lt;ideast&gt;) compiled. Compiling vhdl file "req file.vhd" in Library work Entity &lt;req file&gt; compiled. Entity &lt;req file&gt; (Architecture &lt;NDV&gt;) compiled. Total REAL time to Xst completion: 1.00 secs Total CPU time to Xst completion: 1.12 secs --&gt; Total memory usage is 4477152 kilobytes Number of errors - 0 ( 0 filtered) Number of warnings - 1 ( 0 filtered) Number of infos - 0 ( 0 filtered) &gt;Use incremental -o rep file usinfo IDEAL_mux.n to 1 bus.isim both.exe -o rep file usinfo IDEAL_mux.n to 1 bus.vst -o rep file Run P-4012013 (signature 6a770876b) Number of CPUs detected in this system: 4 Turning on multi-threading, number of parallel sub-compilation jobs: 16 Determining compilation order of HDL files Parsing VHDL file "muento1.vhd" into library work Parsing VHDL file "off.vhd" into library work Parsing VHDL file "req file functions.vhd" into library work Parsing VHDL file "muxoff.vhd" into library work Parsing VHDL file "tshift_req.vhd" into library work Parsing VHDL file "idmuento1.vhd" into library work Parsing VHDL file "muento1 bus IDEAL.vhd" into library work Parsing VHDL file "muento1.vhd" into library work Starting static elaboration Completed static elaboration Compiling package standard Compiling package std logic 1164 Compiling package req file functions Compiling package math real Compiling package numeric std Compiling architecture ideal of entity dmuento1 fdmuento123) Compiling architecture ideal of entity muento1 fmiento1123) Compiling architecture ideal of entity muento1 bus fmiento1 bus2 81) Compiling architecture ideal of entity off foff default) Compiling architecture ideal of entity muxoff fmuxoff23) </pre>	<pre> &gt;set -fni rep file usinfo_mux.n to 1 bus.vst Release 14.7 - set P 20131013 (m64) Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved. =&gt; Parameter THPDR set to: testonnew.bm Total REAL time to Xst completion: 1.00 secs Total CPU time to Xst completion: 0.22 secs --&gt; WARNING:Xst-3164 - Option "debug" found multiple times in the command line. Only the first occurrence is considered. * HDL Compilation Compiling vhdl file "muento1.vhd" in Library work Entity &lt;muento1&gt; compiled. Entity &lt;muento1&gt; (Architecture &lt;+&gt;) compiled. Compiling vhdl file "off.vhd" in Library work Entity &lt;off&gt; compiled. Entity &lt;off&gt; (Architecture &lt;+&gt;) compiled. Compiling vhdl file "muxoff.vhd" in Library work Entity &lt;muxoff&gt; compiled. Entity &lt;muxoff&gt; (Architecture &lt;+&gt;) compiled. Compiling vhdl file "req file functions.vhd" in Library work Package &lt;req file functions&gt; compiled. Package body &lt;req file functions&gt; compiled. Compiling vhdl file "idmuento1.vhd" in Library work Entity &lt;idmuento1&gt; compiled. Entity &lt;idmuento1&gt; (Architecture &lt;+&gt;) compiled. Compiling vhdl file "muento1 bus.vhd" in Library work Entity &lt;muento1 bus&gt; compiled. Entity &lt;muento1 bus&gt; (Architecture &lt;+&gt;) compiled. Compiling vhdl file "tshift_req.vhd" in Library work Entity &lt;tshift_req&gt; compiled. Entity &lt;tshift_req&gt; (Architecture &lt;+&gt;) compiled. Compiling vhdl file "req file.vhd" in Library work Entity &lt;req file&gt; compiled. Entity &lt;req file&gt; (Architecture &lt;NDV&gt;) compiled. Total REAL time to Xst completion: 2.00 secs Total CPU time to Xst completion: 1.51 secs --&gt; Total memory usage is 4477112 kilobytes Number of errors - 0 ( 0 filtered) Number of warnings - 1 ( 0 filtered) Number of infos - 0 ( 0 filtered) &gt;Use incremental -o rep file usinfo_mux.n to 1 bus.isim both.exe -o rep file usinfo_mux.n to 1 bus.vst -o rep file Run P-4012013 (signature 6a770876b) Number of CPUs detected in this system: 4 Turning on multi-threading, number of parallel sub-compilation jobs: 16 Determining compilation order of HDL files Parsing VHDL file "muento1.vhd" into library work Parsing VHDL file "off.vhd" into library work Parsing VHDL file "req file functions.vhd" into library work Parsing VHDL file "muxoff.vhd" into library work Parsing VHDL file "tshift_req.vhd" into library work Parsing VHDL file "idmuento1.vhd" into library work Parsing VHDL file "muento1 bus.vhd" into library work Parsing VHDL file "muento1.vhd" into library work Starting static elaboration Completed static elaboration Compiling package standard Compiling package std logic 1164 Compiling package req file functions Compiling package math real Compiling package numeric std Compiling architecture of entity dmuento1 fdmuento123) Compiling architecture of entity muento1 fmiento1123) Compiling architecture of entity muento1 bus fmiento1 bus2 81) Compiling architecture of entity off foff default) Compiling architecture of entity muxoff fmuxoff23) </pre>
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<pre> -&gt;set -fni rep file usinfo IDEAL_mux.n to 1 bus.vst Release 14.7 - set P 20131013 (m64) Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved. -&gt; Parameter THPDR set to: testonnew.mio Total REAL time to Xst completion: 0.00 secs Total CPU time to Xst completion: 0.22 secs -&gt; WARNING:Xst-3164 - Option "debug" found multiple times in the command line. Only the first occurrence is considered. " HDL Compilation Compiling vhdl file "muento1.vhd" in Library work. Entity &lt;muento1&gt; compiled. Entity &lt;muento1&gt; (Architecture &lt;ideal&gt;) compiled. Compiling vhdl file "off.vhd" in Library work. Entity &lt;off&gt; compiled. Entity &lt;off&gt; (Architecture &lt;ideal&gt;) compiled. Compiling vhdl file "muxoff.vhd" in Library work. Entity &lt;muxoff&gt; compiled. Entity &lt;muxoff&gt; (Architecture &lt;ideal&gt;) compiled. Compiling vhdl file "req file functions.vhd" in Library work. Package &lt;req file functions&gt; compiled. Package body &lt;req file functions&gt; compiled. Compiling vhdl file "muento1_bus IDEAL.vhd" in Library work. Entity &lt;muento1&gt; bus&gt; compiled. Entity &lt;muento1&gt; bus&gt; (Architecture &lt;ideal&gt;) compiled. Compiling vhdl file "muento1.vhd" in Library work. Entity &lt;muento1&gt; compiled. Compiling vhdl file "shift_req.vhd" in Library work. Entity &lt;shift_req&gt; compiled. Entity &lt;shift_req&gt; (Architecture &lt;ideal&gt;) compiled. Compiling vhdl file "req file.vhd" in Library work. Entity &lt;req file&gt; compiled. Entity &lt;req file&gt; (Architecture &lt;NDV&gt;) compiled. Total REAL time to Xst completion: 3.00 secs Total CPU time to Xst completion: 2.62 secs -&gt; Total memory usage is 4477088 kilobytes Number of errors - 0 ( 0 filtered) Number of warnings - 1 ( 0 filtered) Number of infos - 0 ( 0 filtered) -&gt;Use incremental compilation IDEAL_mux.n to 1 bus.isim both.exe.vst rep file usinfo IDEAL_mux.n to 1 bus.vst bus rep file Run P 40131013 (signature 6a770860) Number of CPUs detected in this system: 4 Turning on multi-threading, number of parallel sub-compilation jobs: 16 Determining compilation order of HDL files Parsing VHDL file "muento1.vhd" into library work. Parsing VHDL file "off.vhd" into library work. Parsing VHDL file "req file functions.vhd" into library work. Parsing VHDL file "muxoff.vhd" into library work. Parsing VHDL file "shift_req.vhd" into library work. Parsing VHDL file "muento1_bus IDEAL.vhd" into library work. Parsing VHDL file "muento1.vhd" into library work. Parsing VHDL file "req file.vhd" into library work. Starting static elaboration. Completed static elaboration. Compiling package standard. Compiling package std logic 1164. Compiling package req file functions. Compiling package math real. Compiling package numeric std. Compiling architecture ideal of entity muento1 (muento1/2) Compiling architecture ideal of entity muento1 bus (muento1_bus/2) Compiling architecture ideal of entity muento1 (muento1/3) Compiling architecture ideal of entity off (off default) Compiling architecture ideal of entity muxoff (muxoff/2) </pre>	<pre> -&gt;set -fni rep file usinfo_mux.n to 1 bus.vst Release 14.7 - set P 20131013 (m64) Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved. -&gt; Parameter THPDR set to: testonnew.mio Total REAL time to Xst completion: 1.00 secs Total CPU time to Xst completion: 0.22 secs -&gt; WARNING:Xst-3164 - Option "debug" found multiple times in the command line. Only the first occurrence is considered. " HDL Compilation Compiling vhdl file "muento1.vhd" in Library work. Entity &lt;muento1&gt; compiled. Entity &lt;muento1&gt; (Architecture &lt;+&gt;) compiled. Compiling vhdl file "off.vhd" in Library work. Entity &lt;off&gt; compiled. Entity &lt;off&gt; (Architecture &lt;+&gt;) compiled. Compiling vhdl file "muxoff.vhd" in Library work. Entity &lt;muxoff&gt; compiled. Entity &lt;muxoff&gt; (Architecture &lt;+&gt;) compiled. Compiling vhdl file "req file functions.vhd" in Library work. Package &lt;req file functions&gt; compiled. Package body &lt;req file functions&gt; compiled. Compiling vhdl file "muento1.vhd" in Library work. Entity &lt;muento1&gt; compiled. Entity &lt;muento1&gt; bus&gt; compiled. Entity &lt;muento1&gt; bus&gt; (Architecture &lt;+&gt;) compiled. Compiling vhdl file "muento1_bus.vhd" in Library work. Entity &lt;muento1&gt; bus&gt; compiled. Entity &lt;muento1&gt; bus&gt; (Architecture &lt;+&gt;) compiled. Compiling vhdl file "shift_req.vhd" in Library work. Entity &lt;shift_req&gt; compiled. Entity &lt;shift_req&gt; (Architecture &lt;+&gt;) compiled. Compiling vhdl file "req file.vhd" in Library work. Entity &lt;req file&gt; compiled. Entity &lt;req file&gt; (Architecture &lt;NDV&gt;) compiled. Total REAL time to Xst completion: 2.00 secs Total CPU time to Xst completion: 1.51 secs -&gt; Total memory usage is 4477112 kilobytes Number of errors - 0 ( 0 filtered) Number of warnings - 1 ( 0 filtered) Number of infos - 0 ( 0 filtered) -&gt;Use incremental compilation usinfo_mux.n to 1 bus.isim both.exe.vst rep file usinfo_mux.n to 1 bus.vst bus rep file Run P 40131013 (signature 6a770860) Number of CPUs detected in this system: 4 Turning on multi-threading, number of parallel sub-compilation jobs: 16 Determining compilation order of HDL files Parsing VHDL file "muento1.vhd" into library work. Parsing VHDL file "off.vhd" into library work. Parsing VHDL file "req file functions.vhd" into library work. Parsing VHDL file "muxoff.vhd" into library work. Parsing VHDL file "shift_req.vhd" into library work. Parsing VHDL file "muento1_bus.vhd" into library work. Parsing VHDL file "muento1.vhd" into library work. Parsing VHDL file "req file.vhd" into library work. Starting static elaboration. Completed static elaboration. Compiling package standard. Compiling package std logic 1164. Compiling package req file functions. Compiling package math real. Compiling package numeric std. Compiling architecture of entity muento1 (muento1/2) Compiling architecture of entity muento1 (muento1/3) Compiling architecture of entity muento1 bus (muento1_bus/2) Compiling architecture of entity off (off default) Compiling architecture of entity muxoff (muxoff/2) </pre>
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<pre> &gt; xst -dlm rep file usinfo IDEAL_mux_n to 1 bus.vst Release 14.7 - xst P 20131013 (m64) Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved. =&gt; Parameter THRESHOLD set to 1astoprow.mio Total REAL time to Xst completion: 1.00 secs Total CPU time to Xst completion: 0.22 secs  -&gt; WARNING:Xst-3164 - Option "debug" found multiple times in the command line. Only the first occurrence is considered. * HDL Compilation Compiling vhdl file "muento1.vhd" in Library work Entity &lt;muento1&gt; (Architecture &lt;ideal&gt;) compiled. Compiling vhdl file "off.vhd" in Library work Entity &lt;off&gt; compiled. Entity &lt;off&gt; (Architecture &lt;ideal&gt;) compiled. Compiling vhdl file "muxoff.vhd" in Library work Entity &lt;muxoff&gt; compiled. Entity &lt;muxoff&gt; (Architecture &lt;ideal&gt;) compiled. Compiling vhdl file "req file functions.vhd" in Library work Package &lt;req file functions&gt; compiled. Package body &lt;req file functions&gt; compiled. Compiling vhdl file "dmuento1.vhd" in Library work Entity &lt;dmuento1&gt; compiled. Entity &lt;dmuento1&gt; (Architecture &lt;ideal&gt;) compiled. Compiling vhdl file "muento1 bus IDEAL.vhd" in Library work Entity &lt;muento1 bus&gt; compiled. Entity &lt;muento1 bus&gt; (Architecture &lt;ideal&gt;) compiled. Compiling vhdl file "shift_req.vhd" in Library work Entity &lt;shift_req&gt; compiled. Entity &lt;shift_req&gt; (Architecture &lt;ideal&gt;) compiled. Compiling vhdl file "req file.vhd" in Library work Entity &lt;req file&gt; compiled. Entity &lt;req file&gt; (Architecture &lt;NDV&gt;) compiled. Total REAL time to Xst completion: 2.00 secs Total CPU time to Xst completion: 2.00 secs  -&gt; Total memory usage is 4477180 kilobytes Number of errors : 0 ( 0 filtered) Number of warnings : 1 ( 0 filtered) Number of infos : 0 ( 0 filtered) &gt;Use incremental -o rep file usinfo IDEAL_mux_n to 1 bus.isim both.exe -o rep file usinfo IDEAL_mux_n to 1 bus.art -o rep file Run P-40121012 (signature 6a770876b0) Number of CPUs detected in this system: 4 Turning on multi-threading, number of parallel sub-compilation jobs: 16 Determining compilation order of HDL files Parsing VHDL file "muento1.vhd" into library work Parsing VHDL file "off.vhd" into library work Parsing VHDL file "req file functions.vhd" into library work Parsing VHDL file "muxoff.vhd" into library work Parsing VHDL file "shift_req.vhd" into library work Parsing VHDL file "dmuento1.vhd" into library work Parsing VHDL file "muento1 bus IDEAL.vhd" into library work Parsing VHDL file "req file.vhd" into library work Starting static elaboration Completed static elaboration Compiling package standard Compiling package std_logic_1164 Compiling package req file functions Compiling package math_real Compiling package numeric_std Compiling architecture ideal of entity dmuento1 fdmuento123) Compiling architecture ideal of entity muento1 fmuento123) Compiling architecture ideal of entity muento1 bus fmuento1 bus2 81) Compiling architecture ideal of entity off foff default) Compiling architecture ideal of entity muxoff fmuxoff23) </pre>	<pre> &gt; xst -dlm rep file usinfo_mux_n to 1 bus.vst Release 14.7 - xst P 20131013 (m64) Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved. =&gt; Parameter THRESHOLD set to 1astoprow.mio Total REAL time to Xst completion: 1.00 secs Total CPU time to Xst completion: 0.22 secs  -&gt; WARNING:Xst-3164 - Option "debug" found multiple times in the command line. Only the first occurrence is considered. * HDL Compilation Compiling vhdl file "muento1.vhd" in Library work Entity &lt;muento1&gt; compiled. Entity &lt;muento1&gt; (Architecture &lt;+&gt;) compiled. Compiling vhdl file "off.vhd" in Library work Entity &lt;off&gt; compiled. Entity &lt;off&gt; (Architecture &lt;+&gt;) compiled. Compiling vhdl file "muxoff.vhd" in Library work Entity &lt;muxoff&gt; compiled. Entity &lt;muxoff&gt; (Architecture &lt;+&gt;) compiled. Compiling vhdl file "req file functions.vhd" in Library work Package &lt;req file functions&gt; compiled. Package body &lt;req file functions&gt; compiled. Compiling vhdl file "dmuento1.vhd" in Library work Entity &lt;dmuento1&gt; compiled. Entity &lt;dmuento1&gt; (Architecture &lt;+&gt;) compiled. Compiling vhdl file "muento1 bus.vhd" in Library work Entity &lt;muento1 bus&gt; compiled. Entity &lt;muento1 bus&gt; (Architecture &lt;+&gt;) compiled. Compiling vhdl file "shift_req.vhd" in Library work Entity &lt;shift_req&gt; compiled. Entity &lt;shift_req&gt; (Architecture &lt;+&gt;) compiled. Compiling vhdl file "req file.vhd" in Library work Entity &lt;req file&gt; compiled. Entity &lt;req file&gt; (Architecture &lt;NDV&gt;) compiled. Total REAL time to Xst completion: 2.00 secs Total CPU time to Xst completion: 1.51 secs  -&gt; Total memory usage is 4477112 kilobytes Number of errors : 0 ( 0 filtered) Number of warnings : 1 ( 0 filtered) Number of infos : 0 ( 0 filtered) &gt;Use incremental -o rep file usinfo_mux_n to 1 bus.isim both.exe -o rep file usinfo_mux_n to 1 bus.art -o rep file Run P-40121012 (signature 6a770876b0) Number of CPUs detected in this system: 4 Turning on multi-threading, number of parallel sub-compilation jobs: 16 Determining compilation order of HDL files Parsing VHDL file "muento1.vhd" into library work Parsing VHDL file "off.vhd" into library work Parsing VHDL file "req file functions.vhd" into library work Parsing VHDL file "muxoff.vhd" into library work Parsing VHDL file "shift_req.vhd" into library work Parsing VHDL file "dmuento1.vhd" into library work Parsing VHDL file "muento1 bus.vhd" into library work Parsing VHDL file "req file.vhd" into library work Starting static elaboration Completed static elaboration Compiling package standard Compiling package std_logic_1164 Compiling package req file functions Compiling package math_real Compiling package numeric_std Compiling architecture of entity dmuento1 fdmuento123) Compiling architecture of entity muento1 fmuento123) Compiling architecture of entity muento1 bus fmuento1 bus2 81) Compiling architecture of entity off foff default) Compiling architecture of entity muxoff fmuxoff23) </pre>
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<pre> &gt;set -f; set file_name IDEAL_mux_n.to_1_bus.vst Release 14.7 - set P 20131013 (m64) Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved. =&gt; Parameter THPDR set to: testonnew.bm Total REAL time to Xst completion: 0.00 secs Total CPU time to Xst completion: 0.22 secs  -&gt; WARNING:Xst-3164 - Option "debug" found multiple times in the command line. Only the first occurrence is considered. * HDL Compilation Compiling vhdl file "muento1.vhd" in Library work Entity &lt;muento1&gt; (Architecture &lt;ideal&gt;) compiled Compiling vhdl file "off.vhd" in Library work Entity &lt;off&gt; compiled Entity &lt;off&gt; (Architecture &lt;ideal&gt;) compiled Compiling vhdl file "muxoff.vhd" in Library work Entity &lt;muxoff&gt; compiled Entity &lt;muxoff&gt; (Architecture &lt;ideal&gt;) compiled Compiling vhdl file "seq file functions.vhd" in Library work Package &lt;seq file functions&gt; compiled Package body &lt;seq file functions&gt; compiled Compiling vhdl file "dmuento1.vhd" in Library work Entity &lt;dmuento1&gt; compiled Entity &lt;dmuento1&gt; (Architecture &lt;ideal&gt;) compiled Compiling vhdl file "muento1_bus IDEAL.vhd" in Library work Entity &lt;muento1_bus&gt; compiled Entity &lt;muento1_bus&gt; (Architecture &lt;ideal&gt;) compiled Compiling vhdl file "shift_reg.vhd" in Library work Entity &lt;shift_reg&gt; compiled Entity &lt;shift_reg&gt; (Architecture &lt;ideal&gt;) compiled Compiling vhdl file "seq file.vhd" in Library work Entity &lt;seq file&gt; compiled Entity &lt;seq file&gt; (Architecture &lt;NDV&gt;) compiled Total REAL time to Xst completion: 1.00 secs Total CPU time to Xst completion: 1.14 secs  -&gt; Total memory usage is 4477180 kilobytes Number of errors - 0 ( 0 filtered) Number of warnings - 1 ( 0 filtered) Number of infos - 0 ( 0 filtered) &gt;save incremental -o rep file_name IDEAL_mux_n.to_1_bus.isim both.exe -o1 rep file_name IDEAL_mux_n.to_1_bus.o1.doc rep file Run P-4012013 (signature 6a770876b) Number of CPUs detected in this system: 4 Turning on multi-threading, number of parallel sub-compilation jobs: 16 Determining compilation order of HDL files Parsing VHDL file "muento1.vhd" into library work Parsing VHDL file "off.vhd" into library work Parsing VHDL file "seq file functions.vhd" into library work Parsing VHDL file "muxoff.vhd" into library work Parsing VHDL file "dmuento1.vhd" into library work Parsing VHDL file "muento1_bus IDEAL.vhd" into library work Parsing VHDL file "seq file.vhd" into library work Starting static elaboration Completed static elaboration Compiling package standard Compiling package std logic 1164 Compiling package seq file functions Compiling package math real Compiling package numeric std Compiling architecture ideal of entity dmuento1 fdmuento123) Compiling architecture ideal of entity muento1 fmiento1123) Compiling architecture ideal of entity muento1_bus fmiento1_bus2 81) Compiling architecture ideal of entity off foff default) Compiling architecture ideal of entity muxoff fmuxoff23) </pre>	<pre> &gt;set -f; set file_name mux_n.to_1_bus.vst Release 14.7 - set P 20131013 (m64) Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved. =&gt; Parameter THPDR set to: testonnew.bm Total REAL time to Xst completion: 1.00 secs Total CPU time to Xst completion: 0.22 secs  -&gt; WARNING:Xst-3164 - Option "debug" found multiple times in the command line. Only the first occurrence is considered. * HDL Compilation Compiling vhdl file "muento1.vhd" in Library work Entity &lt;muento1&gt; compiled Entity &lt;muento1&gt; (Architecture &lt;+&gt;) compiled Compiling vhdl file "off.vhd" in Library work Entity &lt;off&gt; compiled Entity &lt;off&gt; (Architecture &lt;+&gt;) compiled Compiling vhdl file "muxoff.vhd" in Library work Entity &lt;muxoff&gt; compiled Entity &lt;muxoff&gt; (Architecture &lt;+&gt;) compiled Compiling vhdl file "seq file functions.vhd" in Library work Package &lt;seq file functions&gt; compiled Package body &lt;seq file functions&gt; compiled Compiling vhdl file "dmuento1.vhd" in Library work Entity &lt;dmuento1&gt; compiled Entity &lt;dmuento1&gt; (Architecture &lt;+&gt;) compiled Compiling vhdl file "muento1_bus.vhd" in Library work Entity &lt;muento1_bus&gt; compiled Entity &lt;muento1_bus&gt; (Architecture &lt;+&gt;) compiled Compiling vhdl file "shift_reg.vhd" in Library work Entity &lt;shift_reg&gt; compiled Entity &lt;shift_reg&gt; (Architecture &lt;+&gt;) compiled Compiling vhdl file "seq file.vhd" in Library work Entity &lt;seq file&gt; compiled Entity &lt;seq file&gt; (Architecture &lt;NDV&gt;) compiled Total REAL time to Xst completion: 2.00 secs Total CPU time to Xst completion: 1.51 secs  -&gt; Total memory usage is 4477112 kilobytes Number of errors - 0 ( 0 filtered) Number of warnings - 1 ( 0 filtered) Number of infos - 0 ( 0 filtered) &gt;save incremental -o rep file_name mux_n.to_1_bus.isim both.exe -o1 rep file_name mux_n.to_1_bus.o1.doc rep file Run P-4012013 (signature 6a770876b) Number of CPUs detected in this system: 4 Turning on multi-threading, number of parallel sub-compilation jobs: 16 Determining compilation order of HDL files Parsing VHDL file "muento1.vhd" into library work Parsing VHDL file "off.vhd" into library work Parsing VHDL file "seq file functions.vhd" into library work Parsing VHDL file "muxoff.vhd" into library work Parsing VHDL file "dmuento1.vhd" into library work Parsing VHDL file "muento1_bus.vhd" into library work Parsing VHDL file "seq file.vhd" into library work Starting static elaboration Completed static elaboration Compiling package standard Compiling package std logic 1164 Compiling package seq file functions Compiling package math real Compiling package numeric std Compiling architecture of entity dmuento1 fdmuento123) Compiling architecture of entity muento1 fmiento1123) Compiling architecture of entity muento1_bus fmiento1_bus2 81) Compiling architecture of entity off foff default) Compiling architecture of entity muxoff fmuxoff23) </pre>
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<pre> &gt;set -f; set file_name IDEAL_mux_n_to_1_bus.vst Release 14.7 - set P 20131013 (m64) Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved. =&gt; Parameter THPDR set to: testonpara.mn Total REAL time to Xst completion: 0.00 secs Total CPU time to Xst completion: 0.22 secs  -&gt; WARNING:Xst-3164 - Option "debug" found multiple times in the command line. Only the first occurrence is considered. * HDL Compilation Compiling vhdl file "muento1.vhd" in Library work Entity &lt;muento1&gt; (Architecture &lt;ideal&gt;) compiled. Compiling vhdl file "off.vhd" in Library work Entity &lt;off&gt; compiled. Entity &lt;off&gt; (Architecture &lt;ideal&gt;) compiled. Compiling vhdl file "muxoff.vhd" in Library work Entity &lt;muxoff&gt; compiled. Entity &lt;muxoff&gt; (Architecture &lt;ideal&gt;) compiled. Compiling vhdl file "seq_file_functions.vhd" in Library work Package &lt;seq_file_functions&gt; compiled. Package body &lt;seq_file_functions&gt; compiled. Compiling vhdl file "dmuento1.vhd" in Library work Entity &lt;dmuento1&gt; compiled. Entity &lt;dmuento1&gt; (Architecture &lt;ideal&gt;) compiled. Compiling vhdl file "muento1_bus IDEAL.vhd" in Library work Entity &lt;muento1_bus&gt; compiled. Entity &lt;muento1_bus&gt; (Architecture &lt;ideal&gt;) compiled. Compiling vhdl file "shift_reg.vhd" in Library work Entity &lt;shift_reg&gt; compiled. Entity &lt;shift_reg&gt; (Architecture &lt;ideal&gt;) compiled. Compiling vhdl file "seq_file.vhd" in Library work Entity &lt;seq_file&gt; compiled. Entity &lt;seq_file&gt; (Architecture &lt;NDV&gt;) compiled. Total REAL time to Xst completion: 1.00 secs Total CPU time to Xst completion: 1.61 secs  -&gt; Total memory usage is 4477112 kilobytes. Number of errors : 0 ( 0 filtered) Number of warnings : 1 ( 0 filtered) Number of infos : 0 ( 0 filtered) &gt;Use incremental compilation IDEAL_mux_n_to_1_bus.ism both.exe.vst.reg.file_name IDEAL_mux_n_to_1_bus.vst.seq.reg.file Run P-40121013 (signature 6a7708060) Number of CPUs detected in this system: 4 Turning on multi-threading, number of parallel sub-compilation jobs: 16 Determining compilation order of HDL files Parsing VHDL file "muento1.vhd" into library work Parsing VHDL file "off.vhd" into library work Parsing VHDL file "seq_file_functions.vhd" into library work Parsing VHDL file "muxoff.vhd" into library work Parsing VHDL file "shift_reg.vhd" into library work Parsing VHDL file "dmuento1.vhd" into library work Parsing VHDL file "muento1_bus IDEAL.vhd" into library work Parsing VHDL file "seq_file.vhd" into library work Starting static elaboration Completed static elaboration Compiling package standard Compiling package std_logic_1164 Compiling package seq_file_functions Compiling package math_real Compiling package numeric_std Compiling architecture ideal of entity dmuento1 fdmuento123) Compiling architecture ideal of entity muento1 fmuento123) Compiling architecture ideal of entity muento1_bus fmuento1_bus2 81) Compiling architecture ideal of entity off foff default) Compiling architecture ideal of entity muxoff fmuxoff23) </pre>	<pre> &gt;set -f; set file_name IDEAL_mux_n_to_1_bus.vst Release 14.7 - set P 20131013 (m64) Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved. =&gt; Parameter THPDR set to: testonpara.mn Total REAL time to Xst completion: 1.00 secs Total CPU time to Xst completion: 0.22 secs  -&gt; WARNING:Xst-3164 - Option "debug" found multiple times in the command line. Only the first occurrence is considered. * HDL Compilation Compiling vhdl file "muento1.vhd" in Library work Entity &lt;muento1&gt; compiled. Entity &lt;muento1&gt; (Architecture &lt;+&gt;) compiled. Compiling vhdl file "off.vhd" in Library work Entity &lt;off&gt; compiled. Entity &lt;off&gt; (Architecture &lt;+&gt;) compiled. Compiling vhdl file "muxoff.vhd" in Library work Entity &lt;muxoff&gt; compiled. Entity &lt;muxoff&gt; (Architecture &lt;+&gt;) compiled. Compiling vhdl file "seq_file_functions.vhd" in Library work Package &lt;seq_file_functions&gt; compiled. Package body &lt;seq_file_functions&gt; compiled. Compiling vhdl file "dmuento1.vhd" in Library work Entity &lt;dmuento1&gt; compiled. Entity &lt;dmuento1&gt; (Architecture &lt;+&gt;) compiled. Compiling vhdl file "muento1_bus.vhd" in Library work Entity &lt;muento1_bus&gt; compiled. Entity &lt;muento1_bus&gt; (Architecture &lt;+&gt;) compiled. Compiling vhdl file "shift_reg.vhd" in Library work Entity &lt;shift_reg&gt; compiled. Entity &lt;shift_reg&gt; (Architecture &lt;+&gt;) compiled. Compiling vhdl file "seq_file.vhd" in Library work Entity &lt;seq_file&gt; compiled. Entity &lt;seq_file&gt; (Architecture &lt;NDV&gt;) compiled. Total REAL time to Xst completion: 2.00 secs Total CPU time to Xst completion: 1.51 secs  -&gt; Total memory usage is 4477112 kilobytes. Number of errors : 0 ( 0 filtered) Number of warnings : 1 ( 0 filtered) Number of infos : 0 ( 0 filtered) &gt;Use incremental compilation IDEAL_mux_n_to_1_bus.ism both.exe.vst.reg.file_name IDEAL_mux_n_to_1_bus.vst.seq.reg.file Run P-40121013 (signature 6a7708060) Number of CPUs detected in this system: 4 Turning on multi-threading, number of parallel sub-compilation jobs: 16 Determining compilation order of HDL files Parsing VHDL file "muento1.vhd" into library work Parsing VHDL file "off.vhd" into library work Parsing VHDL file "seq_file_functions.vhd" into library work Parsing VHDL file "muxoff.vhd" into library work Parsing VHDL file "shift_reg.vhd" into library work Parsing VHDL file "dmuento1.vhd" into library work Parsing VHDL file "muento1_bus.vhd" into library work Parsing VHDL file "seq_file.vhd" into library work Starting static elaboration Completed static elaboration Compiling package standard Compiling package std_logic_1164 Compiling package seq_file_functions Compiling package math_real Compiling package numeric_std Compiling architecture of entity dmuento1 fdmuento123) Compiling architecture of entity muento1 fmuento123) Compiling architecture of entity muento1_bus fmuento1_bus2 81) Compiling architecture of entity off foff default) Compiling architecture of entity muxoff fmuxoff23) </pre>
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<pre> &gt;set -dn; set -f; unset -DEAL; mvx n to 1 bus.vst Release 14.7 - set P 20131013 (m64) Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved. =&gt; Parameter THPDR set to: testonnew.bm Total REAL time to Xst completion: 0.90 secs Total CPU time to Xst completion: 0.23 secs --&gt; WARNING:Xst-3164 - Option "debug" found multiple times in the command line. Only the first occurrence is considered. * HDL Compilation Compiling vhdl file "muento1.vhd" in Library work Entity &lt;muento1&gt; (Architecture &lt;ideast&gt;) compiled. Entity &lt;muento1&gt; (Architecture &lt;ideast&gt;) compiled. Compiling vhdl file "off.vhd" in Library work Entity &lt;off&gt; compiled. Entity &lt;off&gt; (Architecture &lt;ideast&gt;) compiled. Compiling vhdl file "muxoff.vhd" in Library work Entity &lt;muxoff&gt; compiled. Entity &lt;muxoff&gt; (Architecture &lt;ideast&gt;) compiled. Compiling vhdl file "req file functions.vhd" in Library work Package &lt;req file functions&gt; compiled. Package body &lt;req file functions&gt; compiled. Compiling vhdl file "dmuento1.vhd" in Library work Entity &lt;dmuento1&gt; compiled. Entity &lt;dmuento1&gt; (Architecture &lt;ideast&gt;) compiled. Compiling vhdl file "muento1 bus IDEAL.vhd" in Library work Entity &lt;muento1 bus&gt; compiled. Entity &lt;muento1 bus&gt; (Architecture &lt;ideast&gt;) compiled. Compiling vhdl file "shift_req.vhd" in Library work Entity &lt;shift_req&gt; compiled. Entity &lt;shift_req&gt; (Architecture &lt;ideast&gt;) compiled. Compiling vhdl file "req file.vhd" in Library work Entity &lt;req file&gt; compiled. Entity &lt;req file&gt; (Architecture &lt;behavior&gt;) compiled. Total REAL time to Xst completion: 2.00 secs Total CPU time to Xst completion: 2.34 secs --&gt; Total memory usage is 4477104 kilobytes Number of errors - 0 ( 0 filtered) Number of warnings - 1 ( 0 filtered) Number of infos - 0 ( 0 filtered) &gt;Wave incremental -&gt; rep file unset -DEAL; mvx n to 1 bus; setm both.exe -rt rep file unset -DEAL; mvx n to 1 bus; setm both.exe -rt rep file Run P-40121012 (signature 6a7708f0b0) Number of CPUs detected in this system: 4 Turning on multi-threading, number of parallel sub-compilation jobs: 16 Determining compilation order of HDL files Parsing VHDL file "muento1.vhd" into library work Parsing VHDL file "off.vhd" into library work Parsing VHDL file "req file functions.vhd" into library work Parsing VHDL file "muxoff.vhd" into library work Parsing VHDL file "dmuento1.vhd" into library work Parsing VHDL file "muento1 bus IDEAL.vhd" into library work Parsing VHDL file "shift_req.vhd" into library work Starting static elaboration Completed static elaboration Compiling package standard Compiling package std logic 1164 Compiling package req file functions Compiling package math real Compiling package numeric std Compiling architecture ideal of entity dmuento1 fdmuento123) Compiling architecture ideal of entity muento1 fmuento123) Compiling architecture ideal of entity muento1 bus fmuento1 bus2 81) Compiling architecture ideal of entity off foff default) Compiling architecture ideal of entity muxoff fmuxoff23) </pre>	<pre> &gt;set -dn; set -f; unset -mvx n to 1 bus.vst Release 14.7 - set P 20131013 (m64) Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved. =&gt; Parameter THPDR set to: testonnew.bm Total REAL time to Xst completion: 1.00 secs Total CPU time to Xst completion: 0.22 secs --&gt; WARNING:Xst-3164 - Option "debug" found multiple times in the command line. Only the first occurrence is considered. * HDL Compilation Compiling vhdl file "muento1.vhd" in Library work Entity &lt;muento1&gt; compiled. Entity &lt;muento1&gt; (Architecture &lt;+&gt;) compiled. Compiling vhdl file "off.vhd" in Library work Entity &lt;off&gt; compiled. Entity &lt;off&gt; (Architecture &lt;+&gt;) compiled. Compiling vhdl file "muxoff.vhd" in Library work Entity &lt;muxoff&gt; compiled. Entity &lt;muxoff&gt; (Architecture &lt;+&gt;) compiled. Compiling vhdl file "req file functions.vhd" in Library work Package &lt;req file functions&gt; compiled. Package body &lt;req file functions&gt; compiled. Compiling vhdl file "dmuento1.vhd" in Library work Entity &lt;dmuento1&gt; compiled. Entity &lt;dmuento1&gt; (Architecture &lt;+&gt;) compiled. Compiling vhdl file "muento1 bus .vhd" in Library work Entity &lt;muento1 bus&gt; compiled. Entity &lt;muento1 bus&gt; (Architecture &lt;+&gt;) compiled. Compiling vhdl file "shift_req.vhd" in Library work Entity &lt;shift_req&gt; compiled. Entity &lt;shift_req&gt; (Architecture &lt;+&gt;) compiled. Compiling vhdl file "req file.vhd" in Library work Entity &lt;req file&gt; compiled. Entity &lt;req file&gt; (Architecture &lt;NDV&gt;) compiled. Total REAL time to Xst completion: 2.00 secs Total CPU time to Xst completion: 1.51 secs --&gt; Total memory usage is 4477112 kilobytes Number of errors - 0 ( 0 filtered) Number of warnings - 1 ( 0 filtered) Number of infos - 0 ( 0 filtered) &gt;Wave incremental -&gt; rep file unset -mvx n to 1 bus; setm both.exe -rt rep file unset -mvx n to 1 bus; setm both.exe -rt rep file Run P-40121012 (signature 6a7708f0b0) Number of CPUs detected in this system: 4 Turning on multi-threading, number of parallel sub-compilation jobs: 16 Determining compilation order of HDL files Parsing VHDL file "muento1.vhd" into library work Parsing VHDL file "off.vhd" into library work Parsing VHDL file "req file functions.vhd" into library work Parsing VHDL file "muxoff.vhd" into library work Parsing VHDL file "dmuento1.vhd" into library work Parsing VHDL file "muento1 bus .vhd" into library work Parsing VHDL file "shift_req.vhd" into library work Starting static elaboration Completed static elaboration Compiling package standard Compiling package std logic 1164 Compiling package req file functions Compiling package math real Compiling package numeric std Compiling architecture of entity dmuento1 fdmuento123) Compiling architecture of entity muento1 fmuento123) Compiling architecture of entity muento1 bus fmuento1 bus2 81) Compiling architecture of entity off foff default) Compiling architecture of entity muxoff fmuxoff23) </pre>
---	--





>xst -ifn reg\_file\_using\_\_mux\_n\_to\_1\_bus.xst  
Release 14.7 - xst P.20131013 (nt64)  
Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.  
--> Parameter TMPDIR set to ./xst/projnav.tmp  
Total REAL time to Xst completion: 1.00 secs  
Total CPU time to Xst completion: 0.22 secs

--> WARNING:Xst:3164 - Option "-debug" found multiple times in the command line. Only the first occurrence is used.

```
*           HDL Compilation           *
```

Compiling vhdl file "/muxnto1.vhd" in Library work.  
Entity <muxnto1> compiled.  
Entity <muxnto1> (Architecture <>) compiled.  
Compiling vhdl file "/dff.vhd" in Library work.  
Entity <dff> compiled.  
Entity <dff> (Architecture <>) compiled.  
Compiling vhdl file "/muxdff.vhd" in Library work.  
Entity <muxdff> compiled.  
Entity <muxdff> (Architecture <>) compiled.  
Compiling vhdl file "/reg\_file\_functions.vhd" in Library work.  
Package <reg\_file\_functions> compiled.  
Package body <reg\_file\_functions> compiled.  
Compiling vhdl file "/dmuxnto1.vhd" in Library work.  
Entity <dmuxnto1> compiled.  
Entity <dmuxnto1> (Architecture <>) compiled.  
Compiling vhdl file "/muxnto1\_bus\_.vhd" in Library work.  
Entity <muxnto1\_bus> compiled.  
Entity <muxnto1\_bus> (Architecture <>) compiled.  
Compiling vhdl file "/shift\_reg.vhd" in Library work.  
Entity <shift\_reg> compiled.  
Entity <shift\_reg> (Architecture <>) compiled.  
Compiling vhdl file "/reg\_file.vhd" in Library work.  
Entity <reg\_file> compiled.  
Entity <reg\_file> (Architecture <NDV>) compiled.  
Total REAL time to Xst completion: 2.00 secs  
Total CPU time to Xst completion: 1.51 secs

-->

Total memory usage is 4477112 kilobytes  
Number of errors : 0 ( 0 filtered)  
Number of warnings : 1 ( 0 filtered)  
Number of infos : 0 ( 0 filtered)  
>fuse -incremental -o reg\_file\_using\_\_mux\_n\_to\_1\_bus\_isim\_beh.exe -prj reg\_file\_using\_\_mux\_n\_to\_1\_bus\_isim P.20131013 (signature 0x7708f090)  
Number of CPUs detected in this system: 8  
Turning on mult-threading, number of parallel sub-compilation jobs: 16  
Determining compilation order of HDL files  
Parsing VHDL file "muxnto1.vhd" into library work  
Parsing VHDL file "dff.vhd" into library work  
Parsing VHDL file "reg\_file\_functions.vhd" into library work  
Parsing VHDL file "muxdff.vhd" into library work  
Parsing VHDL file "shift\_reg.vhd" into library work  
Parsing VHDL file "muxnto1\_bus\_.vhd" into library work  
Parsing VHDL file "dmuxnto1.vhd" into library work  
Parsing VHDL file "reg\_file.vhd" into library work  
Starting static elaboration  
Completed static elaboration  
Compiling package standard  
Compiling package std\_logic\_1164

Compiling package reg\_file\_functions  
Compiling package math\_real  
Compiling package numeric\_std  
Compiling architecture of entity dmuxnto1 [dmuxnto1(2)]  
Compiling architecture of entity muxnto1 [muxnto1(2)]  
Compiling architecture of entity muxnto1\_bus [muxnto1\_bus(2,8)]  
Compiling architecture of entity dff [dff\_default]  
Compiling architecture of entity muxdff [muxdff(2)]  
Compiling architecture of entity shift\_reg [shift\_reg(8)]  
Compiling architecture ndv of entity reg\_file  
Time Resolution for simulation is 1ps.  
Waiting for 1 sub-compilation(s) to finish...  
Compiled 18 VHDL Units  
Built simulation executable reg\_file\_using\_\_mux\_n\_to\_1\_bus\_isim\_beh.exe  
Fuse Memory Usage: 36592 KB  
Fuse CPU Usage: 936 ms  
>xst -ifn reg\_file\_tb\_using\_\_mux\_n\_to\_1\_bus.xst  
Release 14.7 - xst P.20131013 (nt64)  
Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.  
--> Parameter TMPDIR set to ./xst/projnav.tmp  
Total REAL time to Xst completion: 0.00 secs  
Total CPU time to Xst completion: 0.23 secs

--> WARNING:Xst:3164 - Option "-debug" found multiple times in the command line. Only the first occurrence

```
*                HDL Compilation                *
```

Compiling vhdl file "/muxnto1.vhd" in Library work.  
Architecture of Entity muxnto1 is up to date.  
Compiling vhdl file "/dff.vhd" in Library work.  
Architecture of Entity dff is up to date.  
Compiling vhdl file "/muxdff.vhd" in Library work.  
Architecture of Entity muxdff is up to date.  
Compiling vhdl file "/reg\_file\_functions.vhd" in Library work.  
Architecture reg\_file\_functions of Entity reg\_file\_functions is up to date.  
Compiling vhdl file "/dmuxnto1.vhd" in Library work.  
Architecture of Entity dmuxnto1 is up to date.  
Compiling vhdl file "/muxnto1\_bus.vhd" in Library work.  
Architecture of Entity muxnto1\_bus is up to date.  
Compiling vhdl file "/shift\_reg.vhd" in Library work.  
Architecture of Entity shift\_reg is up to date.  
Compiling vhdl file "/reg\_file.vhd" in Library work.  
Architecture ndv of Entity reg\_file is up to date.  
Compiling vhdl file "/reg\_file\_\_tb\_using\_\_mux\_n\_to\_1\_bus.vhd" in Library work.  
Entity <reg\_file\_tb\_using\_\_mux\_n\_to\_1\_bus> compiled.  
ERROR:HDLParasers:1015 - "/reg\_file\_\_tb\_using\_\_mux\_n\_to\_1\_bus.vhd" Line 67. Wait for statement u  
ERROR:HDLParasers:1015 - "/reg\_file\_\_tb\_using\_\_mux\_n\_to\_1\_bus.vhd" Line 69. Wait for statement u  
Total REAL time to Xst completion: 1.00 secs  
Total CPU time to Xst completion: 0.67 secs

-->

Total memory usage is 4477124 kilobytes  
Number of errors : 2 ( 0 filtered)  
Number of warnings : 1 ( 0 filtered)  
Number of infos : 0 ( 0 filtered)  
>fuse -incremental -o reg\_file\_tb\_using\_\_mux\_n\_to\_1\_bus.exe -prj reg\_file\_tb\_using\_\_mux\_n\_to\_1\_b  
ISim P.20131013 (signature 0x7708f090)  
Number of CPUs detected in this system: 8  
Turning on mult-threading, number of parallel sub-compilation jobs: 16  
Determining compilation order of HDL files  
Parsing VHDL file "muxnto1.vhd" into library work



```

Parsing VHDL file "dff.vhd" into library work
Parsing VHDL file "reg_file_functions.vhd" into library work
Parsing VHDL file "muxdff.vhd" into library work
Parsing VHDL file "shift_reg.vhd" into library work
Parsing VHDL file "muxnto1_bus.vhd" into library work
Parsing VHDL file "dmuxnto1.vhd" into library work
Parsing VHDL file "reg_file.vhd" into library work
Parsing VHDL file "reg_file__tb_using__mux_n_to_1_bus.vhd" into library work
Starting static elaboration
Completed static elaboration
Compiling package standard
Compiling package std_logic_1164
Compiling package numeric_std
Compiling package reg_file_functions
Compiling package textio
Compiling package std_logic_textio
Compiling package math_real
Compiling architecture of entity dmuxnto1 [\dmuxnto1(3)\]
Compiling architecture of entity muxnto1 [\muxnto1(3)\]
Compiling architecture of entity muxnto1_bus [\muxnto1_bus(3,8)\]
Compiling architecture of entity muxnto1 [\muxnto1(2)\]
Compiling architecture of entity dff [dff_default]
Compiling architecture of entity muxdff [\muxdff(2)\]
Compiling architecture of entity shift_reg [\shift_reg(8)\]
Compiling architecture ndv of entity reg_file [\reg_file(8,8)\]
Compiling architecture of entity reg_file_tb_using__mux_n_to...
Time Resolution for simulation is 1ps.
Waiting for 1 sub-compilation(s) to finish...
Compiled 24 VHDL Units
Built simulation executable reg_file_tb_using__mux_n_to_1_bus.exe
Fuse Memory Usage: 37700 KB
Fuse CPU Usage: 1077 ms
>xst -ifn mux_n_to_1_bus.xst
Release 14.7 - xst P.20131013 (nt64)
Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.
--> Parameter TMPDIR set to ./xst/projnav.tmp
Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.23 secs

```

```

--> WARNING:Xst:3164 - Option "-debug" found multiple times in the command line. Only the first occurrence
*          HDL Compilation          *

```

```

WARNING:HDLParasers:3607 - Unit work/muxnto1_bus is now defined in a different file. It was defined
WARNING:HDLParasers:3607 - Unit work/muxnto1_bus/ is now defined in a different file. It was defined

```

```

Compiling vhdI file "/muxnto1.vhd" in Library work.
Architecture of Entity muxnto1 is up to date.
Compiling vhdI file "/dff.vhd" in Library work.
Architecture of Entity dff is up to date.
Compiling vhdI file "/reg_file_functions.vhd" in Library work.
Architecture reg_file_functions of Entity reg_file_functions is up to date.
Compiling vhdI file "/muxnto1_bus.vhd" in Library work.
Architecture of Entity muxnto1_bus is up to date.
Compiling vhdI file "/muxdff.vhd" in Library work.
Architecture of Entity muxdff is up to date.
Compiling vhdI file "/dmuxnto1.vhd" in Library work.
Architecture of Entity dmuxnto1 is up to date.
Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.38 secs

```

```

-->

```

Total memory usage is 4477124 kilobytes  
 Number of errors : 0 ( 0 filtered)  
 Number of warnings : 3 ( 0 filtered)  
 Number of infos : 0 ( 0 filtered)  
 >fuse -incremental -o mux\_n\_to\_1\_bus\_tb\_isim\_beh.exe -prj mux\_n\_to\_1\_bus\_tb.prj -top muxnto1\_bu  
 ISim P.20131013 (signature 0x7708f090)  
 Number of CPUs detected in this system: 8  
 Turning on mult-threading, number of parallel sub-compilation jobs: 16  
 Determining compilation order of HDL files  
 Parsing VHDL file "reg\_file\_functions.vhd" into library work  
 Parsing VHDL file "dff.vhd" into library work  
 Parsing VHDL file "dmuxnto1.vhd" into library work  
 Parsing VHDL file "muxdff.vhd" into library work  
 Parsing VHDL file "muxnto1.vhd" into library work  
 Parsing VHDL file "muxnto1\_bus.vhd" into library work  
 Parsing VHDL file "muxnto1\_bus\_\_tb.vhd" into library work  
 Starting static elaboration  
 Completed static elaboration  
 Compiling package standard  
 Compiling package std\_logic\_1164  
 Compiling package numeric\_std  
 Compiling package textio  
 Compiling package std\_logic\_textio  
 Compiling package reg\_file\_functions  
 Compiling architecture of entity muxnto1 [\muxnto1(2)\]  
 Compiling architecture of entity muxnto1\_bus [\muxnto1\_bus(2,8)\]  
 Compiling architecture tb of entity muxnto1\_bus\_tb  
 Time Resolution for simulation is 1ps.  
 Waiting for 1 sub-compilation(s) to finish...  
 Compiled 11 VHDL Units  
 Built simulation executable mux\_n\_to\_1\_bus\_tb\_isim\_beh.exe  
 Fuse Memory Usage: 36956 KB  
 Fuse CPU Usage: 999 ms  
 >mux\_n\_to\_1\_bus\_tb\_isim\_beh.exe -tclbatch isim\_muxnto1\_bus.tcl -wdb mux\_n\_to\_1\_bus\_tb\_isim\_b  
 ISim P.20131013 (signature 0x7708f090)  
 WARNING: A WEBPACK license was found.  
 WARNING: Please use Xilinx License Configuration Manager to check out a full ISim license.  
 WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for more information on t  
 This is a Lite version of ISim.  
 Time resolution is 1 ps  
 Number of addressess: 2  
 Clk period: 20000 ps  
 Total simulation time is: 80000 ps  
 Simulator is doing circuit initialization process.  
 Finished circuit initialization process.  
 >reg\_file\_tb\_using\_\_mux\_n\_to\_1\_bus.exe -tclbatch isim\_reg\_file.tcl -wdb reg\_file\_tb\_using\_\_mux\_n\_t  
 ISim P.20131013 (signature 0x7708f090)  
 WARNING: A WEBPACK license was found.  
 WARNING: Please use Xilinx License Configuration Manager to check out a full ISim license.  
 WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for more information on t  
 This is a Lite version of ISim.  
 Time resolution is 1 ps  
 Number of registers: 8  
 Clk period: 20000 ps  
 Total simulation time is: 320000 ps  
 Simulator is doing circuit initialization process.  
 Finished circuit initialization process.  
 at 0 ps, Instance /reg\_file\_tb\_using\_\_mux\_n\_to\_1\_bus/UUT/regloop(7)\VRegi\I1(0)\U0/U0/ : Warning:  
 at 0 ps, Instance /reg\_file\_tb\_using\_\_mux\_n\_to\_1\_bus/UUT/regloop(7)\VRegi\I1(1)\U0/U0/ : Warning:

[illegible]

at 0 ps, Instance /reg\_file\_tb\_using\_\_mux\_n\_to\_1\_bus/UUT/regloop(0)\Regi/I1(5)\U0/U0/ : Warning:  
at 0 ps, Instance /reg\_file\_tb\_using\_\_mux\_n\_to\_1\_bus/UUT/regloop(0)\Regi/I1(6)\U0/U0/ : Warning:  
at 0 ps, Instance /reg\_file\_tb\_using\_\_mux\_n\_to\_1\_bus/UUT/regloop(0)\Regi/I1(7)\U0/U0/ : Warning:

rence is considered.

1\_bus.prj -top reg\_file

rence is considered.

insupported.  
insupported.

js.prj -top reg\_file\_tb\_using\_\_mux\_n\_to\_1\_bus

rence is considered.

in "/muxnto1\_bus\_.vhd", and is now defined in "/muxnto1\_bus.vhd".  
l in "/muxnto1\_bus\_.vhd", and is now defined in "/muxnto1\_bus.vhd".

s\_tb

sh.wdb

the differences between the Lite and the Full version.

c\_1\_bus.wdb

the differences between the Lite and the Full version.

NUMERIC\_STD.TO\_INTEGER: metavalue detected, returning 0  
NUMERIC\_STD.TO\_INTEGER: metavalue detected, returning 0



[illegible]

NUMERIC\_STD.TO\_INTEGER: metavalue detected, returning 0  
NUMERIC\_STD.TO\_INTEGER: metavalue detected, returning 0  
NUMERIC\_STD.TO\_INTEGER: metavalue detected, returning 0