

-- **** STUDENT: 64000225.....	2
-- KOMENTARJI K OCENI NALOGE -- Matej Možek: Ni pripomb.....	2
-- **** STUDENT: 64200100.....	5
-- KOMENTARJI K OCENI NALOGE -- Matej Možek: Ni pripomb.....	5
-- **** STUDENT: 64200163.....	7
-- KOMENTARJI K OCENI NALOGE -- Matej Možek: Ni pripomb.....	7
-- **** STUDENT: 64200238.....	9
-- KOMENTARJI K OCENI NALOGE -- Matej Možek: Ni pripomb.....	9
-- **** STUDENT: 64200288.....	13
-- KOMENTARJI K OCENI NALOGE -- Matej Možek: Ni pripomb.....	13
-- **** STUDENT: 64200296.....	15
-- KOMENTARJI K OCENI NALOGE -- Matej Možek: Ni pripomb.....	15
-- **** STUDENT: 64200385.....	19
-- KOMENTARJI K OCENI NALOGE -- Matej Možek: Ni pripomb.....	19
-- **** STUDENT: 64210113.....	22
-- KOMENTARJI K OCENI NALOGE -- Matej Možek: Ni pripomb.....	22
-- **** STUDENT: 64210132.....	25
-- KOMENTARJI K OCENI NALOGE -- Matej Možek: Ni pripomb.....	25
-- **** STUDENT: 64210290.....	28
-- KOMENTARJI K OCENI NALOGE -- Matej Možek: Ni pripomb.....	28
-- **** STUDENT: 64210382.....	31
-- KOMENTARJI K OCENI NALOGE -- Matej Možek: Ni pripomb.....	31
-- **** STUDENT: 64210384.....	34
-- KOMENTARJI K OCENI NALOGE -- Matej Možek: Ni pripomb.....	34
-- **** STUDENT: 64210386.....	38
-- KOMENTARJI K OCENI NALOGE -- Matej Možek: Ni pripomb.....	38
-- **** STUDENT: 64210455.....	43
-- KOMENTARJI K OCENI NALOGE -- Matej Možek: Ni pripomb.....	43
-- **** STUDENT: 64210457.....	46
-- KOMENTARJI K OCENI NALOGE -- Matej Možek: Ni pripomb.....	46
-- **** STUDENT: 64240430.....	49
-- KOMENTARJI K OCENI NALOGE -- Matej Možek: Ni pripomb.....	49

```
-- *****
-- **** STUDENT: 64000225
-- *****
-- KOMENTARJI K OCENI NALOGE
-- Matej Možek: Ni pripomb
-- *****
```

```
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;
```

```
-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
-- USE ieee.numeric_std.ALL;
```

```
ENTITY tff_tb IS
END tff_tb;
```

```
ARCHITECTURE behavior OF tff_tb IS
```

```
    -- Component Declaration for the Unit Under Test ( UUT )
```

```
    COMPONENT tff
    PORT(
        T : IN std_logic;
        clk : IN std_logic;
        nPRESET : IN std_logic;
        nCLEAR : IN std_logic;
        Q : OUT std_logic
    );
    END COMPONENT;
```

```
    -- Inputs
```

```
    signal      T : std_logic := '0';
    signal      clk : std_logic := '0';
    signal      nPRESET : std_logic := '1';
    signal      nCLEAR : std_logic := '1';
```

```
    -- Outputs
```

```
    signal      Q : std_logic;
```

```

    -- Clock period definitions
    constant    clk_period : time := 10 ns;

BEGIN

    -- Instantiate the Unit Under Test ( UUT )
    uut: tff PORT MAP (
    T => T,
    clk => clk,
    nPRESET => nPRESET,
    nCLEAR => nCLEAR,
    Q => Q
    );

    -- Clock process definitions
    clk_process :process
    begin
        clk    <= '0';
        wait for clk_period/2;
        clk    <= '1';
        wait for clk_period/2;
    end process;

    -- Stimulus process
    stim_proc: process
    begin
        -- hold reset state for 100 ns.
        wait for 100 ns;

        wait for clk_period*10;

        T    <= '1';
        wait for clk_period*4;
        T    <= '0';
        wait for clk_period*4;
        T    <= '1';
        wait for clk_period/5;
        nPRESET    <= '0';
        wait for clk_period*4;
    end process;

```

```
nPRESET      <= '1';  
wait for clk_period*4;  
nCLEAR <= '0';  
wait for clk_period*4;  
nCLEAR <= '1';
```

```
wait;  
end process;
```

```
END;
```

```

-- *****
-- **** STUDENT: 64200100
-- *****
-- KOMENTARJI K OCENI NALOGE
-- Matej Možek: Ni pripomb
-- *****
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;

ENTITY tff_tb IS
END tff_tb;

ARCHITECTURE behavior OF tff_tb IS

    COMPONENT tff
    PORT(
T : IN std_logic;
clk : IN std_logic;
nPRESET : IN std_logic;
nCLEAR : IN std_logic;
Q : OUT std_logic );
END COMPONENT;

signal      T : std_logic := '0';
signal      clk : std_logic := '0';
signal      nPRESET : std_logic := '1';
signal      nCLEAR : std_logic := '1';
signal      Q : std_logic;
constant    clkP : time := 10 ns;

BEGIN
uut: tff PORT MAP (
T => T,
clk => clk,
nPRESET => nPRESET,
nCLEAR => nCLEAR,
Q => Q );

clk_process :process
begin

```

```
clk    <= '0';
wait for clkP/2;
clk    <= '1';
wait for clkP/2;
end process;

sproc: process
begin
wait for 100 ns;
wait for clkP*10;
T      <= '1';
wait for clkP*4;
T      <= '0';
wait for clkP*4;
T      <= '1';
wait for clkP/5;
nPRESET <= '0';
wait for clkP*4;
nPRESET <= '1';
wait for clkP*4;
nCLEAR <= '0';
wait for clkP*4;
nCLEAR <= '1';
wait;
end process;
END;
```

```

-- *****
-- **** STUDENT: 64200163
-- *****
-- KOMENTARJI K OCENI NALOGE
-- Matej Možek: Ni pripomb
-- *****
library ieee;
use ieee.std_logic_1164.all;

entity tff_tb is
end tff_tb;

architecture behavior of tff_tb is
    component tff
        port(
            T : in std_logic;
            clk : in std_logic;
            nPRESET : in std_logic;
            nCLEAR : in std_logic;
            Q : out std_logic
        );
    end component;
    signal T : std_logic := '0';
    signal clk : std_logic := '0';
    signal nPRESET : std_logic := '1';
    signal nCLEAR : std_logic := '1';
    signal Q : std_logic;
    constant clk_period : time := 10 ns;
begin
    uut: tff port map(
        T => T,
        clk => clk,
        nPRESET => nPRESET,
        nCLEAR => nCLEAR,
        Q => Q
    );
    clk_process : process
    begin
        clk    <= '0';
        wait for clk_period/2;

```

```

        clk    <= '1';
        wait for clk_period/2;
end process;
stim_proc : process
begin
    wait for clk_period*2.2;
    T      <= '1';
    wait for clk_period*2;
    T      <= '0';
    wait for clk_period*2;
    nPRESET <= '0';
    wait for clk_period*2;
    nPRESET <= '1';
    wait for clk_period*2;
    T      <= '0';
    wait for clk_period*2;
    T      <= '1';
    wait for clk_period*2;
    nCLEAR <= '0';
    wait for clk_period*2.2;
    nCLEAR <= '1';

wait;
end process;
end;

```



```

-- *****
-- **** STUDENT: 64200238
-- *****
-- KOMENTARJI K OCENI NALOGE
-- Matej Možek: Ni pripomb
-- *****
--      --      --      --      --      --      --      --      --      --      --      --      --      --      --      --
--      --      --      --      --      --      --      --      --      --      --      --      --      --      --
--      --      --      --      --      --
-- Company:
-- Engineer:
--
-- Create Date: 18:24:25 12/22/2024
-- Design Name:
-- Module Name: C:/Users/Simon/Desktop/faks/NDS/5_domaca/LIFO/tff_tb.vhd
-- Project Name: LIFO
-- Target Device:
-- Tool versions:
-- Description:
--
-- VHDL Test Bench Created by ISE for module: tff
--
-- Dependencies:
--
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
--
-- Notes:
-- This testbench has been automatically generated using types std_logic and
-- std_logic_vector for the ports of the unit under test. Xilinx recommends
-- that these types always be used for the top-level I/O of a design in order
-- to guarantee that the testbench will bind correctly to the post-implementation
-- simulation model.
--      --      --      --      --      --      --      --      --      --      --      --      --      --      --      --
--      --      --      --      --      --      --      --      --      --      --      --      --      --      --
--      --      --      --      --      --
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;

```

```
-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
-- USE ieee.numeric_std.ALL;
```

```
ENTITY tff_tb IS
END tff_tb;
```

```
ARCHITECTURE behavior OF tff_tb IS
```

```
    -- Component Declaration for the Unit Under Test ( UUT )
```

```
    COMPONENT tff
    PORT(
        T : IN std_logic;
        clk : IN std_logic;
        nPRESET : IN std_logic;
        nCLEAR : IN std_logic;
        Q : OUT std_logic
    );
    END COMPONENT;
```

```
    -- Inputs
```

```
    signal          T : std_logic := '0';
    signal          clk : std_logic := '0';
    signal          nPRESET : std_logic := '0';
    signal          nCLEAR : std_logic := '0';
```

```
    -- Outputs
```

```
    signal          Q : std_logic;
```

```
    -- Clock period definitions
```

```
    constant        clk_period : time := 10 ns;
```

```
BEGIN
```

```
    -- Instantiate the Unit Under Test ( UUT )
```

```
    uut: tff PORT MAP (
        T => T,
        clk => clk,
        nPRESET => nPRESET,
```

```

nCLEAR => nCLEAR,
Q => Q
);

    -- Clock process definitions
clk_process :process
begin
    clk    <= '0';
    wait for clk_period/2;
    clk    <= '1';
    wait for clk_period/2;
end process;

    -- Stimulus process
stim_proc: process
begin
    -- hold reset state for 100 ns.
    wait for 100 ns;

    -- Test 1: Clear
    nCLEAR    <= '0'; WAIT FOR 20 ns;
    nCLEAR    <= '1'; WAIT FOR 20 ns;

    -- Test 2: Preset
    nPRESET    <= '0'; WAIT FOR 20 ns;
    nPRESET    <= '1'; WAIT FOR 20 ns;

    -- Test 3: T = '0'
    T    <= '0'; WAIT FOR 20 ns;

    -- Test 4: T = '1'
    T    <= '1'; WAIT FOR 40 ns;
    T    <= '0'; WAIT FOR 40 ns;

    -- Test 5: Toggle with preset/clear
    T    <= '1'; WAIT FOR 20 ns;
    nPRESET    <= '0'; WAIT FOR 20 ns;
    nPRESET    <= '1'; WAIT FOR 20 ns;
    nCLEAR    <= '0'; WAIT FOR 20 ns;
    nCLEAR    <= '1'; WAIT FOR 20 ns;

```

```
-- insert stimulus here
```

```
wait;  
end process;
```

```
END;
```

```
-- *****
-- **** STUDENT: 64200288
-- *****
-- KOMENTARJI K OCENI NALOGE
-- Matej Možek: Ni pripomb
-- *****
```

```
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;
```

```
ENTITY tff_tb IS
END tff_tb;
```

```
ARCHITECTURE behavior OF tff_tb IS
```

```
    COMPONENT tff
    PORT(
        T : IN std_logic;
        clk : IN std_logic;
        nPRESET : IN std_logic;
        nCLEAR : IN std_logic;
        Q : OUT std_logic
    );
    END COMPONENT;
```

```
    signal          T : std_logic := '0';
    signal          clk : std_logic := '0';
    signal          nPRESET : std_logic := '1';
    signal          nCLEAR : std_logic := '1';
    signal          Q : std_logic;
    constant        ClockPeriode : time := 10 ns;
```

```
BEGIN
    uut: tff PORT MAP (
        T => T,
        clk => clk,
        nPRESET => nPRESET,
        nCLEAR => nCLEAR,
        Q => Q
    );
```

```
s_proc : process
begin
clk  <= '0';
wait for ClockPeriode/2;
clk  <= '1';
wait for ClockPeriode/2;
end process;

sproc: process
begin
wait for 100 ns;
wait for ClockPeriode*10;
T    <= '1';
wait for ClockPeriode*5;
T    <= '0';
wait for ClockPeriode*5;
T    <= '1';
wait for ClockPeriode/5;
nPRESET    <= '0';
wait for ClockPeriode*5;
nPRESET    <= '1';
wait for ClockPeriode*5;
nCLEAR     <= '0';
wait for ClockPeriode*5;
nCLEAR     <= '1';
wait;
end process;

END;
```

```

-- *****
-- **** STUDENT: 64200296
-- *****
-- KOMENTARJI K OCENI NALOGE
-- Matej Možek: Ni pripomb
-- *****
--      --      --      --      --      --      --      --      --      --      --      --      --      --      --      --      --
--      --      --      --      --      --      --      --      --      --      --      --      --      --      --      --      --
--      --      --      --      --      --
-- Company:
-- Engineer:
--
-- Create Date: 12:35:36 12/22/2024
-- Design Name:
-- Module Name: C:/Users/Tim/Downloads/LIFO/LIFO/tff_tb.vhd
-- Project Name: LIFO
-- Target Device:
-- Tool versions:
-- Description:
--
-- VHDL Test Bench Created by ISE for module: tff
--
-- Dependencies:
--
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
--
-- Notes:
-- This testbench has been automatically generated using types std_logic and
-- std_logic_vector for the ports of the unit under test. Xilinx recommends
-- that these types always be used for the top-level I/O of a design in order
-- to guarantee that the testbench will bind correctly to the post-implementation
-- simulation model.
--      --      --      --      --      --      --      --      --      --      --      --      --      --      --      --      --
--      --      --      --      --      --      --      --      --      --      --      --      --      --      --      --      --
--      --      --      --      --      --
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;

```

```
-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
-- USE ieee.numeric_std.ALL;
```

```
ENTITY tff_tb IS
END tff_tb;
```

```
ARCHITECTURE behavior OF tff_tb IS
```

```
    -- Component Declaration for the Unit Under Test ( UUT )
```

```
    COMPONENT tff
    PORT(
        T : IN std_logic;
        clk : IN std_logic;
        nPRESET : IN std_logic;
        nCLEAR : IN std_logic;
        Q : OUT std_logic
    );
    END COMPONENT;
```

```
    -- Inputs
```

```
    signal          T : std_logic := '0';
    signal          clk : std_logic := '0';
    signal          nPRESET : std_logic := '1';
    signal          nCLEAR : std_logic := '1';
```

```
    -- Outputs
```

```
    signal          Q : std_logic;
```

```
    -- Clock period definitions
```

```
    constant        clk_period : time := 10 ns;
```

```
BEGIN
```

```
    -- Instantiate the Unit Under Test ( UUT )
```

```
    uut: tff PORT MAP (
        T => T,
        clk => clk,
        nPRESET => nPRESET,
```



```

nCLEAR => nCLEAR,
Q => Q
);

    -- Clock process definitions
clk_process :process
begin
    clk    <= '0';
    wait for clk_period/2;
    clk    <= '1';
    wait for clk_period/2;
end process;

    -- Stimulus process
stim_proc: process
begin
    -- hold reset state for 100 ns.
    wait for 100 ns;

    wait for clk_period*10;

    -- insert stimulus here

    T      <= '1';
    wait for clk_period*3;
    T      <= '0';
    wait for clk_period;
    T      <= '1';
    wait for clk_period;
    nPRESET <= '0';
    wait for clk_period;
    nPRESET <= '1';
    wait for clk_period;
    nCLEAR <= '0';
    wait for clk_period;
    nCLEAR <= '1';

wait;
end process;

```

END;

```

-- *****
-- **** STUDENT: 64200385
-- *****
-- KOMENTARJI K OCENI NALOGE
-- Matej Možek: Ni pripomb
-- *****
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
-- USE ieee.numeric_std.ALL;

ENTITY tff_tb IS
END tff_tb;

ARCHITECTURE behavior OF tff_tb IS

    -- Component Declaration for the Unit Under Test ( UUT )

    COMPONENT tff
    PORT(
        T : IN std_logic;
        clk : IN std_logic;
        nPRESET : IN std_logic;
        nCLEAR : IN std_logic;
        Q : OUT std_logic
    );
    END COMPONENT;

    -- Inputs
    signal      T : std_logic := '0';
    signal      clk : std_logic := '0';
    signal      nPRESET : std_logic := '0';
    signal      nCLEAR : std_logic := '0';

    -- Outputs
    signal      Q : std_logic;

    -- Clock period definitions

```

```

constant    clk_period : time := 10 ns;

BEGIN

    -- Instantiate the Unit Under Test ( UUT )
    uut: tff PORT MAP (
    T => T,
    clk => clk,
    nPRESET => nPRESET,
    nCLEAR => nCLEAR,
    Q => Q
    );

    -- Clock process definitions
    clk_process :process
    begin
        clk    <= '0';
        wait for clk_period/2;
        clk    <= '1';
        wait for clk_period/2;
    end process;

    -- Stimulus process
    stim_proc: process
    begin
        -- hold reset state for 100 ns.
        wait for 100 ns;

        wait for clk_period*10;

        -- insert stimulus here
        nCLEAR <= '1';
        nPRESET    <= '1';
        T    <= '1';
        wait for clk_period;
        T    <= '0';
        wait for clk_period;
        T    <= '1';
        wait for clk_period;
        nPRESET    <= '0';
    end process;

```

```
wait for clk_period;  
nPRESET    <= '1';  
wait for clk_period;  
nCLEAR <= '0';  
wait for clk_period;  
nCLEAR <= '1';  
wait for clk_period;
```

```
wait;  
end process;
```

```
END;
```

```

-- *****
-- **** STUDENT: 64210113
-- *****
-- KOMENTARJI K OCENI NALOGE
-- Matej Možek: Ni pripomb
-- *****

```

```

LIBRARY ieee;
USE ieee.std_logic_1164.ALL;
-- USE ieee.numeric_std.ALL;

```

```

ENTITY tff_tb IS
END tff_tb;

```

```

ARCHITECTURE behavior OF tff_tb IS

```

```

    -- Component Declaration for the Unit Under Test ( UUT )

```

```

COMPONENT tff
PORT(
T : IN std_logic;
clk : IN std_logic;
nPRESET : IN std_logic;
nCLEAR : IN std_logic;
Q : OUT std_logic
);
END COMPONENT;

```

```

    -- Inputs

```

```

signal      T : std_logic := '0';
signal      clk : std_logic := '0';
signal      nPRESET : std_logic := '1';
signal      nCLEAR : std_logic := '1';

```

```

    -- Outputs

```

```

signal      Q : std_logic;

```

```

    -- Clock period definitions

```

```

constant    clk_period : time := 10 ns;

```

```
BEGIN
```

```
    -- Instantiate the Unit Under Test ( UUT )
```

```
    uut: tff PORT MAP (  
        T => T,  
        clk => clk,  
        nPRESET => nPRESET,  
        nCLEAR => nCLEAR,  
        Q => Q  
    );
```

```
    -- Clock process definitions
```

```
    clk_process :process  
    begin  
        clk    <= '0';  
        wait for clk_period/2;  
        clk    <= '1';  
        wait for clk_period/2;  
    end process;
```

```
    -- Stimulus process
```

```
    stim_proc: process  
    begin  
        -- hold reset state for 100 ns.  
        wait for 100 ns;  
  
        wait for clk_period*10;
```

```
    -- insert stimulus here
```

```
        T    <= '1';  
        wait for 50ns;
```

```
        T    <= '0';  
        wait for 50ns;
```

```
        T    <= '1';  
        wait for 2ns;
```

```
        T    <= '0';
```

```
wait for 50ns;
```

```
T      <= '1';  
wait for 2ns;
```

```
nPRESET <= '0';  
wait for 50ns;
```

```
nPRESET <= '1';  
wait for 50ns;
```

```
nCLEAR <= '0';  
wait for 50ns;
```

```
nCLEAR <= '1';
```

```
wait;  
end process;
```

```
END;
```



```
-- *****
-- **** STUDENT: 64210132
-- *****
-- KOMENTARJI K OCENI NALOGE
-- Matej Možek: Ni pripomb
-- *****
```

```
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;
```

```
USE ieee.numeric_std.ALL;
```

```
ENTITY tff_tb IS
END tff_tb;
```

```
ARCHITECTURE behavior OF tff_tb IS
```

```
    COMPONENT tff
    PORT(
        T : IN std_logic;
        clk : IN std_logic;
        nPRESET : IN std_logic;
        nCLEAR : IN std_logic;
        Q : OUT std_logic
    );
    END COMPONENT;
```

```
    signal          T : std_logic := '0';
    signal          clk : std_logic := '0';
    signal          nPRESET : std_logic := '1';
    signal          nCLEAR : std_logic := '1';
```

```
    -- Outputs
    signal          Q : std_logic;
```

```
    -- Clock period definitions
    constant        clk_period : time := 10 ns;
```

```
BEGIN
```

```
    -- Instantiate the Unit Under Test ( UUT )
```

```
uut: tff PORT MAP (  
  T => T,  
  clk => clk,  
  nPRESET => nPRESET,  
  nCLEAR => nCLEAR,  
  Q => Q  
);
```

```
    -- Clock process definitions
```

```
clk_process :process  
begin  
    clk    <= '0';  
    wait for clk_period/2;  
    clk    <= '1';  
    wait for clk_period/2;  
end process;
```

```
stim_proc: process  
begin  
wait for 100 ns;
```

```
wait for clk_period*10;
```

```
    T    <= '1';  
    wait for clk_period*3;
```

```
    T    <= '0';  
    wait for clk_period*3;
```

```
    T    <= '1';  
    wait for clk_period/3;
```

```
    nPRESET    <= '0';  
    wait for clk_period*3;
```

```
    nPRESET    <= '1';  
    wait for clk_period*3;
```

```
    nCLEAR <= '0';
```

```
wait for clk_period*3;
```

```
nCLEAR <= '1';
```

```
wait;
```

```
end process;
```

```
END;
```

```

-- *****
-- **** STUDENT: 64210290
-- *****
-- KOMENTARJI K OCENI NALOGE
-- Matej Možek: Ni pripomb
-- *****
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;
USE ieee.numeric_std.ALL;

ENTITY tff_tb IS
END tff_tb;

ARCHITECTURE behavior OF tff_tb IS

    -- Component Declaration for the Unit Under Test ( UUT )

    COMPONENT tff
    PORT(
        T : IN std_logic;
        clk : IN std_logic;
        nPRESET : IN std_logic;
        nCLEAR : IN std_logic;
        Q : OUT std_logic
    );
    END COMPONENT;

    -- Inputs
    signal          T : std_logic := '0';
    signal          clk : std_logic := '0';
    signal          nPRESET : std_logic := '0';
    signal          nCLEAR : std_logic := '0';

    -- Outputs
    signal          Q : std_logic;

    -- Clock period definitions
    constant        clk_period : time := 10 ns;

BEGIN

```

```
    -- Instantiate the Unit Under Test ( UUT )
```

```
uut: tff PORT MAP (  
  T => T,  
  clk => clk,  
  nPRESET => nPRESET,  
  nCLEAR => nCLEAR,  
  Q => Q  
);
```

```
    -- Clock process definitions
```

```
clk_process :process  
begin  
    clk    <= '0';  
    wait for clk_period/2;  
    clk    <= '1';  
    wait for clk_period/2;  
end process;
```

```
    -- Stimulus process
```

```
stim_proc: process  
begin  
    -- hold reset state for 100 ns.  
    wait for 100 ns;  
  
    wait for clk_period*10;
```

```
    nCLEAR    <= '1';  
    nPRESET    <= '1';  
    T    <= '0';  
    wait for clk_period*5;  
  
    T    <= '1';  
    wait for clk_period*5;  
  
    wait until Q = '1';  
    wait for clk_period/2;  
    nCLEAR <= '0';  
    wait for clk_period/2;  
    wait for clk_period*2;
```

```
T      <= '1';  
wait for clk_period*5;  
nCLEAR <= '1';  
wait until Q = '0';
```

```
T      <= '0';  
wait for clk_period/2;  
nPRESET <= '0';  
wait for clk_period/2;  
wait for clk_period*2;  
T      <= '1';  
wait for clk_period*5;  
nPRESET <= '1';
```

```
wait;  
end process;
```

```
END;
```

```
-- *****
-- **** STUDENT: 64210382
-- *****
-- KOMENTARJI K OCENI NALOGE
-- Matej Možek: Ni pripomb
-- *****
```

```
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;
```

```
USE ieee.numeric_std.ALL;
```

```
ENTITY tff_tb IS
END tff_tb;
```

```
ARCHITECTURE behavior OF tff_tb IS
```

```
    COMPONENT tff
    PORT(
        T : IN std_logic;
        clk : IN std_logic;
        nPRESET : IN std_logic;
        nCLEAR : IN std_logic;
        Q : OUT std_logic
    );
    END COMPONENT;
```

```
    signal          T : std_logic := '0';
    signal          clk : std_logic := '0';
    signal          nPRESET : std_logic := '1';
    signal          nCLEAR : std_logic := '1';
```

```
    -- Outputs
    signal          Q : std_logic;
```

```
    -- Clock period definitions
    constant        clk_period : time := 10 ns;
```

```
BEGIN
```

```
    -- Instantiate the Unit Under Test ( UUT )
```

```
uut: tff PORT MAP (  
  T => T,  
  clk => clk,  
  nPRESET => nPRESET,  
  nCLEAR => nCLEAR,  
  Q => Q  
);
```

```
    -- Clock process definitions
```

```
clk_process :process  
begin  
    clk    <= '0';  
    wait for clk_period/2;  
    clk    <= '1';  
    wait for clk_period/2;  
end process;
```

```
stim_proc: process  
begin  
  wait for 100 ns;
```

```
  wait for clk_period*10;  
  
    T      <= '1';  
    wait for clk_period*4;  
    T      <= '0';  
    wait for clk_period*4;  
    T      <= '1';  
    wait for clk_period/5;  
    nPRESET <= '0';  
    wait for clk_period*4;  
    nPRESET <= '1';  
    wait for clk_period*4;  
    nCLEAR <= '0';  
    wait for clk_period*4;  
    nCLEAR <= '1';
```

```
wait;  
end process;
```


END;

```

-- *****
-- **** STUDENT: 64210384
-- *****
-- KOMENTARJI K OCENI NALOGE
-- Matej Možek: Ni pripomb
-- *****
--      --      --      --      --      --      --      --      --      --      --      --      --      --      --      --
--      --      --      --      --      --      --      --      --      --      --      --      --      --      --
--      --      --      --      --      --
-- Company:
-- Engineer:
--
-- Create Date: 01:48:51 12/20/2024
-- Design Name:
-- Module Name: C:/NDV/DN5/tff_tb.vhd
-- Project Name: DN5
-- Target Device:
-- Tool versions:
-- Description:
--
-- VHDL Test Bench Created by ISE for module: tff
--
-- Dependencies:
--
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
--
-- Notes:
-- This testbench has been automatically generated using types std_logic and
-- std_logic_vector for the ports of the unit under test. Xilinx recommends
-- that these types always be used for the top-level I/O of a design in order
-- to guarantee that the testbench will bind correctly to the post-implementation
-- simulation model.
--      --      --      --      --      --      --      --      --      --      --      --      --      --      --      --
--      --      --      --      --      --      --      --      --      --      --      --      --      --      --
--      --      --      --      --      --
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;

```

```
-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
-- USE ieee.numeric_std.ALL;
```

```
ENTITY tff_tb IS
END tff_tb;
```

```
ARCHITECTURE behavior OF tff_tb IS
```

```
    -- Component Declaration for the Unit Under Test ( UUT )
```

```
    COMPONENT tff
    PORT(
        T : IN std_logic;
        clk : IN std_logic;
        nPRESET : IN std_logic;
        nCLEAR : IN std_logic;
        Q : OUT std_logic
    );
    END COMPONENT;
```

```
    -- Inputs
```

```
    signal      T : std_logic := '0';
    signal      clk : std_logic := '0';
    signal      nPRESET : std_logic := '1';
    signal      nCLEAR : std_logic := '1';
```

```
    -- Outputs
```

```
    signal      Q : std_logic;
```

```
    -- Clock period definitions
```

```
    constant    clk_period : time := 40 ns;
```

```
BEGIN
```

```
    -- Instantiate the Unit Under Test ( UUT )
```

```
    uut: tff PORT MAP (
        T => T,
        clk => clk,
        nPRESET => nPRESET,
```

```

nCLEAR => nCLEAR,
Q => Q
);

    -- Clock process definitions
clk_process :process
begin
    clk    <= '0';
    wait for clk_period/2;
    clk    <= '1';
    wait for clk_period/2;
end process;

    -- Stimulus process
stim_proc: process
begin
    -- hold reset state for 100 ns.
    wait for 100 ns;

    -- insert stimulus here
    nPRESET    <= '0';
    wait for clk_period/2;
    nPRESET    <= '1';

    T    <= '1';
    wait for clk_period/4;
    T    <= '0';
    wait for clk_period/4;
    T    <= '1';
    wait for clk_period/4;
    T    <= '0';
    wait for clk_period/4;

    nCLEAR <= '0';
    wait for clk_period/2;
    nCLEAR <= '1';

    T    <= '1';
    wait for clk_period/4;
    T    <= '0';

```

```
wait for clk_period/4;  
T      <= '1';  
wait for clk_period/4;  
T      <= '0';  
wait for clk_period/4;
```

```
nCLEAR <= '0';  
wait for clk_period/2;
```

```
T      <= '1';  
wait for clk_period/4;  
T      <= '0';  
wait for clk_period/4;  
T      <= '1';  
wait for clk_period/4;  
T      <= '0';  
wait for clk_period/4;
```

```
nPRESET <= '0';  
wait for clk_period/2;
```

```
wait for clk_period/4;  
T      <= '0';  
wait for clk_period/4;  
T      <= '1';  
wait for clk_period/4;  
T      <= '0';  
wait for clk_period/4;
```

```
wait;  
end process;
```

```
END;
```

```

-- *****
-- **** STUDENT: 64210386
-- *****
-- KOMENTARJI K OCENI NALOGE
-- Matej Možek: Ni pripomb
-- *****
--      --      --      --      --      --      --      --      --      --      --      --      --      --      --      --      --
--      --      --      --      --      --      --      --      --      --      --      --      --      --      --      --      --
--      --      --      --      --      --
-- Company:
-- Engineer:
--
-- Create Date: 16:30:24 12/20/2024
-- Design Name:
-- Module Name: /home/ise/Xilinx_shared/domaca_naloga_5/tff_tb.vhd
-- Project Name: domaca_naloga_5
-- Target Device:
-- Tool versions:
-- Description:
--
-- VHDL Test Bench Created by ISE for module: tff
--
-- Dependencies:
--
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
--
-- Notes:
-- This testbench has been automatically generated using types std_logic and
-- std_logic_vector for the ports of the unit under test. Xilinx recommends
-- that these types always be used for the top-level I/O of a design in order
-- to guarantee that the testbench will bind correctly to the post-implementation
-- simulation model.
--      --      --      --      --      --      --      --      --      --      --      --      --      --      --      --      --
--      --      --      --      --      --      --      --      --      --      --      --      --      --      --      --      --
--      --      --      --      --      --
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;

```

```
-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
-- USE ieee.numeric_std.ALL;
```

```
ENTITY tff_tb IS
END tff_tb;
```

```
ARCHITECTURE behavior OF tff_tb IS
```

```
    -- Component Declaration for the Unit Under Test ( UUT )
```

```
    COMPONENT tff
    PORT(
        T : IN std_logic;
        clk : IN std_logic;
        nPRESET : IN std_logic;
        nCLEAR : IN std_logic;
        Q : OUT std_logic
    );
    END COMPONENT;
```

```
    -- Inputs
```

```
    signal          T : std_logic := '0';
    signal          clk : std_logic := '0';
    signal          nPRESET : std_logic := '1';
    signal          nCLEAR : std_logic := '1';
```

```
    -- Outputs
```

```
    signal          Q : std_logic;
```

```
    -- Clock period definitions
```

```
    constant        clk_period : time := 10 ns;
```

```
BEGIN
```

```
    -- Instantiate the Unit Under Test ( UUT )
```

```
    uut: tff PORT MAP (
        T => T,
        clk => clk,
        nPRESET => nPRESET,
```

```

nCLEAR => nCLEAR,
Q => Q
);

    -- Clock process definitions
clk_process :process
begin
    clk    <= '0';
    wait for clk_period/2;
    clk    <= '1';
    wait for clk_period/2;
end process;

    -- Stimulus process
stim_proc: process
begin
    -- hold reset state for 100 ns.
    wait for 100 ns;

    wait for clk_period*10;

    -- insert stimulus here
    T      <= '1';
    wait for clk_period*4;
    T      <= '0';
    wait for clk_period*4;
    T      <= '1';
    wait for clk_period/5;
    nPRESET <= '0';
    wait for clk_period*4;
    nPRESET <= '1';
    wait for clk_period*4;
    nCLEAR <= '0';
    wait for clk_period*4;
    nCLEAR <= '1';

    wait;
end process;

END;

```



```
-- *****
-- **** STUDENT: 64210445
-- *****
-- KOMENTARJI K OCENI NALOGE
-- Matej Možek: Ni pripomb
-- *****
```

```
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;
```

```
ENTITY tff_tb IS
END tff_tb;
```

```
ARCHITECTURE behavior OF tff_tb IS
```

```
    COMPONENT tff
    PORT(
        T : IN  std_logic;
        clk : IN  std_logic;
        nPRESET : IN  std_logic;
        nCLEAR : IN  std_logic;
        Q : OUT  std_logic
    );
END COMPONENT;
```

--Inputs

```
signal T : std_logic := '0';
signal clk : std_logic := '0';
signal nPRESET : std_logic := '0';
signal nCLEAR : std_logic := '0';
```

--Outputs

```
signal Q : std_logic;
```

-- Clock period definitions

```
constant clk_period : time := 10 ns;
```

```
BEGIN
```

```

    -- Instantiate the Unit Under Test (UUT)
    uut: tff PORT MAP (
        T => T,
        clk => clk,
        nPRESET => nPRESET,
        nCLEAR => nCLEAR,
        Q => Q
    );

    -- Clock process definitions
    clk_process :process
    begin
        clk <= '0';
        wait for clk_period/2;
        clk <= '1';
        wait for clk_period/2;
    end process;

    -- Stimulus process
    stim_proc: process
    begin
        wait for 100 ns;    -- hold reset state for 100 ns.
        nCLEAR <= '1';      wait for clk_period;
        T <= '1';           wait for clk_period;
        T <= '0';           wait for clk_period;
        T <= '1';           wait for clk_period;
        nPRESET <= '0';     wait for clk_period;
        nPRESET <= '1';     wait for clk_period;
        nCLEAR <= '0';      wait;
    end process;

END;

```

```

-- *****
-- **** STUDENT: 64210455
-- *****
-- KOMENTARJI K OCENI NALOGE
-- Matej Možek: Ni pripomb
-- *****
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
-- USE ieee.numeric_std.ALL;

ENTITY tff_tb IS
END tff_tb;

ARCHITECTURE behavior OF tff_tb IS

    -- Component Declaration for the Unit Under Test ( UUT )

    COMPONENT tff
    PORT(
        T : IN std_logic;
        clk : IN std_logic;
        nPRESET : IN std_logic;
        nCLEAR : IN std_logic;
        Q : OUT std_logic
    );
    END COMPONENT;

    -- Inputs
    signal      T : std_logic := '0';
    signal      clk : std_logic := '0';
    signal      nPRESET : std_logic := '1';
    signal      nCLEAR : std_logic := '1';

    -- Outputs
    signal      Q : std_logic;

    -- Clock period definitions

```

```

constant    clk_period : time := 10 ns;

BEGIN

    -- Instantiate the Unit Under Test ( UUT )
    uut: tff PORT MAP (
    T => T,
    clk => clk,
    nPRESET => nPRESET,
    nCLEAR => nCLEAR,
    Q => Q
    );

    -- Clock process definitions
    clk_process :process
    begin
        clk    <= '0';
        wait for clk_period/2;
        clk    <= '1';
        wait for clk_period/2;
    end process;

    -- Stimulus process
    stim_proc: process
    begin
        -- hold reset state for 100 ns.
        wait for 100 ns;

        wait for clk_period*10;

        -- insert stimulus here
        T    <= '1';
        wait for clk_period*4;
        T    <= '0';
        wait for clk_period*4;
        T    <= '1';
        wait for clk_period/5;
        nPRESET    <= '0';
        wait for clk_period*4;
        nPRESET    <= '1';
    end process;

```

```
wait for clk_period*4;  
nCLEAR <= '0';  
wait for clk_period*4;  
nCLEAR <= '1';
```

```
wait;  
end process;
```

```
END;
```

```

-- *****
-- **** STUDENT: 64210457
-- *****
-- KOMENTARJI K OCENI NALOGE
-- Matej Možek: Ni pripomb
-- *****
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
-- USE ieee.numeric_std.ALL;

ENTITY tff_tb IS
END tff_tb;

ARCHITECTURE behavior OF tff_tb IS

    -- Component Declaration for the Unit Under Test ( UUT )

    COMPONENT tff
    PORT(
        T : IN std_logic;
        clk : IN std_logic;
        nPRESET : IN std_logic;
        nCLEAR : IN std_logic;
        Q : OUT std_logic
    );
    END COMPONENT;

    -- Inputs
    signal      T : std_logic := '0';
    signal      clk : std_logic := '0';
    signal      nPRESET : std_logic := '1';
    signal      nCLEAR : std_logic := '1';

    -- Outputs
    signal      Q : std_logic;

    -- Clock period definitions

```

```

constant    clk_period : time := 10 ns;

BEGIN

    -- Instantiate the Unit Under Test ( UUT )
    uut: tff PORT MAP (
    T => T,
    clk => clk,
    nPRESET => nPRESET,
    nCLEAR => nCLEAR,
    Q => Q
    );

    -- Clock process definitions
    clk_process :process
    begin
        clk    <= '0';
        wait for clk_period/2;
        clk    <= '1';
        wait for clk_period/2;
    end process;

    -- Stimulus process
    stim_proc: process
    begin
        -- hold reset state for 100 ns.
        wait for 100 ns;

        wait for clk_period*10;

        -- insert stimulus here
        T    <= '1';
        wait for clk_period*4;
        T    <= '0';
        wait for clk_period*4;
        T    <= '1';
        wait for clk_period/5;
        nPRESET    <= '0';
        wait for clk_period*4;
        nPRESET    <= '1';
    end process;

```

```
wait for clk_period*4;  
nCLEAR <= '0';  
wait for clk_period*4;  
nCLEAR <= '1';
```

```
wait;  
end process;
```

```
END;
```



```

-- *****
-- **** STUDENT: 64240430
-- *****
-- KOMENTARJI K OCENI NALOGE
-- Matej Možek: Ni pripomb
-- *****
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;

ENTITY tff_tb IS
END tff_tb;

ARCHITECTURE behavior OF tff_tb IS

    -- Component Declaration for the Unit Under Test ( UUT )

    COMPONENT tff
    PORT(
        T : IN std_logic;
        clk : IN std_logic;
        nPRESET : IN std_logic;
        nCLEAR : IN std_logic;
        Q : OUT std_logic
    );
    END COMPONENT;

    -- Inputs
    signal      T : std_logic := '0';
    signal      nPRESET : std_logic := '1';
    signal      nCLEAR : std_logic := '1';

    -- Outputs
    signal      Q : std_logic;

    -- Clock period definitions

    signal      clock : std_logic;
    constant    clock_period : time := 100 ns;

BEGIN

```

```

    -- Instantiate the Unit Under Test ( UUT )
uut: tff PORT MAP (
T => T,
clk => clock,
nPRESET => nPRESET,
nCLEAR => nCLEAR,
Q => Q
);

    -- Clock process definitions
clock_process :process
begin
    clock <= '0';
    wait for clock_period/2;
    clock <= '1';
    wait for clock_period/2;
end process;

    -- Stimulus process
stimulus_process: process
begin

    -- najprej se naredi reset nPRESET = 0
    -- izhod Q_sig = 1
        nPRESET <= '0';
        wait for clock_period/4;
    -- zdaj je nPRESET = 1
    -- Q_sig <= not Q_sig za rising_edge( clk ) and T = '1'
    -- ovaj deo dela
        nPRESET <= '1';
        T <= '1';
        wait for clock_period/2;
        T <= '0';
        wait for clock_period/2;
        T <= '1';
        wait for clock_period/2;
        T <= '0';
        wait for clock_period/2;

```

```
-- enako testiramo nCLEAR
  nCLEAR <= '0';
  wait for clock_period/6;
  nCLEAR <= '1';

  T      <= '1';
  wait for clock_period/2;
  T      <= '0';
  wait for clock_period/2;
  T      <= '1';
  wait for clock_period/2;
  T      <= '0';
  wait for clock_period/2;

  wait;
end process;

END;
```

