

[illegible]

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WARNING:HDLParasers:3353 - "C:/vhdl/NDV_DN/2024/05_LIFO/STUDENTI/64210290/dff.vhd" Line 55
WARNING:HDLParasers:3353 - "C:/vhdl/NDV_DN/2024/05_LIFO/STUDENTI/64210290/dff.vhd" Line 58
WARNING:HDLParasers:3353 - "C:/vhdl/NDV_DN/2024/05_LIFO/STUDENTI/64210290/dff.vhd" Line 61
ERROR:HDLParasers:168 - "C:/vhdl/NDV_DN/2024/05_LIFO/STUDENTI/64210290/dff.vhd" Line 631. N
WARNING:HDLParasers:3607 - Unit work/ud_counter is now defined in a different file. It was defined in
WARNING:HDLParasers:3607 - Unit work/tff is now defined in a different file. It was defined in "C:/vhdl/I
WARNING:HDLParasers:3607 - Unit work/ud_counter is now defined in a different file. It was defined in
WARNING:HDLParasers:3607 - Unit work/ud_counter/ideal is now defined in a different file. It was defin
WARNING:HDLParasers:3607 - Unit work/tff is now defined in a different file. It was defined in "C:/vhdl/I
WARNING:HDLParasers:3607 - Unit work/tff/ideal is now defined in a different file. It was defined in "C:/
WARNING:HDLParasers:3607 - Unit work/ud_counter is now defined in a different file. It was defined in
WARNING:HDLParasers:3607 - Unit work/ud_counter/ideal is now defined in a different file. It was defin
WARNING:HDLParasers:3607 - Unit work/tff is now defined in a different file. It was defined in "C:/vhdl/I
WARNING:HDLParasers:3607 - Unit work/tff/ideal is now defined in a different file. It was defined in "C:/
WARNING:HDLParasers:3607 - Unit work/ud_counter is now defined in a different file. It was defined in
WARNING:HDLParasers:3607 - Unit work/ud_counter/ideal is now defined in a different file. It was defin
WARNING:HDLParasers:3607 - Unit work/tff is now defined in a different file. It was defined in "C:/vhdl/I
WARNING:HDLParasers:3607 - Unit work/tff/ideal is now defined in a different file. It was defined in "C:/
WARNING:HDLParasers:3607 - Unit work/ud_counter is now defined in a different file. It was defined in
WARNING:HDLParasers:3607 - Unit work/ud_counter/ideal is now defined in a different file. It was defin
WARNING:HDLParasers:3607 - Unit work/tff is now defined in a different file. It was defined in "C:/vhdl/I
WARNING:HDLParasers:3607 - Unit work/tff/ideal is now defined in a different file. It was defined in "C:/

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ie 56. Primary unit muxdff is being redefined within the file. Prior definition (on line 5) is discarded. (LRM
ie 100. Primary unit muxdff is being redefined within the file. Prior definition (on line 56) is discarded. (LF
ie 144. Primary unit muxdff is being redefined within the file. Prior definition (on line 100) is discarded. (L
ie 188. Primary unit muxdff is being redefined within the file. Prior definition (on line 144) is discarded. (L
ie 232. Primary unit muxdff is being redefined within the file. Prior definition (on line 188) is discarded. (L
ie 276. Primary unit muxdff is being redefined within the file. Prior definition (on line 232) is discarded. (L
ie 320. Primary unit muxdff is being redefined within the file. Prior definition (on line 276) is discarded. (L
ie 364. Primary unit muxdff is being redefined within the file. Prior definition (on line 320) is discarded. (L
ie 408. Primary unit muxdff is being redefined within the file. Prior definition (on line 364) is discarded. (L
ie 452. Primary unit muxdff is being redefined within the file. Prior definition (on line 408) is discarded. (L
ie 496. Primary unit muxdff is being redefined within the file. Prior definition (on line 452) is discarded. (L
ie 540. Primary unit muxdff is being redefined within the file. Prior definition (on line 496) is discarded. (L
ie 584. Primary unit muxdff is being redefined within the file. Prior definition (on line 540) is discarded. (L
ie 628. Primary unit muxdff is being redefined within the file. Prior definition (on line 584) is discarded. (L
ie 672. Primary unit muxdff is being redefined within the file. Prior definition (on line 628) is discarded. (L
ie 716. Primary unit muxdff is being redefined within the file. Prior definition (on line 672) is discarded. (L
ie 760. Primary unit muxdff is being redefined within the file. Prior definition (on line 716) is discarded. (L
ie 804. Primary unit muxdff is being redefined within the file. Prior definition (on line 760) is discarded. (L
ie 848. Primary unit muxdff is being redefined within the file. Prior definition (on line 804) is discarded. (L
ie 892. Primary unit muxdff is being redefined within the file. Prior definition (on line 848) is discarded. (L
25. Non-graphic character (0x1a) is not allowed.

.line 86. Primary unit shift_reg is being redefined within the file. Prior definition (on line 4) is discarded. (L
.line 161. Primary unit shift_reg is being redefined within the file. Prior definition (on line 86) is discarded.
.line 236. Primary unit shift_reg is being redefined within the file. Prior definition (on line 161) is discardec
.line 311. Primary unit shift_reg is being redefined within the file. Prior definition (on line 236) is discardec
.line 386. Primary unit shift_reg is being redefined within the file. Prior definition (on line 311) is discardec
.line 461. Primary unit shift_reg is being redefined within the file. Prior definition (on line 386) is discardec
.line 536. Primary unit shift_reg is being redefined within the file. Prior definition (on line 461) is discardec
.line 611. Primary unit shift_reg is being redefined within the file. Prior definition (on line 536) is discardec
.line 686. Primary unit shift_reg is being redefined within the file. Prior definition (on line 611) is discardec
.line 761. Primary unit shift_reg is being redefined within the file. Prior definition (on line 686) is discardec
.line 836. Primary unit shift_reg is being redefined within the file. Prior definition (on line 761) is discardec
.line 911. Primary unit shift_reg is being redefined within the file. Prior definition (on line 836) is discardec
.line 986. Primary unit shift_reg is being redefined within the file. Prior definition (on line 911) is discardec
.line 1061. Primary unit shift_reg is being redefined within the file. Prior definition (on line 986) is discarde
.line 1136. Primary unit shift_reg is being redefined within the file. Prior definition (on line 1061) is discarc
.line 1211. Primary unit shift_reg is being redefined within the file. Prior definition (on line 1136) is discarc
.line 1286. Primary unit shift_reg is being redefined within the file. Prior definition (on line 1211) is discarc
.line 1361. Primary unit shift_reg is being redefined within the file. Prior definition (on line 1286) is discarc
.line 1436. Primary unit shift_reg is being redefined within the file. Prior definition (on line 1361) is discarc
.line 1511. Primary unit shift_reg is being redefined within the file. Prior definition (on line 1436) is discarc
1576. Non-graphic character (0x1a) is not allowed.

"C:/vhdl/NDV_DN/2024/05_LIFO/STUDENTI/64200163/ud_counter.vhd", and is now defined in "C:/vhdl/
ied in "C:/vhdl/NDV_DN/2024/05_LIFO/STUDENTI/64200163/ud_counter.vhd", and is now defined in "C
NDV_DN/2024/05_LIFO/STUDENTI/64200163/tff.vhd", and is now defined in "C:/vhdl/NDV_DN/2024/05
'vhdl/NDV_DN/2024/05_LIFO/STUDENTI/64200163/tff.vhd", and is now defined in "C:/vhdl/NDV_DN/20
Line 66. Choice OR is not a locally static expression.

"C:/vhdl/NDV_DN/2024/05_LIFO/STUDENTI/64200238/ud_counter.vhd", and is now defined in "C:/vhdl/
ied in "C:/vhdl/NDV_DN/2024/05_LIFO/STUDENTI/64200238/ud_counter.vhd", and is now defined in "C
NDV_DN/2024/05_LIFO/STUDENTI/64200238/tff.vhd", and is now defined in "C:/vhdl/NDV_DN/2024/05
'vhdl/NDV_DN/2024/05_LIFO/STUDENTI/64200238/tff.vhd", and is now defined in "C:/vhdl/NDV_DN/20
"C:/vhdl/NDV_DN/2024/05_LIFO/STUDENTI/64200288/ud_counter.vhd", and is now defined in "C:/vhd
ied in "C:/vhdl/NDV_DN/2024/05_LIFO/STUDENTI/64200288/ud_counter.vhd", and is now defined in "C
NDV_DN/2024/05_LIFO/STUDENTI/64200288/tff.vhd", and is now defined in "C:/vhdl/NDV_DN/2024/05
'vhdl/NDV_DN/2024/05_LIFO/STUDENTI/64200288/tff.vhd", and is now defined in "C:/vhdl/NDV_DN/20
End Identifier improved does not match declaration, ideal.

"C:/vhdl/NDV_DN/2024/05_LIFO/STUDENTI/64200296/ud_counter.vhd", and is now defined in "C:/vhdl/
ied in "C:/vhdl/NDV_DN/2024/05_LIFO/STUDENTI/64200296/ud_counter.vhd", and is now defined in "C
NDV_DN/2024/05_LIFO/STUDENTI/64200296/tff.vhd", and is now defined in "C:/vhdl/NDV_DN/2024/05

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RM 11.1)
.RM 11.1
.RM 11.1
.RM 11.1
.RM 11.1
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.RM 11.1
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.RM 11.1
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.RM 11.1)
.RM 11.1)
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.RM 11.1)
.RM 11.1)
.RM 11.1)
.RM 11.1)
.RM 11.1)
```

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```
I/NDV_DN/2024/05_LIFO/STUDENTI/64210132/ud_counter_IDEAL.vhd".
;_LIFO/STUDENTI/64210132/tff_IDEAL.vhd".
```

```
I/NDV_DN/2024/05_LIFO/STUDENTI/64210290/ud_counter_IDEAL.vhd".
.:vhdI/NDV_DN/2024/05_LIFO/STUDENTI/64210290/ud_counter_IDEAL.vhd".
;_LIFO/STUDENTI/64210290/tff_IDEAL.vhd".
24/05_LIFO/STUDENTI/64210290/tff_IDEAL.vhd".
```

$$\begin{pmatrix}) \\) \\) \\) \\) \\) \\) \\) \\) \\) \\) \\) \end{pmatrix}$$

)
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)

I/NDV_DN/2024/05_LIFO/STUDENTI/64210382/ud_counter_IDEAL.vhd".
;_LIFO/STUDENTI/64210382/tff_IDEAL.vhd".
I/NDV_DN/2024/05_LIFO/STUDENTI/64210384/ud_counter_IDEAL.vhd".
:/vhdl/NDV_DN/2024/05_LIFO/STUDENTI/64210384/ud_counter_IDEAL.vhd".
;_LIFO/STUDENTI/64210384/tff_IDEAL.vhd".
24/05_LIFO/STUDENTI/64210384/tff_IDEAL.vhd".
I/NDV_DN/2024/05_LIFO/STUDENTI/64210386/ud_counter_IDEAL.vhd".
:/vhdl/NDV_DN/2024/05_LIFO/STUDENTI/64210386/ud_counter_IDEAL.vhd".
;_LIFO/STUDENTI/64210386/tff_IDEAL.vhd".
24/05_LIFO/STUDENTI/64210386/tff_IDEAL.vhd".
I/NDV_DN/2024/05_LIFO/STUDENTI/64210445/ud_counter_IDEAL.vhd".
:/vhdl/NDV_DN/2024/05_LIFO/STUDENTI/64210445/ud_counter_IDEAL.vhd".
;_LIFO/STUDENTI/64210445/tff_IDEAL.vhd".
24/05_LIFO/STUDENTI/64210445/tff_IDEAL.vhd".
I/NDV_DN/2024/05_LIFO/STUDENTI/64210455/ud_counter_IDEAL.vhd".
;_LIFO/STUDENTI/64210455/tff_IDEAL.vhd".
I/NDV_DN/2024/05_LIFO/STUDENTI/64210457/ud_counter_IDEAL.vhd".
;_LIFO/STUDENTI/64210457/tff_IDEAL.vhd".
I/NDV_DN/2024/05_LIFO/STUDENTI/64240430/ud_counter_IDEAL.vhd".
:/vhdl/NDV_DN/2024/05_LIFO/STUDENTI/64240430/ud_counter_IDEAL.vhd".
;_LIFO/STUDENTI/64240430/tff_IDEAL.vhd".
24/05_LIFO/STUDENTI/64240430/tff_IDEAL.vhd".
OV_DN/2024/05_LIFO/STUDENTI/IDEAL/ud_counter_IDEAL.vhd".
rdI/NDV_DN/2024/05_LIFO/STUDENTI/IDEAL/ud_counter_IDEAL.vhd".
FO/STUDENTI/IDEAL/tff_IDEAL.vhd".
05_LIFO/STUDENTI/IDEAL/tff_IDEAL.vhd".

[illegible]


```

IDEAL>xst -ifn ud_counter.xst
Release 14.7 - xst P.20131013 (nt64)
Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.
--> Parameter TMPDIR set to ./xst/projnav.tmp
Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.23 secs

--> WARNING:Xst:3164 - Option "-debug" found multiple times in the command line. Only the first occurrence
*          HDL Compilation          *
Compiling vhdl file "C:/vhdl/NDV_DN/2024/05_LIFO/STUDENTI/IDEAL/tff.vhd" in Library work.
Entity <tff> compiled.
Entity <tff> (Architecture <ideal>) compiled.
Compiling vhdl file "C:/vhdl/NDV_DN/2024/05_LIFO/STUDENTI/IDEAL/ud_counter.vhd" in Library work
Entity <ud_counter> compiled.
Entity <ud_counter> (Architecture <ideal>) compiled.
Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.30 secs

-->
Total memory usage is 4468928 kilobytes
Number of errors   : 0 ( 0 filtered)
Number of warnings : 1 ( 0 filtered)
Number of infos    : 0 ( 0 filtered)
IDEAL>fuse -incremental -o ud_counter_tb_isim_beh.exe -prj ud_counter_tb.prj -top ud_counter_IDEAL
ISim P.20131013 (signature 0x7708f090)
Number of CPUs detected in this system: 8
Turning on mult-threading, number of parallel sub-compilation jobs: 16
Determining compilation order of HDL files
Parsing VHDL file "tff.vhd" into library work
Parsing VHDL file "ud_counter.vhd" into library work
Parsing VHDL file "ud_counter_IDEAL_tb.vhd" into library work
Starting static elaboration
Completed static elaboration
Compiling package standard
Compiling package std_logic_1164
Compiling package numeric_std
Compiling package textio
Compiling package std_logic_textio
Compiling architecture ideal of entity tff [tff_default]
Compiling architecture ideal of entity ud_counter [ud_counter(3)]
Compiling architecture ideal of entity ud_counter_ideal_tb
Time Resolution for simulation is 1ps.
Waiting for 1 sub-compilation(s) to finish...
Compiled 10 VHDL Units
Built simulation executable ud_counter_tb_isim_beh.exe
Fuse Memory Usage: 36920 KB
Fuse CPU Usage: 858 ms
IDEAL>ud_counter_tb_isim_beh.exe -tclbatch isim_ud_ctr.tcl -wdb ud_counter_tb_isim_beh.wdb
ISim P.20131013 (signature 0x7708f090)
WARNING: A WEBPACK license was found.
WARNING: Please use Xilinx License Configuration Manager to check out a full ISim license.
WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for more information on t
This is a Lite version of ISim.
Time resolution is 1 ps
Simulator is doing circuit initialization process.
Finished circuit initialization process.
IDEAL>xst -ifn lifo.xst
Release 14.7 - xst P.20131013 (nt64)

```

Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.

--> Parameter TMPDIR set to ./xst/projnav.tmp

Total REAL time to Xst completion: 0.00 secs

Total CPU time to Xst completion: 0.27 secs

--> WARNING:Xst:3164 - Option "-debug" found multiple times in the command line. Only the first occurrence is used.

* HDL Compilation *

WARNING:HDLParasers:3607 - Unit work/ud_counter is now defined in a different file. It was defined in

WARNING:HDLParasers:3607 - Unit work/ud_counter/ideal is now defined in a different file. It was defined in

WARNING:HDLParasers:3607 - Unit work/tff is now defined in a different file. It was defined in "C:/vhd/

WARNING:HDLParasers:3607 - Unit work/tff/ideal is now defined in a different file. It was defined in "C:/

Compiling vhd file "C:/vhd/NDV_DN/2024/05_LIFO/STUDENTI/IDEAL/muxnto1.vhd" in Library work.

Entity <muxnto1> compiled.

Entity <muxnto1> (Architecture <ideal>) compiled.

Compiling vhd file "C:/vhd/NDV_DN/2024/05_LIFO/STUDENTI/IDEAL/dff.vhd" in Library work.

Entity <dff> compiled.

Entity <dff> (Architecture <ideal>) compiled.

Compiling vhd file "C:/vhd/NDV_DN/2024/05_LIFO/STUDENTI/IDEAL/tff_IDEAL.vhd" in Library work.

Architecture ideal of Entity tff is up to date.

Compiling vhd file "C:/vhd/NDV_DN/2024/05_LIFO/STUDENTI/IDEAL/muxdff.vhd" in Library work.

Entity <muxdff> compiled.

Entity <muxdff> (Architecture <ideal>) compiled.

Compiling vhd file "C:/vhd/NDV_DN/2024/05_LIFO/STUDENTI/IDEAL/shift_reg.vhd" in Library work.

Entity <shift_reg> compiled.

Entity <shift_reg> (Architecture <ideal>) compiled.

Compiling vhd file "C:/vhd/NDV_DN/2024/05_LIFO/STUDENTI/IDEAL/ud_counter_IDEAL.vhd" in Library work.

Architecture ideal of Entity ud_counter is up to date.

Compiling vhd file "C:/vhd/NDV_DN/2024/05_LIFO/STUDENTI/IDEAL/lifo.vhd" in Library work.

Entity <lifo> compiled.

Entity <lifo> (Architecture <ideal>) compiled.

Total REAL time to Xst completion: 0.00 secs

Total CPU time to Xst completion: 0.41 secs

-->

Total memory usage is 4477180 kilobytes

Number of errors : 0 (0 filtered)

Number of warnings : 5 (0 filtered)

Number of infos : 0 (0 filtered)

IDEAL>fuse -incremental -o lifo_tb_isim_beh.exe -prj lifo_tb.prj -top lifo_IDEAL_tb

ISim P.20131013 (signature 0x7708f090)

Number of CPUs detected in this system: 8

Turning on mult-threading, number of parallel sub-compilation jobs: 16

Determining compilation order of HDL files

Parsing VHDL file "dff.vhd" into library work

Parsing VHDL file "tff_IDEAL.vhd" into library work

Parsing VHDL file "muxnto1.vhd" into library work

Parsing VHDL file "muxdff.vhd" into library work

Parsing VHDL file "shift_reg.vhd" into library work

Parsing VHDL file "ud_counter_IDEAL.vhd" into library work

Parsing VHDL file "lifo.vhd" into library work

Parsing VHDL file "lifo_IDEAL_tb.vhd" into library work

Starting static elaboration

Completed static elaboration

Compiling package standard

Compiling package std_logic_1164

Compiling package numeric_std

Compiling package textio

Compiling package std_logic_textio

Compiling package math_real

Compiling architecture ideal of entity muxnto1 [\muxnto1(2)\]
Compiling architecture ideal of entity dff [dff_default]
Compiling architecture ideal of entity muxdff [\muxdff(2)\]
Compiling architecture ideal of entity shift_reg [\shift_reg(11)\]
Compiling architecture ideal of entity tff [tff_default]
Compiling architecture ideal of entity ud_counter [\ud_counter(4)\]
Compiling architecture ideal of entity lifo [\lifo(8,11)\]
Compiling architecture ideal of entity lifo_ideal_tb
Time Resolution for simulation is 1ps.
Waiting for 1 sub-compilation(s) to finish...
Compiled 21 VHDL Units
Built simulation executable lifo_tb_isim_beh.exe
Fuse Memory Usage: 37304 KB
Fuse CPU Usage: 1031 ms
IDEAL>lifo_tb_isim_beh.exe -tclbatch isim_lifo.tcl -wdb lifo_tb_isim_beh.wdb
ISim P.20131013 (signature 0x7708f090)
WARNING: A WEBPACK license was found.
WARNING: Please use Xilinx License Configuration Manager to check out a full ISim license.
WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for more information on t
This is a Lite version of ISim.
Time resolution is 1 ps
Simulator is doing circuit initialization process.
at 0 ps, Instance /lifo_ideal_tb/UUT/ : Warning: NUMERIC_STD."=": metavalue detected, returning FAL
at 0 ps, Instance /lifo_ideal_tb/UUT/ : Warning: NUMERIC_STD."=": metavalue detected, returning FAL
Finished circuit initialization process.

rence is considered.

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L_tb

the differences between the Lite and the Full version.

rence is considered.

[illegible]

any work.

the differences between the Lite and the Full version.

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0V_DN/2024/05_LIFO/STUDENTI/IDEAL/ud_counter_IDEAL.vhd".
1dI/NDV_DN/2024/05_LIFO/STUDENTI/IDEAL/ud_counter_IDEAL.vhd".
FO/STUDENTI/IDEAL/tff_IDEAL.vhd".
05_LIFO/STUDENTI/IDEAL/tff_IDEAL.vhd".