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```

-- *****
-- **** STUDENT: 64000225
-- *****
-- KOMENTARJI K OCENI NALOGE
-- Matej Možek: Ni pripomb
-- *****

LIBRARY ieee;
USE ieee.std_logic_1164.ALL;
USE ieee.numeric_std.ALL;

ENTITY muxnto1_tb IS
    generic( n_addr: natural := 2 );
END muxnto1_tb;

ARCHITECTURE behavior OF muxnto1_tb IS

    -- Component Declaration for the Unit Under Test ( UUT )

    COMPONENT muxnto1
        generic ( n_addr: natural := 2 );          -- število naslovov izbiralnika
        PORT (
            s : in std_logic_vector( n_addr - 1 downto 0 );    -- vektor naslovov
            w : in std_logic_vector( 2**n_addr - 1 downto 0 );  -- vektor podatkovnih vhodov
            f : OUT STD_LOGIC );          -- izhod izbiralnika
    END COMPONENT;

    -- Inputs
    signal s : std_logic_vector( n_addr - 1 downto 0 );
    signal w : std_logic_vector( 2**n_addr - 1 downto 0 );

    -- Outputs
    signal f : std_logic;

BEGIN

    -- Instantiate the Unit Under Test ( UUT )
    uut: muxnto1 PORT MAP (
        s => s,
        w => w,

```

```

f => f
);

-- Stimulus process
stim_proc: process
begin
    for a in 0 to 2**n_addr - 1 loop
        s <= std_logic_vector( to_unsigned( a, n_addr ) );
        for i in 0 to 2**( 2**n_addr ) - 1 loop
            w <= std_logic_vector( to_unsigned( i, 2**n_addr ) );
            wait for 10 ns;
        end loop;
    end loop;
wait;
end process;

END;

```

```

-- *****
-- **** STUDENT: 64200100
-- *****
-- KOMENTARJI K OCENI NALOGE
-- Matej Možek: Ni pripomb
-- *****
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;
USE ieee.numeric_std.ALL;

ENTITY muxnto1_tb IS
    generic( n_addr: natural := 2 );
END ENTITY;

ARCHITECTURE behavior OF muxnto1_tb IS

    COMPONENT muxnto1 IS
        generic ( n_addr: natural := 2 );
        PORT( s:in std_logic_vector( n_addr - 1 downto 0 );
              w:in std_logic_vector( 2**n_addr - 1 downto 0 );
              f:OUT STD_LOGIC );
    END COMPONENT;

    signal      s: std_logic_VECTOR( n_addr - 1 downto 0 );
    signal      w: std_logic_VECTOR( 2**n_addr - 1 downto 0 );
    signal      f: std_logic;

BEGIN
    uut: muxnto1 PORT MAP( s => s,w => w,f => f );

    sproc: process
    begin
        for g in 0 to 2**n_addr - 1 loop
            s    <= STD_LOGIC_VECTOR( to_unsigned( g, n_addr ) );
            for i in 0 to 2**( 2**n_addr ) - 1 loop
                w    <= STD_LOGIC_VECTOR( to_unsigned( i, 2**n_addr ) );
            wait for 10 ns;
            end loop;
        end loop;
    wait;

```

```
end process;  
END;
```

```

-- *****
-- **** STUDENT: 64200163
-- *****
-- KOMENTARJI K OCENI NALOGE
-- Matej Možek: Ni pripomb
-- *****

library ieee;
use ieee.std_logic_1164.all;
use ieee.numeric_std.all;

entity muxnto1_tb is
    generic( n_addr : natural := 2 );
end muxnto1_tb;

architecture behavior of muxnto1_tb is
    component muxnto1
        generic( n_addr: natural := 2 );
        port(
            s : in std_logic_vector( n_addr - 1 downto 0 );
            w : in std_logic_vector( 2**n_addr - 1 downto 0 );
            f : out std_logic
        );
    end component;

    signal s : std_logic_vector( n_addr - 1 downto 0 ) := ( others => '0' );
    signal w : std_logic_vector( 2**n_addr - 1 downto 0 ) := ( others => '0' );
    signal f : std_logic;
begin
    uut: muxnto1
        generic map( n_addr => n_addr )
        port map(
            s => s,
            w => w,
            f => f
        );
    stim_proc : process
    begin
        for i in 0 to 2**n_addr - 1 loop
            s <= std_logic_vector( to_unsigned( i, n_addr ) );
            for j in 0 to 2**n_addr - 1 loop
                w <= std_logic_vector( to_unsigned( j, 2**n_addr ) );
            end loop
        end loop
    end process
end muxnto1_tb;

```

```
        wait for 10 ns;  
    end loop;  
end loop;  
wait;  
end process;  
end;
```

```

-- *****
-- **** STUDENT: 64200238
-- *****
-- KOMENTARJI K OCENI NALOGE
-- Matej Možek: Ni pripomb
-- *****
--      --      --      --      --      --      --      --      --      --      --      --      --      --      --      --
--      --      --      --      --      --      --      --      --      --      --      --      --      --      --
--      --      --      --      --      --
-- Company:
-- Engineer:
--
-- Create Date: 22:05:17 12/20/2024
-- Design Name:
-- Module Name: C:/Users/Simon/Desktop/faks/NDS/4_domaca/FIFO/muxnto1_tb.vhd
-- Project Name: FIFO
-- Target Device:
-- Tool versions:
-- Description:
--
-- VHDL Test Bench Created by ISE for module: muxnto1
--
-- Dependencies:
--
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
--
-- Notes:
-- This testbench has been automatically generated using types std_logic and
-- std_logic_vector for the ports of the unit under test. Xilinx recommends
-- that these types always be used for the top-level I/O of a design in order
-- to guarantee that the testbench will bind correctly to the post-implementation
-- simulation model.
--      --      --      --      --      --      --      --      --      --      --      --      --      --      --      --
--      --      --      --      --      --      --      --      --      --      --      --      --      --      --
--      --      --      --      --      --
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;
USE ieee.numeric_std.ALL;

```



```
-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
-- USE ieee.numeric_std.ALL;
```

```
ENTITY muxnto1_tb IS
generic( n_addr: natural := 2 );
END muxnto1_tb;
```

```
ARCHITECTURE behavior OF muxnto1_tb IS
```

```
    -- Component Declaration for the Unit Under Test ( UUT )
```

```
COMPONENT muxnto1 IS
    generic ( n_addr: natural := 2 );          -- število naslovov izbiralnika
    PORT (
        s : in std_logic_vector( n_addr - 1 downto 0 );    -- vektor naslovov
        w : in std_logic_vector( 2*n_addr - 1 downto 0 );  -- vektor podatkovnih vhodov
        f : OUT STD_LOGIC );          -- izhod izbiralnika
    END COMPONENT;
```

```
    -- Inputs
```

```
signal      s : std_logic_vector( n_addr - 1 downto 0 ) := ( others => '0' );
signal      w : std_logic_vector( 2*n_addr - 1 downto 0 ) := ( others => '0' );
```

```
    -- Outputs
```

```
signal      f : std_logic;
-- No clocks detected in port list. Replace <clock> below with
-- appropriate port name
```

```
BEGIN
```

```
    -- Instantiate the Unit Under Test ( UUT )
```

```
uut: muxnto1 PORT MAP (
s => s,
w => w,
f => f
);
```

```
    -- Clock process definitions
```

```

    -- Stimulus process
stim_proc: process
begin

    wait for 10 ns;
        w      <="0101";
        s( 0 ) <= '0';
        s( 1 ) <= '0';
        wait for 10 ns;
            s( 0 ) <= '0';
            s( 1 ) <= '1';
    wait for 10 ns;
        s( 0 ) <= '1';
        s( 1 ) <= '0';
    wait for 10 ns;
        s( 0 ) <= '1';
        s( 1 ) <= '1';
        wait for 10 ns;

    wait;
end process;

END;

```

```

-- *****
-- **** STUDENT: 64200296
-- *****
-- KOMENTARJI K OCENI NALOGE
-- Matej Možek: Ni pripomb
-- *****
--      --      --      --      --      --      --      --      --      --      --      --      --      --      --      --      --
--      --      --      --      --      --      --      --      --      --      --      --      --      --      --      --      --
--      --      --      --      --      --
-- Company:
-- Engineer:
--
-- Create Date: 20:10:50 12/20/2024
-- Design Name:
-- Module Name: C:/Users/Tim/Downloads/FIFO/FIFO/muxnto1_tb.vhd
-- Project Name: FIFO
-- Target Device:
-- Tool versions:
-- Description:
--
-- VHDL Test Bench Created by ISE for module: muxnto1
--
-- Dependencies:
--
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
--
-- Notes:
-- This testbench has been automatically generated using types std_logic and
-- std_logic_vector for the ports of the unit under test. Xilinx recommends
-- that these types always be used for the top-level I/O of a design in order
-- to guarantee that the testbench will bind correctly to the post-implementation
-- simulation model.
--      --      --      --      --      --      --      --      --      --      --      --      --      --      --      --      --
--      --      --      --      --      --      --      --      --      --      --      --      --      --      --      --      --
--      --      --      --      --      --
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;
USE ieee.numeric_std.ALL;

```

```

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
-- USE ieee.numeric_std.ALL;

ENTITY muxnto1_tb IS
    generic( n_addr: natural := 2 );
END muxnto1_tb;

ARCHITECTURE behavior OF muxnto1_tb IS

    -- Component Declaration for the Unit Under Test ( UUT )

    COMPONENT muxnto1
    PORT(
        s : IN std_logic_vector( 1 downto 0 );
        w : IN std_logic_vector( 3 downto 0 );
        f : OUT std_logic
    );
    END COMPONENT;

    -- Inputs
    signal      s : std_logic_vector( 1 downto 0 ) := ( others => '0' );
    signal      w : std_logic_vector( 3 downto 0 ) := ( others => '0' );

    -- Outputs
    signal      f : std_logic;
    -- No clocks detected in port list. Replace <clock> below with
    -- appropriate port name
BEGIN

    -- Instantiate the Unit Under Test ( UUT )
    uut: muxnto1 PORT MAP (
        s => s,
        w => w,
        f => f
    );

    -- Stimulus process
    stim_proc: process

```

```
begin
    for i in 0 to 2**n_addr - 1 loop
        s      <= std_logic_vector( to_unsigned( i, n_addr ) );
        for j in 0 to 2**( 2**n_addr ) - 1 loop
            w      <= std_logic_vector( to_unsigned( j, 2**n_addr ) );
            wait for 10 ns;
        end loop;
    end loop;
    -- insert stimulus here

    wait;
end process;

END;
```

```

-- *****
-- **** STUDENT: 64200385
-- *****
-- KOMENTARJI K OCENI NALOGE
-- Matej Možek: Ni pripomb
-- *****
-- TestBench Template

LIBRARY ieee;
USE ieee.std_logic_1164.ALL;
USE ieee.numeric_std.ALL;

ENTITY muxnto1_tb IS
    generic( n_addr: natural := 2 );
END muxnto1_tb;

ARCHITECTURE behavior OF muxnto1_tb IS

    -- Component Declaration for the Unit Under Test ( UUT )

    COMPONENT muxnto1
        generic( n_addr: natural := 2 );
    PORT(
        s : IN std_logic_vector( n_addr - 1 downto 0 );
        w : IN std_logic_vector( 2*n_addr - 1 downto 0 );
        f : OUT std_logic
    );
    END COMPONENT;

    -- Inputs
    signal      s : std_logic_vector( n_addr - 1 downto 0 );
    signal      w : std_logic_vector( 2*n_addr - 1 downto 0 );

    -- Outputs
    signal      f : std_logic;

BEGIN

    -- Instantiate the Unit Under Test ( UUT )
    uut: muxnto1 PORT MAP (

```

```

s => s,
w => w,
f => f
);

-- Stimulus process
stim_proc: process
begin
for i in 0 to 2**n_addr - 1 loop
    s    <= std_logic_vector( to_unsigned( i, n_addr ) );
    for j in 0 to 2**( 2**n_addr ) - 1 loop
        w    <= std_logic_vector( to_unsigned( j, 2**n_addr ) );
        wait for 10 ns;
    end loop;
end loop;
wait;
end process;

END;

```

```

-- *****
-- **** STUDENT: 64210113
-- *****
-- KOMENTARJI K OCENI NALOGE
-- Matej Možek: Ni pripomb
-- *****
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;
USE ieee.numeric_std.ALL;

ENTITY muxnto1_tb IS
    generic( n_addr: natural := 2 );
END muxnto1_tb;

ARCHITECTURE behavior OF muxnto1_tb IS

    COMPONENT muxnto1
        generic ( n_addr: natural := 2 );
        PORT(
            s : IN std_logic_vector( ( n_addr - 1 ) downto 0 );
            w : IN std_logic_vector( ( 2*n_addr - 1 ) downto 0 );
            f : OUT std_logic
        );
    END COMPONENT;

    -- Inputs
    signal s : std_logic_vector( n_addr - 1 downto 0 ) := ( others => '0' );
    signal w : std_logic_vector( 2*n_addr - 1 downto 0 ) := ( others => '0' );

    -- Outputs
    signal f : std_logic;

BEGIN

    -- Instantiate the Unit Under Test ( UUT )
    uut: muxnto1 PORT MAP (
        s => s,
        w => w,
        f => f
    );

```



```
stim_proc: process

variable a : integer := 0;
variable i : integer := 0;

begin

while a < 2**n_addr loop
s    <= std_logic_vector( to_unsigned( a, n_addr ) );

i := 0;
while i < 2**( 2**n_addr ) loop
w    <= std_logic_vector( to_unsigned( i, 2**n_addr ) );
wait for 10 ns;
i := i + 1;
end loop;

a := a + 1;

end loop;

wait;
end process;

END behavior;
```

```

-- *****
-- **** STUDENT: 64210132
-- *****
-- KOMENTARJI K OCENI NALOGE
-- Matej Možek: Ni pripomb
-- *****
--      --      --      --      --      --      --      --      --      --      --      --      --      --      --      --
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--      --      --      --      --      --
-- Company:
-- Engineer:
--
-- Create Date: 01:23:59 12/23/2024
-- Design Name:
-- Module Name: C:/Users/blazk/Desktop/NDV/DN/fifo/mux/muxnto1_tb.vhd
-- Project Name: mux
-- Target Device:
-- Tool versions:
-- Description:
--
-- VHDL Test Bench Created by ISE for module: muxnto1
--
-- Dependencies:
--
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
--
-- Notes:
-- This testbench has been automatically generated using types std_logic and
-- std_logic_vector for the ports of the unit under test. Xilinx recommends
-- that these types always be used for the top-level I/O of a design in order
-- to guarantee that the testbench will bind correctly to the post-implementation
-- simulation model.
--      --      --      --      --      --      --      --      --      --      --      --      --      --      --      --
--      --      --      --      --      --      --      --      --      --      --      --      --      --      --
--      --      --      --      --      --
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;
use ieee.numeric_std.all;

```

```
-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
-- USE ieee.numeric_std.ALL;
```

```
ENTITY muxnto1_tb IS
END muxnto1_tb;
```

```
ARCHITECTURE behavior OF muxnto1_tb IS
```

```
    -- Component Declaration for the Unit Under Test ( UUT )
```

```
    COMPONENT muxnto1
        GENERIC( n_addr: natural :=2 );
    PORT(
        s : IN std_logic_vector( 1 downto 0 );
        w : IN std_logic_vector( 3 downto 0 );
        f : OUT std_logic
    );
END COMPONENT;
```

```
    -- Inputs
```

```
    signal      s : std_logic_vector( 1 downto 0 ) := ( others => '0' );
    signal      w : std_logic_vector( 3 downto 0 ) := ( others => '0' );
```

```
    -- Outputs
```

```
    signal      f : std_logic;
    -- No clocks detected in port list. Replace <clock> below with
    -- appropriate port name
```

```
    constant    clock_period : time := 10 ns;
```

```
    signal      test_sig: unsigned( 3 downto 0 ) := ( others => '0' );
```

```
BEGIN
```

```
    -- Instantiate the Unit Under Test ( UUT )
```

```
    uut: muxnto1 PORT MAP (
        s => s,
        w => w,
```

```

f => f
);

    -- Stimulus process
stim_proc: process
begin
    -- hold reset state for 100 ns.
wait for 100 ns;

    -- insert stimulus here

        w      <= std_logic_vector( test_sig );

        for i in 0 to 15 loop
            for j in 0 to 3 loop
                s      <= std_logic_vector( to_unsigned( j,2 ) );
                wait for 100 ns;
                assert( f = w( j ) );
            end loop;

            test_sig    <= test_sig+1;
            w      <= std_logic_vector( test_sig );
            wait for 100 ns;

        end loop;
wait;
end process;

END;

```

```

-- *****
-- **** STUDENT: 64210290
-- *****
-- KOMENTARJI K OCENI NALOGE
-- Matej Možek: Ni pripomb
-- *****
--      --      --      --      --      --      --      --      --      --      --      --      --      --      --      --
--      --      --      --      --      --      --      --      --      --      --      --      --      --      --
--      --      --      --      --      --
-- Company:
-- Engineer:
--
-- Create Date: 17:51:17 12/14/2024
-- Design Name:
-- Module Name: E:/Master/NDV/DN/4DN/FIFO/FIFO/muxnto1_tb.vhd
-- Project Name: FIFO
-- Target Device:
-- Tool versions:
-- Description:
--
-- VHDL Test Bench Created by ISE for module: muxnto1
--
-- Dependencies:
--
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
--
-- Notes:
-- This testbench has been automatically generated using types std_logic and
-- std_logic_vector for the ports of the unit under test. Xilinx recommends
-- that these types always be used for the top-level I/O of a design in order
-- to guarantee that the testbench will bind correctly to the post-implementation
-- simulation model.
--      --      --      --      --      --      --      --      --      --      --      --      --      --      --      --
--      --      --      --      --      --      --      --      --      --      --      --      --      --      --
--      --      --      --      --      --
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;
USE ieee.numeric_std.ALL;

```

```

ENTITY muxnto1_tb IS
END muxnto1_tb;

ARCHITECTURE behavior OF muxnto1_tb IS

    -- Component Declaration for the Unit Under Test ( UUT )

    COMPONENT muxnto1
        GENERIC(
            n_addr : natural
        );
    PORT(
        s : IN std_logic_vector( n_addr-1 downto 0 );
        w : IN std_logic_vector( 2**n_addr-1 downto 0 );
        f : OUT std_logic
    );
    END COMPONENT;

    constant    n : natural := 4;

    -- Inputs
    signal      s : std_logic_vector( n-1 downto 0 ) := ( others => '0' );
    constant    w : std_logic_vector( 2**n-1 downto 0 ) := x"A5A5";

    -- Outputs
    signal      f : std_logic;

    constant    clock_period : time := 10 ns;
    signal      clock: std_logic;

BEGIN

    -- Instantiate the Unit Under Test ( UUT )
    uut: muxnto1
        generic map(
            n_addr => n
        )
        port map(
            s => s,           w => w,           f => f

```

```

    );

    -- Clock process definitions
clock_process :process
begin
    clock <= '0';
    wait for clock_period/2;
    clock <= '1';
    wait for clock_period/2;
end process;

    -- Stimulus process
stim_proc: process
begin
    -- hold reset state for 100 ns.
    wait for 100 ns;

    wait for clock_period*10;

    for ids in 0 to 2**n-1 loop
        s      <= std_logic_vector( to_unsigned( ids, n ) );
        wait for 10 ns;
    end loop;

    wait;
end process;

END;
```

```

-- *****
-- **** STUDENT: 64210382
-- *****
-- KOMENTARJI K OCENI NALOGE
-- Matej Možek: Ni pripomb
-- *****
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;
USE ieee.numeric_std.ALL;

ENTITY muxnto1_tb IS
    generic( n_addr: natural := 2 );
END ENTITY;

ARCHITECTURE behavior OF muxnto1_tb IS

    COMPONENT muxnto1 IS
        generic ( n_addr: natural := 2 );          -- število naslovov izbiralnika
        PORT (
            s : in std_logic_vector( n_addr - 1 downto 0 );    -- vektor naslovov
            w : in std_logic_vector( 2**n_addr - 1 downto 0 );  -- vektor podatkovnih vhodov
            f : OUT STD_LOGIC );                                -- izhod izbiralnika
    END COMPONENT;

    signal      s : std_logic_vector( n_addr - 1 downto 0 );
    signal      w : std_logic_vector( 2**n_addr - 1 downto 0 );

    signal      f : std_logic;

BEGIN

    uut: muxnto1 PORT MAP (
        s => s,          w => w,          f => f
    );

    stim_proc: process
    begin
        for a in 0 to 2**n_addr - 1 loop
            s    <= std_logic_vector( to_unsigned( a, n_addr ) );
            for i in 0 to 2**n_addr - 1 loop
                w    <= std_logic_vector( to_unsigned( i, 2**n_addr ) );
            end loop
        end loop
    end process
end behavior

```



```
        wait for 10 ns;  
    end loop;  
end loop;  
wait;  
end process;  
END;
```

```

-- *****
-- **** STUDENT: 64210384
-- *****
-- KOMENTARJI K OCENI NALOGE
-- Matej Možek: Ni pripomb
-- *****
--      --      --      --      --      --      --      --      --      --      --      --      --      --      --      --
--      --      --      --      --      --      --      --      --      --      --      --      --      --      --      --
--      --      --      --      --      --
-- Company:
-- Engineer:
--
-- Create Date: 18:57:53 12/19/2024
-- Design Name:
-- Module Name: C:/NDV/DN4/muxnto1_tb.vhd
-- Project Name: DN4
-- Target Device:
-- Tool versions:
-- Description:
--
-- VHDL Test Bench Created by ISE for module: muxnto1
--
-- Dependencies:
--
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
--
-- Notes:
-- This testbench has been automatically generated using types std_logic and
-- std_logic_vector for the ports of the unit under test. Xilinx recommends
-- that these types always be used for the top-level I/O of a design in order
-- to guarantee that the testbench will bind correctly to the post-implementation
-- simulation model.
--      --      --      --      --      --      --      --      --      --      --      --      --      --      --      --
--      --      --      --      --      --      --      --      --      --      --      --      --      --      --      --
--      --      --      --      --      --
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;

```

```

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
USE ieee.numeric_std.ALL;

ENTITY muxnto1_tb IS
    generic( n_addr: natural := 2 );
END muxnto1_tb;

ARCHITECTURE behavior OF muxnto1_tb IS

    -- Component Declaration for the Unit Under Test ( UUT )

    COMPONENT muxnto1
        generic ( n_addr: natural := 2 );      -- število naslovov izbiralnika
    PORT(
        s : IN std_logic_vector( n_addr - 1 downto 0 );    -- vektor naslovov
        w : IN std_logic_vector( 2**n_addr - 1 downto 0 ); -- vektor podatkovnih vhodov
        f : OUT std_logic                                  -- izhod izbiralnika
    );
    END COMPONENT;

    -- Inputs
    signal      s : std_logic_vector( n_addr - 1 downto 0 );
    signal      w : std_logic_vector( 2**n_addr - 1 downto 0 );

    -- Outputs
    signal      f : std_logic;

BEGIN

    -- Instantiate the Unit Under Test ( UUT )
    uut: muxnto1 PORT MAP (
        s => s,
        w => w,
        f => f
    );

    -- Stimulus process
    stim_proc: process

```

```
begin
  for a in 0 to 2**n_addr - 1 loop
    s <= std_logic_vector( to_unsigned( a, n_addr ) );
    for i in 0 to 2**( 2**n_addr ) - 1 loop
      w <= std_logic_vector( to_unsigned( i, 2**n_addr ) );
      wait for 10 ns;
    end loop;
  end loop;
wait;
end process;

END;
```

```

-- *****
-- **** STUDENT: 64210386
-- *****
-- KOMENTARJI K OCENI NALOGE
-- Matej Možek: Ni pripomb
-- *****
--      --      --      --      --      --      --      --      --      --      --      --      --      --      --      --      --
--      --      --      --      --      --      --      --      --      --      --      --      --      --      --      --      --
--      --      --      --      --      --
-- Company:
-- Engineer:
--
-- Create Date: 12:55:59 12/10/2024
-- Design Name:
-- Module Name: /home/ise/Xilinx_shared/domaca_naloga_4/muxnto1_tb.vhd
-- Project Name: domaca_naloga_4
-- Target Device:
-- Tool versions:
-- Description:
--
-- VHDL Test Bench Created by ISE for module: muxnto1
--
-- Dependencies:
--
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
--
-- Notes:
-- This testbench has been automatically generated using types std_logic and
-- std_logic_vector for the ports of the unit under test. Xilinx recommends
-- that these types always be used for the top-level I/O of a design in order
-- to guarantee that the testbench will bind correctly to the post-implementation
-- simulation model.
--      --      --      --      --      --      --      --      --      --      --      --      --      --      --      --      --
--      --      --      --      --      --      --      --      --      --      --      --      --      --      --      --      --
--      --      --      --      --      --
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;
USE ieee.numeric_std.ALL;

```

```
-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
-- USE ieee.numeric_std.ALL;
```

```
ENTITY muxnto1_tb IS
generic( n_addr: natural := 4 );
END muxnto1_tb;
```

```
ARCHITECTURE behavior OF muxnto1_tb IS
```

```
    -- Component Declaration for the Unit Under Test ( UUT )
```

```
    COMPONENT muxnto1 is
        generic( n_addr: natural := 4 );
    PORT(
        s : IN std_logic_vector( n_addr - 1 downto 0 );
        w : IN std_logic_vector( 2**n_addr - 1 downto 0 );
        f : OUT std_logic
    );
    END COMPONENT;
```

```
    -- Inputs
```

```
    signal      s : std_logic_vector( n_addr - 1 downto 0 ) := ( others => '0' );
    signal      w : std_logic_vector( 2**n_addr - 1 downto 0 ) := ( others => '0' );
```

```
    -- Outputs
```

```
    signal      f : std_logic;
    -- No clocks detected in port list. Replace <clock> below with
    -- appropriate port name
```

```
BEGIN
```

```
    -- Instantiate the Unit Under Test ( UUT )
```

```
    uut: muxnto1 PORT MAP (
        s => s,
        w => w,
        f => f
    );
```

```
    -- Stimulus process
```

```
stim_proc: process
begin
    -- insert stimulus here
    for i in 0 to 2**n_addr - 1 loop
        s      <= std_logic_vector( to_unsigned( i, n_addr ) );
        for u in 0 to 2**( 2**n_addr ) - 1 loop
            w      <= std_logic_vector( to_unsigned( u, 2**n_addr ) );
            wait for 10 ns;
        end loop;
    end loop;

    wait;
end process;

END;
```

```

-- *****
-- **** STUDENT: 64210445
-- *****
-- KOMENTARJI K OCENI NALOGE
-- Matej Možek: Ni pripomb
-- *****
--      --      --      --      --      --      --      --      --      --      --      --      --      --      --      --
--      --      --      --      --      --      --      --      --      --      --      --      --      --      --      --
--      --      --      --      --      --
-- Company:
-- Engineer:
--
-- Create Date: 10:11:24 12/21/2024
-- Design Name:
-- Module Name: C:/UN-LJ/NDV/DVaja4/FIFO/muxnto1_tb.vhd
-- Project Name: FIFO
-- Target Device:
-- Tool versions:
-- Description:
--
-- VHDL Test Bench Created by ISE for module: muxnto1
--
-- Dependencies:
--
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
--
-- Notes:
-- This testbench has been automatically generated using types std_logic and
-- std_logic_vector for the ports of the unit under test. Xilinx recommends
-- that these types always be used for the top-level I/O of a design in order
-- to guarantee that the testbench will bind correctly to the post-implementation
-- simulation model.
--      --      --      --      --      --      --      --      --      --      --      --      --      --      --      --
--      --      --      --      --      --      --      --      --      --      --      --      --      --      --      --
--      --      --      --      --      --
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;
USE ieee.numeric_std.ALL;

```



```
-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
-- USE ieee.numeric_std.ALL;
```

```
ENTITY muxnto1_tb IS
    generic( n_addr: natural := 4 );
END muxnto1_tb;
```

```
ARCHITECTURE behavior OF muxnto1_tb IS
```

```
    -- Component Declaration for the Unit Under Test ( UUT )
```

```
    COMPONENT muxnto1 IS generic( n_addr: natural := 2 );    -- število naslovov izbiralnika
    PORT (
        s : in std_logic_vector( n_addr - 1 downto 0 );    -- vektor naslovov
        w : in std_logic_vector( 2*n_addr - 1 downto 0 );    -- vektor podatkovnih vhodov
        f : OUT STD_LOGIC    -- izhod izbiralnika
    );
END COMPONENT;
```

```
    -- Inputs
```

```
signal    s : std_logic_vector( 1 downto 0 ) := ( others => '0' );
signal    w : std_logic_vector( 3 downto 0 ) := ( others => '0' );
signal    clock : std_logic := '0';
```

```
    -- Outputs
```

```
signal    f : std_logic;
    -- No clocks detected in port list. Replace <clock> below with
    -- appropriate port name
```

```
constant    clock_period : time := 10 ns;
```

```
BEGIN
```

```
    -- Instantiate the Unit Under Test ( UUT )
```

```
    uut: muxnto1 PORT MAP (
        s => s,
        w => w,
        f => f
    );
```

```

    -- Stimulus process
stim_proc: process
begin
    -- hold reset state for 100 ns.
wait for 100 ns;
    -- insert stimulus here

    for a in 0 to 2**n_addr - 1 loop
        s <= std_logic_vector( to_unsigned( a, n_addr ) );
        for i in 0 to 2**( 2**n_addr ) - 1 loop
            w <= std_logic_vector( to_unsigned( i, 2**n_addr ) );
            wait for clock_period;
        end loop;
    end loop;

wait;

wait;
end process;

END;

```

```

-- *****
-- **** STUDENT: 64210455
-- *****
-- KOMENTARJI K OCENI NALOGE
-- Matej Možek: Ni pripomb
-- *****
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;
USE ieee.numeric_std.ALL;

ENTITY muxnto1_tb IS
    generic( n_addr: natural := 2 );
END ENTITY;

ARCHITECTURE behavior OF muxnto1_tb IS

    COMPONENT muxnto1 IS
        generic ( n_addr: natural := 2 );           -- število naslovov izbiralnika
        PORT (
            s : in std_logic_vector( n_addr - 1 downto 0 );    -- vektor naslovov
            w : in std_logic_vector( 2*n_addr - 1 downto 0 );    -- vektor podatkovnih vhodov
            f : OUT STD_LOGIC );    -- izhod izbiralnika
    END COMPONENT;

    -- Inputs
    signal s : std_logic_vector( n_addr - 1 downto 0 );
    signal w : std_logic_vector( 2*n_addr - 1 downto 0 );

    -- Outputs
    signal f : std_logic;

BEGIN

    -- Instantiate the Unit Under Test ( UUT )
    uut: muxnto1 PORT MAP (
        s => s,
        w => w,
        f => f
    );

    -- Stimulus process
    stim_proc: process
    begin

```

```
for a in 0 to 2**n_addr - 1 loop
s    <= std_logic_vector( to_unsigned( a, n_addr ) );
    for i in 0 to 2**( 2**n_addr ) - 1 loop
        w    <= std_logic_vector( to_unsigned( i, 2**n_addr ) );
        wait for 10 ns;
    end loop;
end loop;

wait;
end process;

END;
```

```

-- *****
-- **** STUDENT: 64210457
-- *****
-- KOMENTARJI K OCENI NALOGE
-- Matej Možek: Ni pripomb
-- *****
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;
USE ieee.numeric_std.ALL;

ENTITY muxnto1_tb IS
    generic( n_addr: natural := 2 );
END ENTITY;

ARCHITECTURE behavior OF muxnto1_tb IS

    COMPONENT muxnto1 IS
        generic ( n_addr: natural := 2 );          -- število naslovov izbiralnika
        PORT (
            s : in std_logic_vector( n_addr - 1 downto 0 );    -- vektor naslovov
            w : in std_logic_vector( 2*n_addr - 1 downto 0 );    -- vektor podatkovnih vhodov
            f : OUT STD_LOGIC );          -- izhod izbiralnika
    END COMPONENT;

    -- Inputs
    signal s : std_logic_vector( n_addr - 1 downto 0 );
    signal w : std_logic_vector( 2*n_addr - 1 downto 0 );

    -- Outputs
    signal f : std_logic;

BEGIN

    -- Instantiate the Unit Under Test ( UUT )
    uut: muxnto1 PORT MAP (
        s => s,          w => w,          f => f
    );

    -- Stimulus process
    stim_proc: process
    begin

```

```
for a in 0 to 2**n_addr - 1 loop
s    <= std_logic_vector( to_unsigned( a, n_addr ) );
    for i in 0 to 2**( 2**n_addr ) - 1 loop
        w    <= std_logic_vector( to_unsigned( i, 2**n_addr ) );
        wait for 10 ns;
    end loop;
end loop;

wait;
end process;

END;
```

```

-- *****
-- **** STUDENT: 64240430
-- *****
-- KOMENTARJI K OCENI NALOGE
-- Matej Možek: Ni pripomb
-- *****
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;
use ieee.numeric_std.all;
ENTITY muxnto1_tb IS
    generic ( n_addr: natural := 2 );
END muxnto1_tb;

ARCHITECTURE behavior OF muxnto1_tb IS

    -- Component Declaration for the Unit Under Test ( UUT )

    COMPONENT muxnto1
    PORT(
        s : IN std_logic_vector( 1 downto 0 );
        w : IN std_logic_vector( 3 downto 0 );
        f : OUT std_logic
    );
    END COMPONENT;

    -- Inputs
    signal      s : std_logic_vector( 1 downto 0 ) := ( others => '0' );
    signal      w : std_logic_vector( 3 downto 0 ) := ( others => '0' );

    -- Outputs
    signal      f : std_logic;
    -- No clocks detected in port list. Replace <clock> below with
    -- appropriate port name
    signal      clock : std_logic;
    constant    clock_period : time := 100 ns;

BEGIN

    -- Instantiate the Unit Under Test ( UUT )
    uut: muxnto1 PORT MAP (

```

```

s => s,
w => w,
f => f
);

    -- Clock process definitions
clock_process :process
begin
    clock <= '0';
    wait for clock_period/2;
    clock <= '1';
    wait for clock_period/2;
end process;

    -- Stimulus process
stim_proc: process
begin

    for i in 0 to 2**n_addr - 1 loop
        s <= std_logic_vector( to_unsigned( i, n_addr ) );
        for j in 0 to 2**( 2**n_addr ) - 1 loop
            w <= std_logic_vector( to_unsigned( j, 2**n_addr ) );
            wait for clock_period;
        end loop;
    end loop;

wait;
end process;

END;

```



```

-- *****
-- **** STUDENT: 64200288
-- *****
-- KOMENTARJI K OCENI NALOGE
-- Matej Možek: Ni pripomb
-- *****
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;
USE ieee.numeric_std.ALL;

ENTITY muxnto1_tb IS
generic( n_addr: natural := 2 );
END muxnto1_tb;

ARCHITECTURE behavior OF muxnto1_tb IS

COMPONENT muxnto1 IS
    generic ( n_addr: natural := 2 );          -- Ātevílo naslovov izbiralnika
    PORT (
        s : in std_logic_vector( n_addr - 1 downto 0 );    -- vektor naslovov
        w : in std_logic_vector( 2**n_addr - 1 downto 0 );  -- vektor podatkovnih vhodov
        f : OUT STD_LOGIC );                                -- izhod izbiralnika
    END COMPONENT;

    signal          s : std_logic_vector( n_addr - 1 downto 0 ) := ( others => '0' );
    signal          w : std_logic_vector( 2**n_addr - 1 downto 0 ) := ( others => '0' );
    signal          f : std_logic;

BEGIN
    uut: muxnto1 PORT MAP( s => s, w => w, f => f );

    s_proc: process
    begin
        for g in 0 to 2**n_addr - 1 loop
            s <= STD_LOGIC_VECTOR( to_unsigned( g, n_addr ) );
            for i in 0 to 2**( 2**n_addr ) - 1 loop
                w <= STD_LOGIC_VECTOR( to_unsigned( i, 2**n_addr ) );
            wait for 10 ns;
            end loop;
        end loop;
    wait;

```

```
end process;  
END;
```

