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-- KOMENTARJI K OCENI NALOGE -- Matej Možek: Ni pripomb.....	2

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LIBRARY ieee;
USE ieee.std_logic_1164.ALL;
USE ieee.numeric_std.ALL;

ENTITY muxdff_tb IS
END muxdff_tb;

ARCHITECTURE behavior OF muxdff_tb IS

    -- Component Declaration for the Unit Under Test ( UUT )

    COMPONENT muxdff
    PORT(
        S : IN std_logic_vector( 3 downto 0 );
        D : IN std_logic_vector( 15 downto 0 );
        clk : IN std_logic;
        nCLEAR : IN std_logic;
        Q : OUT std_logic
    );
    END COMPONENT;

    -- Inputs
    signal          S : std_logic_vector( 3 downto 0 ) := ( others => '0' );
    signal          D : std_logic_vector( 15 downto 0 ) := x"A5A5";
    signal          clk : std_logic := '0';
    signal          nCLEAR : std_logic := '0';

    -- Outputs
    signal          Q : std_logic;

    -- Clock period definitions
    constant        clk_period : time := 10 ns;

```

```
BEGIN
```

```
    -- Instantiate the Unit Under Test ( UUT )
```

```
    uut: muxdff PORT MAP (  
    S => S,  
    D => D,  
    clk => clk,  
    nCLEAR => nCLEAR,  
    Q => Q  
    );
```

```
    -- Clock process definitions
```

```
    clk_process :process  
    begin  
        clk    <= '0';  
        wait for clk_period/2;  
        clk    <= '1';  
        wait for clk_period/2;  
    end process;
```

```
    -- Stimulus process
```

```
    stim_proc: process  
    begin  
        -- hold reset state for 100 ns.  
        wait for 100 ns;  
  
        wait for clk_period*10;  
  
        nCLEAR <= '1';  
        wait for clk_period;  
  
        for i in 0 to 15 loop  
            S    <= std_logic_vector( to_unsigned( i,S'length ) );  
            wait for clk_period;  
        end loop;  
  
        wait;  
    end process;  
  
END;
```

