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```

-- *****
-- **** STUDENT: 64000225
-- *****
-- KOMENTARJI K OCENI NALOGE
-- Matej Možek: Ni pripomb
-- *****
LIBRARY ieee ;
USE ieee.std_logic_1164.all;

ENTITY muxdff IS
    generic( n_addr: natural := 2 ); -- stevilo naslovov ULM strukture
    PORT (
        S : in std_logic_vector( n_addr - 1 downto 0 );
        D : in      std_logic_vector( 2*n_addr - 1 downto 0 ); -- vektor vhodov ULM strukture
        clk, -- signal           ure ( prožen na sprednjo fronto )
        nCLEAR : IN std_logic; -- signal           za asinhrono brisanje ( nCLEAR = '0' se postavi
Q=>'0' )
        Q : out std_logic -- izhod ULM strukture
    );
END muxdff;

ARCHITECTURE ideal OF muxdff IS
    signal      muxout : std_logic;

    COMPONENT muxnto1 IS
        generic( n_addr: natural := 2 );
        PORT (
            s : in std_logic_vector( n_addr - 1 downto 0 );
            w : in      std_logic_vector( 2*n_addr - 1 downto 0 );
            f : OUT STD_LOGIC
        );
    END COMPONENT;

    COMPONENT dff IS
        PORT (
            D, clk, nCLEAR : IN STD_LOGIC;
            Q : OUT std_logic );
    END COMPONENT;

    BEGIN
        U0: muxnto1 generic map ( n_addr => n_addr ) port map ( s => S, w => D, f => muxout );
        U1: dff port map ( D => muxout, clk => clk, nCLEAR => nCLEAR, Q => Q );
    END ideal;

```

```

-- *****
-- **** STUDENT: 64190088
-- *****
-- KOMENTARJI K OCENI NALOGE
-- Matej Možek: Ni pripomb
-- *****
LIBRARY ieee ;
USE ieee.std_logic_1164.all;

ENTITY muxdff IS
    generic( n_addr: natural := 2 ); -- stevilo naslovov ULM strukture
    PORT (
        S : in std_logic_vector( n_addr - 1 downto 0 );
        D : in      std_logic_vector( 2**n_addr - 1 downto 0 ); -- vektor vhodov ULM strukture
        clk, -- signal          ure ( prožen na sprednjo fronto )
        nCLEAR : IN std_logic; -- signal          za asinhrono brisanje ( nCLEAR = '0' se postavi
Q=>'0' )
        Q : out std_logic -- izhod ULM strukture
    );
END muxdff;

ARCHITECTURE ideal OF muxdff IS
    signal      muxout : std_logic;

    COMPONENT muxnto1 IS
        generic( n_addr: natural := 2 );
        PORT (
            s : in std_logic_vector( n_addr - 1 downto 0 );
            w : in      std_logic_vector( 2**n_addr - 1 downto 0 );
            f : OUT STD_LOGIC
        );
    END COMPONENT;

    COMPONENT dff IS
        PORT (
            D, clk, nCLEAR : IN STD_LOGIC;
            Q : OUT std_logic );
    END COMPONENT;

    BEGIN
        U0: muxnto1 generic map ( n_addr => n_addr ) port map ( s => S, w => D, f => muxout );
        U1: dff port map ( D => muxout, clk => clk, nCLEAR => nCLEAR, Q => Q );
    END ideal;

```

```

-- *****
-- **** STUDENT: 64200100
-- *****
-- KOMENTARJI K OCENI NALOGE
-- Matej Možek: Ni pripomb
-- *****
LIBRARY ieee ;
USE ieee.std_logic_1164.all;

ENTITY muxdff IS
    generic( n_addr: natural := 2 ); -- stevilo naslovov ULM strukture
    PORT (
        S : in std_logic_vector( n_addr - 1 downto 0 );
        D : in      std_logic_vector( 2**n_addr - 1 downto 0 ); -- vektor vhodov ULM strukture
        clk, -- signal           ure ( prožen na sprednjo fronto )
        nCLEAR : IN std_logic; -- signal           za asinhrono brisanje ( nCLEAR = '0' se postavi
Q=>'0' )
        Q : out std_logic -- izhod ULM strukture
    );
END muxdff;

ARCHITECTURE ideal OF muxdff IS
    signal      muxout : std_logic;

    COMPONENT muxnto1 IS
        generic( n_addr: natural := 2 );
        PORT (
            s : in std_logic_vector( n_addr - 1 downto 0 );
            w : in      std_logic_vector( 2**n_addr - 1 downto 0 );
            f : OUT STD_LOGIC
        );
    END COMPONENT;

    COMPONENT dff IS
        PORT (
            D, clk, nCLEAR : IN STD_LOGIC;
            Q : OUT std_logic );
    END COMPONENT;

    BEGIN
        U0: muxnto1 generic map ( n_addr => n_addr ) port map ( s => S, w => D, f => muxout );
        U1: dff port map ( D => muxout, clk => clk, nCLEAR => nCLEAR, Q => Q );
    END ideal;

```

```

-- *****
-- **** STUDENT: 64200112
-- *****
-- KOMENTARJI K OCENI NALOGE
-- Matej Možek: Ni pripomb
-- *****
LIBRARY ieee ;
USE ieee.std_logic_1164.all;

ENTITY muxdff IS
    generic( n_addr: natural := 2 ); -- stevilo naslovov ULM strukture
    PORT (
        S : in std_logic_vector( n_addr - 1 downto 0 );
        D : in std_logic_vector( 2**n_addr - 1 downto 0 ); -- vektor vhodov ULM strukture
        clk, -- signal ure ( prožen na sprednjo fronto )
        nCLEAR : IN std_logic; -- signal za asinhrono brisanje ( nCLEAR = '0' se postavi
Q=>'0' )
        Q : out std_logic -- izhod ULM strukture
    );
END muxdff;

ARCHITECTURE ideal OF muxdff IS
    signal muxout : std_logic;

    COMPONENT muxnto1 IS
        generic( n_addr: natural := 2 );
        PORT (
            s : in std_logic_vector( n_addr - 1 downto 0 );
            w : in std_logic_vector( 2**n_addr - 1 downto 0 );
            f : OUT STD_LOGIC
        );
    END COMPONENT;

    COMPONENT dff IS
        PORT (
            D, clk, nCLEAR : IN STD_LOGIC;
            Q : OUT std_logic );
    END COMPONENT;

    BEGIN
        U0: muxnto1 generic map ( n_addr => n_addr ) port map ( s => S, w => D, f => muxout );
        U1: dff port map ( D => muxout, clk => clk, nCLEAR => nCLEAR, Q => Q );
    END ideal;

```

```

-- *****
-- **** STUDENT: 64200163
-- *****
-- KOMENTARJI K OCENI NALOGE
-- Matej Možek: Ni pripomb
-- *****
LIBRARY ieee ;
USE ieee.std_logic_1164.all;

ENTITY muxdff IS
    generic( n_addr: natural := 2 ); -- stevilo naslovov ULM strukture
    PORT (
        S : in std_logic_vector( n_addr - 1 downto 0 );
        D : in std_logic_vector( 2*n_addr - 1 downto 0 ); -- vektor vhodov ULM strukture
        clk, -- signal ure ( prožen na sprednjo fronto )
        nCLEAR : IN std_logic; -- signal za asinhrono brisanje ( nCLEAR = '0' se postavi
Q=>'0' )
        Q : out std_logic -- izhod ULM strukture
    );
END muxdff;

ARCHITECTURE ideal OF muxdff IS
    signal muxout : std_logic;

    COMPONENT muxnto1 IS
        generic( n_addr: natural := 2 );
        PORT (
            s : in std_logic_vector( n_addr - 1 downto 0 );
            w : in std_logic_vector( 2*n_addr - 1 downto 0 );
            f : OUT STD_LOGIC
        );
    END COMPONENT;

    COMPONENT dff IS
        PORT (
            D, clk, nCLEAR : IN STD_LOGIC;
            Q : OUT std_logic );
    END COMPONENT;

    BEGIN
        U0: muxnto1 generic map ( n_addr => n_addr ) port map ( s => S, w => D, f => muxout );
        U1: dff port map ( D => muxout, clk => clk, nCLEAR => nCLEAR, Q => Q );
    END ideal;

```

```

-- *****
-- **** STUDENT: 64200238
-- *****
-- KOMENTARJI K OCENI NALOGE
-- Matej Možek: Ni pripomb
-- *****
LIBRARY ieee ;
USE ieee.std_logic_1164.all;

ENTITY muxdff IS
    generic( n_addr: natural := 2 ); -- stevilo naslovov ULM strukture
    PORT (
        S : in std_logic_vector( n_addr - 1 downto 0 );
        D : in      std_logic_vector( 2**n_addr - 1 downto 0 ); -- vektor vhodov ULM strukture
        clk, -- signal          ure ( prožen na sprednjo fronto )
        nCLEAR : IN std_logic; -- signal          za asinhrono brisanje ( nCLEAR = '0' se postavi
Q=>'0' )
        Q : out std_logic -- izhod ULM strukture
    );
END muxdff;

ARCHITECTURE ideal OF muxdff IS
    signal      muxout : std_logic;

    COMPONENT muxnto1 IS
        generic( n_addr: natural := 2 );
        PORT (
            s : in std_logic_vector( n_addr - 1 downto 0 );
            w : in      std_logic_vector( 2**n_addr - 1 downto 0 );
            f : OUT STD_LOGIC
        );
    END COMPONENT;

    COMPONENT dff IS
        PORT (
            D, clk, nCLEAR : IN STD_LOGIC;
            Q : OUT std_logic );
    END COMPONENT;

    BEGIN
        U0: muxnto1 generic map ( n_addr => n_addr ) port map ( s => S, w => D, f => muxout );
        U1: dff port map ( D => muxout, clk => clk, nCLEAR => nCLEAR, Q => Q );
    END ideal;

```



```

-- *****
-- **** STUDENT: 64200288
-- *****
-- KOMENTARJI K OCENI NALOGE
-- Matej Možek: Ni pripomb
-- *****
LIBRARY ieee ;
USE ieee.std_logic_1164.all;

ENTITY muxdff IS
    generic( n_addr: natural := 2 ); -- stevilo naslovov ULM strukture
    PORT (
        S : in std_logic_vector( n_addr - 1 downto 0 );
        D : in      std_logic_vector( 2*n_addr - 1 downto 0 ); -- vektor vhodov ULM strukture
        clk, -- signal          ure ( prožen na sprednjo fronto )
        nCLEAR : IN std_logic; -- signal          za asinhrono brisanje ( nCLEAR = '0' se postavi
Q=>'0' )
        Q : out std_logic -- izhod ULM strukture
    );
END muxdff;

ARCHITECTURE ideal OF muxdff IS
    signal      muxout : std_logic;

    COMPONENT muxnto1 IS
        generic( n_addr: natural := 2 );
        PORT (
            s : in std_logic_vector( n_addr - 1 downto 0 );
            w : in      std_logic_vector( 2*n_addr - 1 downto 0 );
            f : OUT STD_LOGIC
        );
    END COMPONENT;

    COMPONENT dff IS
        PORT (
            D, clk, nCLEAR : IN STD_LOGIC;
            Q : OUT std_logic );
    END COMPONENT;

    BEGIN
        U0: muxnto1 generic map ( n_addr => n_addr ) port map ( s => S, w => D, f => muxout );
        U1: dff port map ( D => muxout, clk => clk, nCLEAR => nCLEAR, Q => Q );
    END ideal;

```

```

-- *****
-- **** STUDENT: 64200296
-- *****
-- KOMENTARJI K OCENI NALOGE
-- Matej Možek: Ni pripomb
-- *****
LIBRARY ieee ;
USE ieee.std_logic_1164.all;

ENTITY muxdff IS
    generic( n_addr: natural := 2 ); -- stevilo naslovov ULM strukture
    PORT (
        S : in std_logic_vector( n_addr - 1 downto 0 );
        D : in      std_logic_vector( 2**n_addr - 1 downto 0 ); -- vektor vhodov ULM strukture
        clk, -- signal          ure ( prožen na sprednjo fronto )
        nCLEAR : IN std_logic; -- signal          za asinhrono brisanje ( nCLEAR = '0' se postavi
Q=>'0' )
        Q : out std_logic -- izhod ULM strukture
    );
END muxdff;

ARCHITECTURE ideal OF muxdff IS
    signal      muxout : std_logic;

    COMPONENT muxnto1 IS
        generic( n_addr: natural := 2 );
        PORT (
            s : in std_logic_vector( n_addr - 1 downto 0 );
            w : in      std_logic_vector( 2**n_addr - 1 downto 0 );
            f : OUT STD_LOGIC
        );
    END COMPONENT;

    COMPONENT dff IS
        PORT (
            D, clk, nCLEAR : IN STD_LOGIC;
            Q : OUT std_logic );
    END COMPONENT;

BEGIN
    U0: muxnto1 generic map ( n_addr => n_addr ) port map ( s => S, w => D, f => muxout );
    U1: dff port map ( D => muxout, clk => clk, nCLEAR => nCLEAR, Q => Q );
END ideal;

```

```

-- *****
-- **** STUDENT: 64200385
-- *****
-- KOMENTARJI K OCENI NALOGE
-- Matej Možek: Ni pripomb
-- *****
LIBRARY ieee ;
USE ieee.std_logic_1164.all;

ENTITY muxdff IS
    generic( n_addr: natural := 2 ); -- stevilo naslovov ULM strukture
    PORT (
        S : in std_logic_vector( n_addr - 1 downto 0 );
        D : in std_logic_vector( 2*n_addr - 1 downto 0 ); -- vektor vhodov ULM strukture
        clk, -- signal ure ( prožen na sprednjo fronto )
        nCLEAR : IN std_logic; -- signal za asinhrono brisanje ( nCLEAR = '0' se postavi
Q=>'0' )
        Q : out std_logic -- izhod ULM strukture
    );
END muxdff;

ARCHITECTURE ideal OF muxdff IS
    signal muxout : std_logic;

    COMPONENT muxnto1 IS
        generic( n_addr: natural := 2 );
        PORT (
            s : in std_logic_vector( n_addr - 1 downto 0 );
            w : in std_logic_vector( 2*n_addr - 1 downto 0 );
            f : OUT STD_LOGIC
        );
    END COMPONENT;

    COMPONENT dff IS
        PORT (
            D, clk, nCLEAR : IN STD_LOGIC;
            Q : OUT std_logic );
    END COMPONENT;

    BEGIN
        U0: muxnto1 generic map ( n_addr => n_addr ) port map ( s => S, w => D, f => muxout );
        U1: dff port map ( D => muxout, clk => clk, nCLEAR => nCLEAR, Q => Q );
    END ideal;

```

```

-- *****
-- **** STUDENT: 64210113
-- *****
-- KOMENTARJI K OCENI NALOGE
-- Matej Možek: Ni pripomb
-- *****
LIBRARY ieee ;
USE ieee.std_logic_1164.all;

ENTITY muxdff IS
    generic( n_addr: natural := 2 ); -- stevilo naslovov ULM strukture
    PORT (
        S : in std_logic_vector( n_addr - 1 downto 0 );
        D : in      std_logic_vector( 2**n_addr - 1 downto 0 ); -- vektor vhodov ULM strukture
        clk, -- signal          ure ( prožen na sprednjo fronto )
        nCLEAR : IN std_logic; -- signal          za asinhrono brisanje ( nCLEAR = '0' se postavi
Q=>'0' )
        Q : out std_logic -- izhod ULM strukture
    );
END muxdff;

ARCHITECTURE ideal OF muxdff IS
    signal      muxout : std_logic;

    COMPONENT muxnto1 IS
        generic( n_addr: natural := 2 );
        PORT (
            s : in std_logic_vector( n_addr - 1 downto 0 );
            w : in      std_logic_vector( 2**n_addr - 1 downto 0 );
            f : OUT STD_LOGIC
        );
    END COMPONENT;

    COMPONENT dff IS
        PORT (
            D, clk, nCLEAR : IN STD_LOGIC;
            Q : OUT std_logic );
    END COMPONENT;

    BEGIN
        U0: muxnto1 generic map ( n_addr => n_addr ) port map ( s => S, w => D, f => muxout );
        U1: dff port map ( D => muxout, clk => clk, nCLEAR => nCLEAR, Q => Q );
    END ideal;

```

```

-- *****
-- **** STUDENT: 64210132
-- *****
-- KOMENTARJI K OCENI NALOGE
-- Matej Možek: Ni pripomb
-- *****
LIBRARY ieee ;
USE ieee.std_logic_1164.all;

ENTITY muxdff IS
    generic( n_addr: natural := 2 ); -- stevilo naslovov ULM strukture
    PORT (
        S : in std_logic_vector( n_addr - 1 downto 0 );
        D : in      std_logic_vector( 2**n_addr - 1 downto 0 ); -- vektor vhodov ULM strukture
        clk, -- signal          ure ( prožen na sprednjo fronto )
        nCLEAR : IN std_logic; -- signal          za asinhrono brisanje ( nCLEAR = '0' se postavi
Q=>'0' )
        Q : out std_logic -- izhod ULM strukture
    );
END muxdff;

ARCHITECTURE ideal OF muxdff IS
    signal      muxout : std_logic;

    COMPONENT muxnto1 IS
        generic( n_addr: natural := 2 );
        PORT (
            s : in std_logic_vector( n_addr - 1 downto 0 );
            w : in      std_logic_vector( 2**n_addr - 1 downto 0 );
            f : OUT STD_LOGIC
        );
    END COMPONENT;

    COMPONENT dff IS
        PORT (
            D, clk, nCLEAR : IN STD_LOGIC;
            Q : OUT std_logic );
    END COMPONENT;

BEGIN
    U0: muxnto1 generic map ( n_addr => n_addr ) port map ( s => S, w => D, f => muxout );
    U1: dff port map ( D => muxout, clk => clk, nCLEAR => nCLEAR, Q => Q );
END ideal;

```

```

-- *****
-- **** STUDENT: 64210290
-- *****
-- KOMENTARJI K OCENI NALOGE
-- Matej Možek: Ni pripomb
-- *****
LIBRARY ieee ;
USE ieee.std_logic_1164.all;

ENTITY muxdff IS
    generic( n_addr: natural := 2 ); -- stevilo naslovov ULM strukture
    PORT (
        S : in std_logic_vector( n_addr - 1 downto 0 );
        D : in      std_logic_vector( 2*n_addr - 1 downto 0 ); -- vektor vhodov ULM strukture
        clk, -- signal          ure ( prožen na sprednjo fronto )
        nCLEAR : IN std_logic; -- signal          za asinhrono brisanje ( nCLEAR = '0' se postavi
Q=>'0' )
        Q : out std_logic -- izhod ULM strukture
    );
END muxdff;

ARCHITECTURE ideal OF muxdff IS
    signal      muxout : std_logic;

    COMPONENT muxnto1 IS
        generic( n_addr: natural := 2 );
        PORT (
            s : in std_logic_vector( n_addr - 1 downto 0 );
            w : in      std_logic_vector( 2*n_addr - 1 downto 0 );
            f : OUT STD_LOGIC
        );
    END COMPONENT;

    COMPONENT dff IS
        PORT (
            D, clk, nCLEAR : IN STD_LOGIC;
            Q : OUT std_logic );
    END COMPONENT;

    BEGIN
        U0: muxnto1 generic map ( n_addr => n_addr ) port map ( s => S, w => D, f => muxout );
        U1: dff port map ( D => muxout, clk => clk, nCLEAR => nCLEAR, Q => Q );
    END ideal;

```

```

-- *****
-- **** STUDENT: 64210382
-- *****
-- KOMENTARJI K OCENI NALOGE
-- Matej Možek: Ni pripomb
-- *****
LIBRARY ieee ;
USE ieee.std_logic_1164.all;

ENTITY muxdff IS
    generic( n_addr: natural := 2 ); -- stevilo naslovov ULM strukture
    PORT (
        S : in std_logic_vector( n_addr - 1 downto 0 );
        D : in      std_logic_vector( 2**n_addr - 1 downto 0 ); -- vektor vhodov ULM strukture
        clk, -- signal          ure ( prožen na sprednjo fronto )
        nCLEAR : IN std_logic; -- signal          za asinhrono brisanje ( nCLEAR = '0' se postavi
Q=>'0' )
        Q : out std_logic -- izhod ULM strukture
    );
END muxdff;

ARCHITECTURE ideal OF muxdff IS
    signal      muxout : std_logic;

    COMPONENT muxnto1 IS
        generic( n_addr: natural := 2 );
        PORT (
            s : in std_logic_vector( n_addr - 1 downto 0 );
            w : in      std_logic_vector( 2**n_addr - 1 downto 0 );
            f : OUT STD_LOGIC
        );
    END COMPONENT;

    COMPONENT dff IS
        PORT (
            D, clk, nCLEAR : IN STD_LOGIC;
            Q : OUT std_logic );
    END COMPONENT;

    BEGIN
        U0: muxnto1 generic map ( n_addr => n_addr ) port map ( s => S, w => D, f => muxout );
        U1: dff port map ( D => muxout, clk => clk, nCLEAR => nCLEAR, Q => Q );
    END ideal;

```

```

-- *****
-- **** STUDENT: 64210384
-- *****
-- KOMENTARJI K OCENI NALOGE
-- Matej Možek: Ni pripomb
-- *****
LIBRARY ieee ;
USE ieee.std_logic_1164.all;

ENTITY muxdff IS
    generic( n_addr: natural := 2 ); -- stevilo naslovov ULM strukture
    PORT (
        S : in std_logic_vector( n_addr - 1 downto 0 );
        D : in      std_logic_vector( 2**n_addr - 1 downto 0 ); -- vektor vhodov ULM strukture
        clk, -- signal          ure ( prožen na sprednjo fronto )
        nCLEAR : IN std_logic; -- signal          za asinhrono brisanje ( nCLEAR = '0' se postavi
Q=>'0' )
        Q : out std_logic -- izhod ULM strukture
    );
END muxdff;

ARCHITECTURE ideal OF muxdff IS
    signal      muxout : std_logic;

    COMPONENT muxnto1 IS
        generic( n_addr: natural := 2 );
        PORT (
            s : in std_logic_vector( n_addr - 1 downto 0 );
            w : in      std_logic_vector( 2**n_addr - 1 downto 0 );
            f : OUT STD_LOGIC
        );
    END COMPONENT;

    COMPONENT dff IS
        PORT (
            D, clk, nCLEAR : IN STD_LOGIC;
            Q : OUT std_logic );
    END COMPONENT;

    BEGIN
        U0: muxnto1 generic map ( n_addr => n_addr ) port map ( s => S, w => D, f => muxout );
        U1: dff port map ( D => muxout, clk => clk, nCLEAR => nCLEAR, Q => Q );
    END ideal;

```



```

-- *****
-- **** STUDENT: 64210386
-- *****
-- KOMENTARJI K OCENI NALOGE
-- Matej Možek: Ni pripomb
-- *****
LIBRARY ieee ;
USE ieee.std_logic_1164.all;

ENTITY muxdff IS
    generic( n_addr: natural := 2 ); -- stevilo naslovov ULM strukture
    PORT (
        S : in std_logic_vector( n_addr - 1 downto 0 );
        D : in      std_logic_vector( 2**n_addr - 1 downto 0 ); -- vektor vhodov ULM strukture
        clk, -- signal          ure ( prožen na sprednjo fronto )
        nCLEAR : IN std_logic; -- signal          za asinhrono brisanje ( nCLEAR = '0' se postavi
Q=>'0' )
        Q : out std_logic -- izhod ULM strukture
    );
END muxdff;

ARCHITECTURE ideal OF muxdff IS
    signal      muxout : std_logic;

    COMPONENT muxnto1 IS
        generic( n_addr: natural := 2 );
        PORT (
            s : in std_logic_vector( n_addr - 1 downto 0 );
            w : in      std_logic_vector( 2**n_addr - 1 downto 0 );
            f : OUT STD_LOGIC
        );
    END COMPONENT;

    COMPONENT dff IS
        PORT (
            D, clk, nCLEAR : IN STD_LOGIC;
            Q : OUT std_logic );
    END COMPONENT;

    BEGIN
        U0: muxnto1 generic map ( n_addr => n_addr ) port map ( s => S, w => D, f => muxout );
        U1: dff port map ( D => muxout, clk => clk, nCLEAR => nCLEAR, Q => Q );
    END ideal;

```

```

-- *****
-- **** STUDENT: 64210445
-- *****
-- KOMENTARJI K OCENI NALOGE
-- Matej Možek: Ni pripomb
-- *****
LIBRARY ieee ;
USE ieee.std_logic_1164.all;

ENTITY muxdff IS
    generic( n_addr: natural := 2 ); -- stevilo naslovov ULM strukture
    PORT (
        S : in std_logic_vector( n_addr - 1 downto 0 );
        D : in std_logic_vector( 2**n_addr - 1 downto 0 ); -- vektor vhodov ULM strukture
        clk, -- signal ure ( prožen na sprednjo fronto )
        nCLEAR : IN std_logic; -- signal za asinhrono brisanje ( nCLEAR = '0' se postavi
Q=>'0' )
        Q : out std_logic -- izhod ULM strukture
    );
END muxdff;

ARCHITECTURE ideal OF muxdff IS
    signal muxout : std_logic;

    COMPONENT muxnto1 IS
        generic( n_addr: natural := 2 );
        PORT (
            s : in std_logic_vector( n_addr - 1 downto 0 );
            w : in std_logic_vector( 2**n_addr - 1 downto 0 );
            f : OUT STD_LOGIC
        );
    END COMPONENT;

    COMPONENT dff IS
        PORT (
            D, clk, nCLEAR : IN STD_LOGIC;
            Q : OUT std_logic );
    END COMPONENT;

    BEGIN
        U0: muxnto1 generic map ( n_addr => n_addr ) port map ( s => S, w => D, f => muxout );
        U1: dff port map ( D => muxout, clk => clk, nCLEAR => nCLEAR, Q => Q );
    END ideal;

```

```

-- *****
-- **** STUDENT: 64210455
-- *****
-- KOMENTARJI K OCENI NALOGE
-- Matej Možek: Ni pripomb
-- *****
LIBRARY ieee ;
USE ieee.std_logic_1164.all;

ENTITY muxdff IS
    generic( n_addr: natural := 2 ); -- stevilo naslovov ULM strukture
    PORT (
        S : in std_logic_vector( n_addr - 1 downto 0 );
        D : in std_logic_vector( 2**n_addr - 1 downto 0 ); -- vektor vhodov ULM strukture
        clk, -- signal ure ( prožen na sprednjo fronto )
        nCLEAR : IN std_logic; -- signal za asinhrono brisanje ( nCLEAR = '0' se postavi
Q=>'0' )
        Q : out std_logic -- izhod ULM strukture
    );
END muxdff;

ARCHITECTURE ideal OF muxdff IS
    signal muxout : std_logic;

    COMPONENT muxnto1 IS
        generic( n_addr: natural := 2 );
        PORT (
            s : in std_logic_vector( n_addr - 1 downto 0 );
            w : in std_logic_vector( 2**n_addr - 1 downto 0 );
            f : OUT STD_LOGIC
        );
    END COMPONENT;

    COMPONENT dff IS
        PORT (
            D, clk, nCLEAR : IN STD_LOGIC;
            Q : OUT std_logic );
    END COMPONENT;

    BEGIN
        U0: muxnto1 generic map ( n_addr => n_addr ) port map ( s => S, w => D, f => muxout );
        U1: dff port map ( D => muxout, clk => clk, nCLEAR => nCLEAR, Q => Q );
    END ideal;

```

```

-- *****
-- **** STUDENT: 64210457
-- *****
-- KOMENTARJI K OCENI NALOGE
-- Matej Možek: Ni pripomb
-- *****
LIBRARY ieee ;
USE ieee.std_logic_1164.all;

ENTITY muxdff IS
    generic( n_addr: natural := 2 ); -- stevilo naslovov ULM strukture
    PORT (
        S : in std_logic_vector( n_addr - 1 downto 0 );
        D : in      std_logic_vector( 2**n_addr - 1 downto 0 ); -- vektor vhodov ULM strukture
        clk, -- signal          ure ( prožen na sprednjo fronto )
        nCLEAR : IN std_logic; -- signal          za asinhrono brisanje ( nCLEAR = '0' se postavi
Q=>'0' )
        Q : out std_logic -- izhod ULM strukture
    );
END muxdff;

ARCHITECTURE ideal OF muxdff IS
    signal      muxout : std_logic;

    COMPONENT muxnto1 IS
        generic( n_addr: natural := 2 );
        PORT (
            s : in std_logic_vector( n_addr - 1 downto 0 );
            w : in      std_logic_vector( 2**n_addr - 1 downto 0 );
            f : OUT STD_LOGIC
        );
    END COMPONENT;

    COMPONENT dff IS
        PORT (
            D, clk, nCLEAR : IN STD_LOGIC;
            Q : OUT std_logic );
    END COMPONENT;

    BEGIN
        U0: muxnto1 generic map ( n_addr => n_addr ) port map ( s => S, w => D, f => muxout );
        U1: dff port map ( D => muxout, clk => clk, nCLEAR => nCLEAR, Q => Q );
    END ideal;

```

```

-- *****
-- **** STUDENT: 64240430
-- *****
-- KOMENTARJI K OCENI NALOGE
-- Matej Možek: Ni pripomb
-- *****
LIBRARY ieee ;
USE ieee.std_logic_1164.all;

ENTITY muxdff IS
    generic( n_addr: natural := 2 ); -- stevilo naslovov ULM strukture
    PORT (
        S : in std_logic_vector( n_addr - 1 downto 0 );
        D : in      std_logic_vector( 2**n_addr - 1 downto 0 ); -- vektor vhodov ULM strukture
        clk, -- signal          ure ( prožen na sprednjo fronto )
        nCLEAR : IN std_logic; -- signal          za asinhrono brisanje ( nCLEAR = '0' se postavi
Q=>'0' )
        Q : out std_logic -- izhod ULM strukture
    );
END muxdff;

ARCHITECTURE ideal OF muxdff IS
    signal      muxout : std_logic;

    COMPONENT muxnto1 IS
        generic( n_addr: natural := 2 );
        PORT (
            s : in std_logic_vector( n_addr - 1 downto 0 );
            w : in      std_logic_vector( 2**n_addr - 1 downto 0 );
            f : OUT STD_LOGIC
        );
    END COMPONENT;

    COMPONENT dff IS
        PORT (
            D, clk, nCLEAR : IN STD_LOGIC;
            Q : OUT std_logic );
    END COMPONENT;

BEGIN
    U0: muxnto1 generic map ( n_addr => n_addr ) port map ( s => S, w => D, f => muxout );
    U1: dff port map ( D => muxout, clk => clk, nCLEAR => nCLEAR, Q => Q );
END ideal;

```

```

-- *****
-- **** PREDLOGA VAJE
-- *****
-- KOMENTARJI K OCENI NALOGE
-- Matej Možek: Ni pripomb
-- *****
LIBRARY ieee ;
USE ieee.std_logic_1164.all;

ENTITY muxdff IS
    generic( n_addr: natural := 2 ); -- stevilo naslovov ULM strukture
    PORT (
        S : in std_logic_vector( n_addr - 1 downto 0 );
        D : in      std_logic_vector( 2**n_addr - 1 downto 0 ); -- vektor vhodov ULM strukture
        clk, -- signal          ure ( prožen na sprednjo fronto )
        nCLEAR : IN std_logic; -- signal          za asinhrono brisanje ( nCLEAR = '0' se postavi
Q=>'0' )
        Q : out std_logic -- izhod ULM strukture
    );
END muxdff;

ARCHITECTURE ideal OF muxdff IS
    signal      muxout : std_logic;

    COMPONENT muxnto1 IS
        generic( n_addr: natural := 2 );
        PORT (
            s : in std_logic_vector( n_addr - 1 downto 0 );
            w : in      std_logic_vector( 2**n_addr - 1 downto 0 );
            f : OUT STD_LOGIC
        );
    END COMPONENT;

    COMPONENT dff IS
        PORT (
            D, clk, nCLEAR : IN STD_LOGIC;
            Q : OUT std_logic );
    END COMPONENT;

    BEGIN
        U0: muxnto1 generic map ( n_addr => n_addr ) port map ( s => S, w => D, f => muxout );
        U1: dff port map ( D => muxout, clk => clk, nCLEAR => nCLEAR, Q => Q );
    END ideal;

```

