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```

>xst -ifn muxnto1.xst
Release 14.7 - xst P.20131013 (nt64)
Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.
--> Parameter TMPDIR set to ./xst/projnav.tmp
Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.23 secs

--> WARNING:Xst:3164 - Option "-debug" found multiple times in the command line. Only the first occurrence
*           HDL Compilation           *
Compiling vhdl file "/muxnto1.vhd" in Library work.
Entity <muxnto1> compiled.
Entity <muxnto1> (Architecture <>) compiled.
Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.29 secs

-->
Total memory usage is 4468956 kilobytes
Number of errors   : 0 ( 0 filtered)
Number of warnings : 1 ( 0 filtered)
Number of infos    : 0 ( 0 filtered)
>fuse -incremental -o muxnto1_tb_isim_beh.exe -prj muxnto1_tb.prj -top muxnto1__tb
ISim P.20131013 (signature 0x7708f090)
Number of CPUs detected in this system: 8
Turning on mult-threading, number of parallel sub-compilation jobs: 16
Determining compilation order of HDL files
Parsing VHDL file "muxnto1.vhd" into library work
Parsing VHDL file "muxnto1__tb.vhd" into library work
Starting static elaboration
Completed static elaboration
Compiling package standard
Compiling package std_logic_1164
Compiling package numeric_std
Compiling package textio
Compiling package std_logic_textio
Compiling architecture of entity muxnto1 [muxnto1(2)]
Compiling architecture of entity muxnto1__tb
Time Resolution for simulation is 1ps.
Waiting for 1 sub-compilation(s) to finish...
Compiled 8 VHDL Units
Built simulation executable muxnto1_tb_isim_beh.exe
Fuse Memory Usage: 36636 KB
Fuse CPU Usage: 827 ms
>muxnto1_tb_isim_beh.exe -tclbatch isim_muxnto1.tcl -wdb muxnto1_isim_beh.wdb
ISim P.20131013 (signature 0x7708f090)
WARNING: A WEBPACK license was found.
WARNING: Please use Xilinx License Configuration Manager to check out a full ISim license.
WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for more information on t
This is a Lite version of ISim.
Time resolution is 1 ps
Simulator is doing circuit initialization process.
Finished circuit initialization process.
>xst -ifn shift_reg.xst
Release 14.7 - xst P.20131013 (nt64)
Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.
--> Parameter TMPDIR set to ./xst/projnav.tmp
Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.22 secs

```

--> WARNING:Xst:3164 - Option "-debug" found multiple times in the command line. Only the first occurrence is used.

\* HDL Compilation \*

Compiling vhdl file "/muxnto1.vhd" in Library work.

Architecture of Entity muxnto1 is up to date.

Compiling vhdl file "/dff.vhd" in Library work.

Entity <dff> compiled.

Entity <dff> (Architecture <>) compiled.

Compiling vhdl file "/muxdff.vhd" in Library work.

Entity <muxdff> compiled.

Entity <muxdff> (Architecture <>) compiled.

Compiling vhdl file "/shift\_reg.vhd" in Library work.

Entity <shift\_reg> compiled.

Entity <shift\_reg> (Architecture <>) compiled.

Total REAL time to Xst completion: 0.00 secs

Total CPU time to Xst completion: 0.32 secs

-->

Total memory usage is 4468912 kilobytes

Number of errors : 0 ( 0 filtered)

Number of warnings : 1 ( 0 filtered)

Number of infos : 0 ( 0 filtered)

>fuse -incremental -o shift\_reg\_tb\_isim\_beh.exe -prj shift\_reg\_tb.prj -top shift\_reg\_tb

ISim P.20131013 (signature 0x7708f090)

Number of CPUs detected in this system: 8

Turning on mult-threading, number of parallel sub-compilation jobs: 16

Determining compilation order of HDL files

Parsing VHDL file "dff.vhd" into library work

Parsing VHDL file "muxnto1.vhd" into library work

Parsing VHDL file "muxdff.vhd" into library work

Parsing VHDL file "shift\_reg.vhd" into library work

Parsing VHDL file "shift\_reg\_\_tb.vhd" into library work

Starting static elaboration

Completed static elaboration

Compiling package standard

Compiling package std\_logic\_1164

Compiling package numeric\_std

Compiling package textio

Compiling package std\_logic\_textio

Compiling architecture of entity muxnto1 [muxnto1(2)]

Compiling architecture of entity dff [dff\_default]

Compiling architecture of entity muxdff [muxdff(2)]

Compiling architecture of entity shift\_reg [shift\_reg(4)]

Compiling architecture of entity shift\_reg\_\_tb

Time Resolution for simulation is 1ps.

Waiting for 1 sub-compilation(s) to finish...

Compiled 14 VHDL Units

Built simulation executable shift\_reg\_tb\_isim\_beh.exe

Fuse Memory Usage: 36908 KB

Fuse CPU Usage: 858 ms

>shift\_reg\_tb\_isim\_beh.exe -tclbatch isim\_shift\_reg.tcl -wdb shift\_reg\_tb\_isim\_beh.wdb

ISim P.20131013 (signature 0x7708f090)

WARNING: A WEBPACK license was found.

WARNING: Please use Xilinx License Configuration Manager to check out a full ISim license.

WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for more information on t

This is a Lite version of ISim.

Time resolution is 1 ps

WARNING: Simulation object /shift\_reg\_\_tb/comment was not traceable in the design for the following i

ISim does not yet support tracing of VHDL variables.

Simulator is doing circuit initialization process.

```

at 0 ps: Note: 0000000000000000 (/shift_reg__tb/UUT/).
Finished circuit initialization process.
at 0 ps: Note: 0000000000000000 (/shift_reg__tb/UUT/).
at 0 ps: Note: 0000000000000000 (/shift_reg__tb/UUT/).
at 20 ns(2): Note: 0000000000001000 (/shift_reg__tb/UUT/).
at 60 ns(2): Note: 0010000000001000 (/shift_reg__tb/UUT/).
at 70 ns(3): Note: 0010000001001001 (/shift_reg__tb/UUT/).
at 110 ns(3): Note: 0011001000001000 (/shift_reg__tb/UUT/).
at 130 ns(3): Note: 0111001100101000 (/shift_reg__tb/UUT/).
at 150 ns(3): Note: 0111011100111010 (/shift_reg__tb/UUT/).
at 170 ns(3): Note: 0111011101110111 (/shift_reg__tb/UUT/).
at 210 ns(3): Note: 0111011100111010 (/shift_reg__tb/UUT/).
at 230 ns(3): Note: 0111001100101000 (/shift_reg__tb/UUT/).
at 250 ns(3): Note: 0011001000001000 (/shift_reg__tb/UUT/).
at 270 ns(3): Note: 0010000000001000 (/shift_reg__tb/UUT/).

```

```
>xst -ifn fifo.xst
```

```
Release 14.7 - xst P.20131013 (nt64)
```

```
Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.
```

```
--> Parameter TMPDIR set to ./xst/projnav.tmp
```

```
Total REAL time to Xst completion: 0.00 secs
```

```
Total CPU time to Xst completion: 0.23 secs
```

```
--> WARNING:Xst:3164 - Option "-debug" found multiple times in the command line. Only the first occu
```

```
* HDL Compilation *
```

```
Compiling vhdl file "/muxnto1.vhd" in Library work.
```

```
Architecture of Entity muxnto1 is up to date.
```

```
Compiling vhdl file "/dff.vhd" in Library work.
```

```
Architecture of Entity dff is up to date.
```

```
Compiling vhdl file "/muxdff.vhd" in Library work.
```

```
Architecture of Entity muxdff is up to date.
```

```
Compiling vhdl file "/shift_reg.vhd" in Library work.
```

```
Architecture of Entity shift_reg is up to date.
```

```
Compiling vhdl file "/fifo.vhd" in Library work.
```

```
Entity <fifo> compiled.
```

```
Entity <fifo> (Architecture <>) compiled.
```

```
Total REAL time to Xst completion: 0.00 secs
```

```
Total CPU time to Xst completion: 0.34 secs
```

```
-->
```

```
Total memory usage is 4477092 kilobytes
```

```
Number of errors : 0 ( 0 filtered)
```

```
Number of warnings : 1 ( 0 filtered)
```

```
Number of infos : 0 ( 0 filtered)
```

```
>fuse -incremental -o fifo_tb_isim_beh.exe -prj fifo_tb.prj -top fifo__tb
```

```
ISim P.20131013 (signature 0x7708f090)
```

```
Number of CPUs detected in this system: 8
```

```
Turning on multi-threading, number of parallel sub-compilation jobs: 16
```

```
Determining compilation order of HDL files
```

```
Parsing VHDL file "dff.vhd" into library work
```

```
Parsing VHDL file "muxnto1.vhd" into library work
```

```
Parsing VHDL file "muxdff.vhd" into library work
```

```
Parsing VHDL file "shift_reg.vhd" into library work
```

```
Parsing VHDL file "fifo.vhd" into library work
```

```
Parsing VHDL file "fifo__tb.vhd" into library work
```

```
Starting static elaboration
```

```
Completed static elaboration
```

```
Compiling package standard
```

```
Compiling package std_logic_1164
```

```
Compiling package numeric_std
```

Compiling package textio  
Compiling package std\_logic\_textio  
Compiling architecture of entity muxnto1 [muxnto1(2)]  
Compiling architecture of entity dff [dff\_default]  
Compiling architecture of entity muxdff [muxdff(2)]  
Compiling architecture of entity shift\_reg [shift\_reg(8)]  
Compiling architecture of entity fifo [fifo(4,8)]  
Compiling architecture of entity fifo\_\_tb  
Time Resolution for simulation is 1ps.  
Waiting for 1 sub-compilation(s) to finish...  
Compiled 16 VHDL Units  
Built simulation executable fifo\_tb\_isim\_beh.exe  
Fuse Memory Usage: 37100 KB  
Fuse CPU Usage: 874 ms  
>fifo\_tb\_isim\_beh.exe -tclbatch isim\_fifo.tcl -wdb fifo\_tb\_isim\_beh.wdb  
ISim P.20131013 (signature 0x7708f090)  
WARNING: A WEBPACK license was found.  
WARNING: Please use Xilinx License Configuration Manager to check out a full ISim license.  
WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for more information on t  
This is a Lite version of ISim.  
Time resolution is 1 ps  
WARNING: Simulation object /fifo\_\_tb/comment was not traceable in the design for the following reason  
ISim does not yet support tracing of VHDL variables.  
Simulator is doing circuit initialization process.  
at 0 ps: Note: 00000000000000000000000000000000 (/fifo\_\_tb/UUT/).  
at 0 ps: Note: 00000000000000000000000000000000 (/fifo\_\_tb/UUT/I1(0)VU0/).  
at 0 ps, Instance /fifo\_\_tb/UUT/I1(0)VU0/I1(0)VU0/U0/ : Warning: NUMERIC\_STD.TO\_INTEGER: met  
at 0 ps, Instance /fifo\_\_tb/UUT/I1(0)VU0/I1(1)VU0/U0/ : Warning: NUMERIC\_STD.TO\_INTEGER: met  
at 0 ps, Instance /fifo\_\_tb/UUT/I1(0)VU0/I1(2)VU0/U0/ : Warning: NUMERIC\_STD.TO\_INTEGER: met  
at 0 ps, Instance /fifo\_\_tb/UUT/I1(0)VU0/I1(3)VU0/U0/ : Warning: NUMERIC\_STD.TO\_INTEGER: met  
at 0 ps, Instance /fifo\_\_tb/UUT/I1(0)VU0/I1(4)VU0/U0/ : Warning: NUMERIC\_STD.TO\_INTEGER: met  
at 0 ps, Instance /fifo\_\_tb/UUT/I1(0)VU0/I1(5)VU0/U0/ : Warning: NUMERIC\_STD.TO\_INTEGER: met  
at 0 ps, Instance /fifo\_\_tb/UUT/I1(0)VU0/I1(6)VU0/U0/ : Warning: NUMERIC\_STD.TO\_INTEGER: met  
at 0 ps, Instance /fifo\_\_tb/UUT/I1(0)VU0/I1(7)VU0/U0/ : Warning: NUMERIC\_STD.TO\_INTEGER: met  
at 0 ps: Note: 00000000000000000000000000000000 (/fifo\_\_tb/UUT/I1(1)VU0/).  
at 0 ps, Instance /fifo\_\_tb/UUT/I1(1)VU0/I1(0)VU0/U0/ : Warning: NUMERIC\_STD.TO\_INTEGER: met  
at 0 ps, Instance /fifo\_\_tb/UUT/I1(1)VU0/I1(1)VU0/U0/ : Warning: NUMERIC\_STD.TO\_INTEGER: met  
at 0 ps, Instance /fifo\_\_tb/UUT/I1(1)VU0/I1(2)VU0/U0/ : Warning: NUMERIC\_STD.TO\_INTEGER: met  
at 0 ps, Instance /fifo\_\_tb/UUT/I1(1)VU0/I1(3)VU0/U0/ : Warning: NUMERIC\_STD.TO\_INTEGER: met  
at 0 ps, Instance /fifo\_\_tb/UUT/I1(1)VU0/I1(4)VU0/U0/ : Warning: NUMERIC\_STD.TO\_INTEGER: met  
at 0 ps, Instance /fifo\_\_tb/UUT/I1(1)VU0/I1(5)VU0/U0/ : Warning: NUMERIC\_STD.TO\_INTEGER: met  
at 0 ps, Instance /fifo\_\_tb/UUT/I1(1)VU0/I1(6)VU0/U0/ : Warning: NUMERIC\_STD.TO\_INTEGER: met  
at 0 ps, Instance /fifo\_\_tb/UUT/I1(1)VU0/I1(7)VU0/U0/ : Warning: NUMERIC\_STD.TO\_INTEGER: met  
at 0 ps: Note: 00000000000000000000000000000000 (/fifo\_\_tb/UUT/I1(2)VU0/).  
at 0 ps, Instance /fifo\_\_tb/UUT/I1(2)VU0/I1(0)VU0/U0/ : Warning: NUMERIC\_STD.TO\_INTEGER: met  
at 0 ps, Instance /fifo\_\_tb/UUT/I1(2)VU0/I1(1)VU0/U0/ : Warning: NUMERIC\_STD.TO\_INTEGER: met  
at 0 ps, Instance /fifo\_\_tb/UUT/I1(2)VU0/I1(2)VU0/U0/ : Warning: NUMERIC\_STD.TO\_INTEGER: met  
at 0 ps, Instance /fifo\_\_tb/UUT/I1(2)VU0/I1(3)VU0/U0/ : Warning: NUMERIC\_STD.TO\_INTEGER: met  
at 0 ps, Instance /fifo\_\_tb/UUT/I1(2)VU0/I1(4)VU0/U0/ : Warning: NUMERIC\_STD.TO\_INTEGER: met  
at 0 ps, Instance /fifo\_\_tb/UUT/I1(2)VU0/I1(5)VU0/U0/ : Warning: NUMERIC\_STD.TO\_INTEGER: met  
at 0 ps, Instance /fifo\_\_tb/UUT/I1(2)VU0/I1(6)VU0/U0/ : Warning: NUMERIC\_STD.TO\_INTEGER: met  
at 0 ps, Instance /fifo\_\_tb/UUT/I1(2)VU0/I1(7)VU0/U0/ : Warning: NUMERIC\_STD.TO\_INTEGER: met  
at 0 ps: Note: 00000000000000000000000000000000 (/fifo\_\_tb/UUT/I1(3)VU0/).  
at 0 ps, Instance /fifo\_\_tb/UUT/I1(3)VU0/I1(0)VU0/U0/ : Warning: NUMERIC\_STD.TO\_INTEGER: met  
at 0 ps, Instance /fifo\_\_tb/UUT/I1(3)VU0/I1(1)VU0/U0/ : Warning: NUMERIC\_STD.TO\_INTEGER: met  
at 0 ps, Instance /fifo\_\_tb/UUT/I1(3)VU0/I1(2)VU0/U0/ : Warning: NUMERIC\_STD.TO\_INTEGER: met  
at 0 ps, Instance /fifo\_\_tb/UUT/I1(3)VU0/I1(3)VU0/U0/ : Warning: NUMERIC\_STD.TO\_INTEGER: met  
at 0 ps, Instance /fifo\_\_tb/UUT/I1(3)VU0/I1(4)VU0/U0/ : Warning: NUMERIC\_STD.TO\_INTEGER: met  
at 0 ps, Instance /fifo\_\_tb/UUT/I1(3)VU0/I1(5)VU0/U0/ : Warning: NUMERIC\_STD.TO\_INTEGER: met

[illegible]



at 230 ns(3): Note: 01010011001001000101001100100000 (/fifo\_\_tb/UUT/A1(1)VU0/).  
at 230 ns(3): Note: 00000100010101110111001100100000 (/fifo\_\_tb/UUT/A1(2)VU0/).  
at 230 ns(3): Note: 0000000000000000000010001010111 (/fifo\_\_tb/UUT/A1(3)VU0/).  
at 240 ns(2): Note: 01010011001001000101001100100100 (/fifo\_\_tb/UUT/A1(1)VU0/).  
at 240 ns(2): Note: 01000001011000010110000101100001 (/fifo\_\_tb/UUT/A1(0)VU0/).  
at 250 ns(3): Note: 00010110000101100001011000010010 (/fifo\_\_tb/UUT/A1(0)VU0/).  
at 250 ns(3): Note: 00000111011110001001100110101010 (/fifo\_\_tb/UUT/).  
at 250 ns(3): Note: 00010010010001010011001001000101 (/fifo\_\_tb/UUT/A1(1)VU0/).  
at 250 ns(3): Note: 01000101011101110011001000000000 (/fifo\_\_tb/UUT/A1(2)VU0/).  
at 250 ns(3): Note: 0000000000000000000100010101110111 (/fifo\_\_tb/UUT/A1(3)VU0/).  
at 260 ns(2): Note: 00010110000101100001011000010110 (/fifo\_\_tb/UUT/A1(0)VU0/).  
at 270 ns(3): Note: 01000001011000010110000101100101 (/fifo\_\_tb/UUT/A1(0)VU0/).  
at 270 ns(3): Note: 00001111111100000011001101010101 (/fifo\_\_tb/UUT/).  
at 270 ns(3): Note: 00000100010100110010010001010111 (/fifo\_\_tb/UUT/A1(1)VU0/).  
at 270 ns(3): Note: 01010111011100110010000000000000 (/fifo\_\_tb/UUT/A1(2)VU0/).  
at 270 ns(3): Note: 00000000000001000101011101110111 (/fifo\_\_tb/UUT/A1(3)VU0/).  
at 280 ns(2): Note: 01010111011100110010000000000100 (/fifo\_\_tb/UUT/A1(2)VU0/).  
at 280 ns(2): Note: 00000100010100110010010001010011 (/fifo\_\_tb/UUT/A1(1)VU0/).  
at 280 ns(2): Note: 01000001011000010110000101100001 (/fifo\_\_tb/UUT/A1(0)VU0/).  
at 290 ns(3): Note: 00010110000101100001011000010010 (/fifo\_\_tb/UUT/A1(0)VU0/).  
at 290 ns(3): Note: 00011111111000010110011010101010 (/fifo\_\_tb/UUT/).  
at 290 ns(3): Note: 01000101001100100100010100110010 (/fifo\_\_tb/UUT/A1(1)VU0/).  
at 290 ns(3): Note: 01010111001100100000000001000101 (/fifo\_\_tb/UUT/A1(2)VU0/).  
at 290 ns(3): Note: 00000000010001010111011101110111 (/fifo\_\_tb/UUT/A1(3)VU0/).  
at 300 ns(2): Note: 00010110000101100001011000010110 (/fifo\_\_tb/UUT/A1(0)VU0/).  
at 310 ns(3): Note: 01000001011000010110000101100101 (/fifo\_\_tb/UUT/A1(0)VU0/).  
at 310 ns(3): Note: 00111111111000011100110001010101 (/fifo\_\_tb/UUT/).  
at 310 ns(3): Note: 01010011001001000101001100100000 (/fifo\_\_tb/UUT/A1(1)VU0/).  
at 310 ns(3): Note: 01010011001000000000010001010111 (/fifo\_\_tb/UUT/A1(2)VU0/).  
at 310 ns(3): Note: 00000100010101110111011101110111 (/fifo\_\_tb/UUT/A1(3)VU0/).  
at 320 ns(2): Note: 01010011001001000101001100100100 (/fifo\_\_tb/UUT/A1(1)VU0/).  
at 320 ns(2): Note: 01000001011000010110000101100001 (/fifo\_\_tb/UUT/A1(0)VU0/).  
at 330 ns(3): Note: 00010110000101100001011000010010 (/fifo\_\_tb/UUT/A1(0)VU0/).  
at 330 ns(3): Note: 01111111100001111001100110101010 (/fifo\_\_tb/UUT/).  
at 330 ns(3): Note: 00010010010001010011001001000101 (/fifo\_\_tb/UUT/A1(1)VU0/).  
at 330 ns(3): Note: 0001001000000000000100010101110111 (/fifo\_\_tb/UUT/A1(2)VU0/).  
at 330 ns(3): Note: 01000101011101110111011101110111 (/fifo\_\_tb/UUT/A1(3)VU0/).  
at 340 ns(2): Note: 00010110000101100001011000010110 (/fifo\_\_tb/UUT/A1(0)VU0/).  
at 350 ns(3): Note: 01000001011000010110000101100101 (/fifo\_\_tb/UUT/A1(0)VU0/).  
at 350 ns(3): Note: 11111111000011110011001101010101 (/fifo\_\_tb/UUT/).  
at 350 ns(3): Note: 00000100010100110010010001010111 (/fifo\_\_tb/UUT/A1(1)VU0/).  
at 350 ns(3): Note: 00000000000001000101011101110111 (/fifo\_\_tb/UUT/A1(2)VU0/).  
at 350 ns(3): Note: 01010111011101110111011101110111 (/fifo\_\_tb/UUT/A1(3)VU0/).  
at 360 ns, Instance /fifo\_\_tb/: Warning: NUMERIC\_STD.TO\_UNSIGNED: vector truncated  
at 360 ns(2): Note: 01010111011101110111011101110011 (/fifo\_\_tb/UUT/A1(3)VU0/).  
at 360 ns(2): Note: 00000000000001000101011101110011 (/fifo\_\_tb/UUT/A1(2)VU0/).  
at 360 ns(2): Note: 00000100010100110010010001010011 (/fifo\_\_tb/UUT/A1(1)VU0/).  
at 360 ns(2): Note: 01000001011000010110000101100001 (/fifo\_\_tb/UUT/A1(0)VU0/).  
at 370 ns(3): Note: 00010110000101100001011000010010 (/fifo\_\_tb/UUT/A1(0)VU0/).  
at 370 ns(3): Note: 11111110000111100110011010101010 (/fifo\_\_tb/UUT/).  
at 370 ns(3): Note: 01000101001100100100010100110010 (/fifo\_\_tb/UUT/A1(1)VU0/).  
at 370 ns(3): Note: 00000000010001010111011100110010 (/fifo\_\_tb/UUT/A1(2)VU0/).  
at 370 ns(3): Note: 01010111011101110111011100110010 (/fifo\_\_tb/UUT/A1(3)VU0/).  
at 390 ns(3): Note: 01000001011000010110000100100000 (/fifo\_\_tb/UUT/A1(0)VU0/).  
at 390 ns(3): Note: 11111100001111001100110001010100 (/fifo\_\_tb/UUT/).  
at 390 ns(3): Note: 01010011001001000101001100100000 (/fifo\_\_tb/UUT/A1(1)VU0/).  
at 390 ns(3): Note: 00000100010101110111001100100000 (/fifo\_\_tb/UUT/A1(2)VU0/).  
at 390 ns(3): Note: 0101011101110111001100100000 (/fifo\_\_tb/UUT/A1(3)VU0/).  
at 410 ns(3): Note: 00010110000101100001001000000000 (/fifo\_\_tb/UUT/A1(0)VU0/).



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