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```

-- *****
-- **** STUDENT: 64000225
-- *****
-- KOMENTARJI K OCENI NALOGE
-- Matej Možek: Ni pripomb
-- *****

LIBRARY ieee;
USE ieee.std_logic_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
-- USE ieee.numeric_std.ALL;

ENTITY fifo_tb IS

    generic(
        fifo_width: natural := 4; -- dolžina vhodnega podatka
        fifo_size: natural := 8 ); -- število hranjenih podatkov

END fifo_tb;

ARCHITECTURE behavior OF fifo_tb IS

    -- Component Declaration for the Unit Under Test ( UUT )

    COMPONENT fifo
        generic(
            fifo_width: natural := 4; -- dolžina vhodnega podatka
            fifo_size: natural := 8 ); -- število hranjenih podatkov
        PORT(
            clk : IN std_logic;
            nCLR : IN std_logic;
            nEnable : IN std_logic;
            LOAD : IN std_logic;
            fifo_in : IN std_logic_vector( 3 downto 0 );
            fifo_out : OUT std_logic_vector( 3 downto 0 )
        );
    END COMPONENT;

    -- Inputs

```

```

signal      clk : std_logic := '0';
signal      nCLR : std_logic := '1';
signal      nEnable : std_logic := '1';
signal      LOAD : std_logic := '0';
signal      fifo_in : std_logic_vector( 3 downto 0 ) := ( others => '0' );

-- Outputs
signal      fifo_out : std_logic_vector( 3 downto 0 );

-- Clock period definitions
constant    clk_period : time := 10 ns;

BEGIN

    -- Instantiate the Unit Under Test ( UUT )
    uut: fifo
        GENERIC MAP ( fifo_width => fifo_width,          fifo_size => fifo_size )
        PORT MAP (
            clk => clk,
            nCLR => nCLR,
            nEnable => nEnable,
            LOAD => LOAD,
            fifo_in => fifo_in,
            fifo_out => fifo_out
        );

    -- Clock process definitions
    clk_process :process
    begin
        clk    <= '0';
        wait for clk_period/2;
        clk    <= '1';
        wait for clk_period/2;
    end process;

    -- Stimulus process
    stim_proc: process
    begin
        -- hold reset state for 100 ns.
        wait for 100 ns;

```

```

wait for clk_period*10;

    nEnable    <= '0';
    LOAD    <= '1';
    fifo_in    <= "0001";
    wait for clk_period;
    fifo_in    <= "0010";
    wait for clk_period;
    fifo_in    <= "0100";
    wait for clk_period;
    fifo_in    <= "1000";
    wait for clk_period;
    fifo_in    <= "0101";
    wait for clk_period;
    fifo_in    <= "0011";
    wait for clk_period;
    fifo_in    <= "1101";
    wait for clk_period;
    fifo_in    <= "1001";
    wait for clk_period;
    fifo_in    <= "0110";
    wait for clk_period;
    fifo_in    <= "0111";
    nENABLE    <= '1';
    wait for clk_period*3;
    nENABLE    <= '0';
    wait for clk_period;
    fifo_in    <= "0000";
    wait for clk_period*3;
    nCLR    <= '0';
    wait for clk_period;
    nCLR    <= '1';

wait;
end process;

END;

```

```

-- *****
-- **** STUDENT: 64200100
-- *****
-- KOMENTARJI K OCENI NALOGE
-- Matej Možek: Ni pripomb
-- *****
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;

ENTITY fifo_tb IS
    generic(
        fifo_width: natural := 4;
        fifo_size: natural := 8 );
END fifo_tb;

ARCHITECTURE behavior OF fifo_tb IS

    COMPONENT fifo
    generic(
        fifo_width: natural := 4;
        fifo_size: natural := 8 );
    PORT(
        clk : IN std_logic;
        nCLR : IN std_logic;
        nEnable : IN std_logic;
        LOAD : IN std_logic;
        fifo_in : IN std_logic_vector( 3 downto 0 );
        fifo_out : OUT std_logic_vector( 3 downto 0 ) );
    END COMPONENT;

    signal        clk : std_logic := '0';
    signal        nCLR : std_logic := '1';
    signal        nEnable : std_logic := '1';
    signal        LOAD : std_logic := '0';
    signal        fifo_in : std_logic_vector( 3 downto 0 ) := ( others => '0' );
    signal        fifo_out : std_logic_vector( 3 downto 0 );
    constant      clkP : time := 10 ns;

BEGIN
    uut: fifo
    GENERIC MAP ( fifo_width => fifo_width, fifo_size => fifo_size )
    PORT MAP (

```

```
clk => clk,  
nCLR => nCLR,  
nEnable => nEnable,  
LOAD => LOAD,  
fifo_in => fifo_in,  
fifo_out => fifo_out );
```

```
clk_process :process  
begin  
  clk    <= '0';  
  wait for clkP/2;  
  clk    <= '1';  
  wait for clkP/2;  
end process;
```

```
sproc: process  
begin  
  wait for 100 ns;  
  wait for clkP*10;  
  nEnable    <= '0';  
  LOAD    <= '1';  
  fifo_in    <= "0001";  
  wait for clkP;  
  fifo_in    <= "0010";  
  wait for clkP;  
  fifo_in    <= "0100";  
  wait for clkP;  
  fifo_in    <= "1000";  
  wait for clkP;  
  fifo_in    <= "0101";  
  wait for clkP;  
  fifo_in    <= "0011";  
  wait for clkP;  
  fifo_in    <= "1101";  
  wait for clkP;  
  fifo_in    <= "1001";  
  wait for clkP;  
  fifo_in    <= "0110";  
  wait for clkP;  
  fifo_in    <= "0111";
```

```
nENABLE      <= '1';  
wait for clkP*3;  
nENABLE      <= '0';  
wait for clkP;  
fifo_in      <= "0000";  
wait for clkP*3;  
nCLR         <= '0';  
wait for clkP;  
nCLR         <= '1';  
wait;  
end process;  
END;
```

```

-- *****
-- **** STUDENT: 64200163
-- *****
-- KOMENTARJI K OCENI NALOGE
-- Matej Možek: Ni pripomb
-- *****
library ieee;
use ieee.std_logic_1164.all;

entity fifo_tb is
    generic( fifo_width : natural := 4;
             fifo_size : natural := 8 );
end fifo_tb;

architecture behavior of fifo_tb is
    component fifo
        generic( fifo_width : natural := 4;
                 fifo_size : natural := 8 );
    port(
        clk : in std_logic;
        nCLR : in std_logic;
        nEnable : in std_logic;
        LOAD : in std_logic;
        fifo_in : in std_logic_vector( fifo_width - 1 downto 0 );
        fifo_out : out std_logic_vector( fifo_width - 1 downto 0 )
    );
    end component;
    signal        clk : std_logic := '0';
    signal        nCLR : std_logic := '1';
    signal        nEnable : std_logic := '1';
    signal        LOAD : std_logic := '0';
    signal        fifo_in : std_logic_vector( fifo_width - 1 downto 0 ) := ( others => '0' );
    signal        fifo_out : std_logic_vector( fifo_width - 1 downto 0 );
    constant      clk_period : time := 10 ns;
begin
    uut: fifo port map(
        clk => clk,
        nCLR => nCLR,
        nEnable => nEnable,
        LOAD => LOAD,

```



```

fifo_in => fifo_in,
fifo_out => fifo_out
    );
clk_process : process
begin
    clk    <= '0';
    wait for clk_period/2;
    clk    <= '1';
    wait for clk_period/2;
end process;
stim_proc : process
begin
    wait for clk_period*5;
    nEnable    <= '0';
    LOAD    <= '1';
    fifo_in    <= "0001";
    wait for clk_period;
    fifo_in    <= "0010";
    wait for clk_period;
    fifo_in    <= "0011";
    wait for clk_period;
    fifo_in    <= "0101";
    wait for clk_period;
    fifo_in    <= "0110";
    wait for clk_period;
    fifo_in    <= "0111";
    wait for clk_period;
    fifo_in    <= "1000";
    wait for clk_period;
    fifo_in    <= "1001";
    wait for clk_period;
    fifo_in    <= "1010";
    wait for clk_period;
    fifo_in    <= "1011";
    nENABLE    <= '1';
    wait for clk_period;
    nENABLE    <= '0';
    wait for clk_period;
    fifo_in    <= "1100";
    wait for clk_period*2.5;

```

```
        nCLR    <= '0';  
        wait for clk_period*5;  
        nCLR    <= '1';  
    end process;  
end;
```

```

-- *****
-- **** STUDENT: 64200238
-- *****
-- KOMENTARJI K OCENI NALOGE
-- Matej Možek: Ni pripomb
-- *****
--      --      --      --      --      --      --      --      --      --      --      --      --      --      --      --      --
--      --      --      --      --      --      --      --      --      --      --      --      --      --      --      --      --
--      --      --      --      --      --
-- Company:
-- Engineer:
--
-- Create Date: 17:16:46 12/22/2024
-- Design Name:
-- Module Name: C:/Users/Simon/Desktop/faks/NDS/4_domaca/FIFO/fifo_tb.vhd
-- Project Name: FIFO
-- Target Device:
-- Tool versions:
-- Description:
--
-- VHDL Test Bench Created by ISE for module: fifo
--
-- Dependencies:
--
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
--
-- Notes:
-- This testbench has been automatically generated using types std_logic and
-- std_logic_vector for the ports of the unit under test. Xilinx recommends
-- that these types always be used for the top-level I/O of a design in order
-- to guarantee that the testbench will bind correctly to the post-implementation
-- simulation model.
--      --      --      --      --      --      --      --      --      --      --      --      --      --      --      --      --
--      --      --      --      --      --      --      --      --      --      --      --      --      --      --      --      --
--      --      --      --      --      --
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;

```

```

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
USE ieee.numeric_std.ALL;

ENTITY fifo_tb IS
END fifo_tb;

ARCHITECTURE behavior OF fifo_tb IS

    -- Component Declaration for the Unit Under Test ( UUT )

    COMPONENT fifo
        generic(
            fifo_width: natural := 4; -- dolžina vhodnega podatka
            fifo_size: natural := 8 ); -- število hranjenih podatkov
    PORT(
        clk : IN std_logic;
        nCLR : IN std_logic;
        nEnable : IN std_logic;
        LOAD : IN std_logic;
        fifo_in : IN std_logic_vector( 3 downto 0 );
        fifo_out : OUT std_logic_vector( 3 downto 0 )
    );
    END COMPONENT;

    -- Inputs
    signal      clk : std_logic := '0';
    signal      nCLR : std_logic := '1';
    signal      nEnable : std_logic := '0';
    signal      LOAD : std_logic := '0';
    signal      fifo_in : std_logic_vector( 3 downto 0 ) := ( others => '0' );

    -- Outputs
    signal      fifo_out : std_logic_vector( 3 downto 0 );

    -- Clock period definitions
    constant    clk_period : time := 10 ns;

BEGIN

    -- Instantiate the Unit Under Test ( UUT )

```

```

uut: fifo PORT MAP (
clk => clk,
nCLR => nCLR,
nEnable => nEnable,
LOAD => LOAD,
fifo_in => fifo_in,
fifo_out => fifo_out
);

```

-- Clock process definitions

```

clk_process :process
begin
    clk    <= '0';
    wait for clk_period/2;
    clk    <= '1';
    wait for clk_period/2;
end process;

```

-- Stimulus process

```

stim_proc: process
BEGIN
    nEnable    <= '0';
    LOAD    <= '1';
    fifo_in    <= "0001";
    wait for clk_period;
    fifo_in    <= "0010";
    wait for clk_period;
    fifo_in    <= "0100";
    wait for clk_period;
    fifo_in    <= "1000";
    wait for clk_period;
    fifo_in    <= "0101";
    wait for clk_period;
    fifo_in    <= "0011";
    wait for clk_period;
    fifo_in    <= "1101";
    wait for clk_period;
    fifo_in    <= "1001";
    wait for clk_period;
    fifo_in    <= "0110";

```

```
wait for clk_period;  
fifo_in    <= "0111";  
nENABLE    <= '1';  
wait for clk_period*3;  
nENABLE    <= '0';  
wait for clk_period;  
fifo_in    <= "0000";  
wait for clk_period*3;  
nCLR       <= '0';  
wait for clk_period;  
nCLR       <= '1';
```

```
wait;  
END PROCESS;
```

```
END;
```

```

-- *****
-- **** STUDENT: 64200288
-- *****
-- KOMENTARJI K OCENI NALOGE
-- Matej Možek: Ni pripomb
-- *****
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;
USE ieee.numeric_std.ALL;

ENTITY fifo_tb IS
    generic(
        fifo_width: natural := 4;
        fifo_size: natural := 8 );
END fifo_tb;

ARCHITECTURE behavior OF fifo_tb IS

    COMPONENT fifo
        generic(
            fifo_width: natural := 4; -- dolžina vhodnega podatka
            fifo_size: natural := 8 ); -- število hranjenih podatkov
    PORT(
        clk : IN std_logic;
        nCLR : IN std_logic;
        nEnable : IN std_logic;
        LOAD : IN std_logic;
        fifo_in : IN std_logic_vector( 3 downto 0 );
        fifo_out : OUT std_logic_vector( 3 downto 0 )
    );
    END COMPONENT;

    signal
        clk : std_logic := '0';
        nCLR : std_logic := '1';
        nEnable : std_logic := '0';
        LOAD : std_logic := '0';
        fifo_in : std_logic_vector( 3 downto 0 ) := ( others => '0' );
        fifo_out : std_logic_vector( 3 downto 0 );

    constant    clk_period : time := 10 ns;

BEGIN

```

```

uut: fifo
PORT MAP (
clk => clk,
nCLR => nCLR,
nEnable => nEnable,
LOAD => LOAD,
fifo_in => fifo_in,
fifo_out => fifo_out
);

clk_process :process
begin
    clk    <= '0';
    wait for clk_period/2;
    clk    <= '1';
    wait for clk_period/2;
end process;

s_proc: process
BEGIN
    nEnable    <= '0';
    LOAD    <= '1';
    fifo_in    <= "0011";
    wait for clk_period;
    fifo_in    <= "0110";
    wait for clk_period;
    fifo_in    <= "1100";
    wait for clk_period;
    fifo_in    <= "1001";
    wait for clk_period;
    fifo_in    <= "0101";
    wait for clk_period;
    fifo_in    <= "1011";
    wait for clk_period;
    fifo_in    <= "1101";
    wait for clk_period;
    fifo_in    <= "1101";
    wait for clk_period;
    fifo_in    <= "0110";

```



```
wait for clk_period;  
fifo_in    <= "1101";  
nENABLE    <= '1';  
wait for clk_period*5;  
nENABLE    <= '0';  
wait for clk_period;  
fifo_in    <= "0000";  
wait for clk_period*5;  
nCLR       <= '0';  
wait for clk_period;  
nCLR       <= '1';  
wait;
```

```
END PROCESS;  
END;
```

```

-- *****
-- **** STUDENT: 64200296
-- *****
-- KOMENTARJI K OCENI NALOGE
-- Matej Možek: Ni pripomb
-- *****
--      --      --      --      --      --      --      --      --      --      --      --      --      --      --      --      --
--      --      --      --      --      --      --      --      --      --      --      --      --      --      --      --      --
--      --      --      --      --      --
-- Company:
-- Engineer:
--
-- Create Date: 21:22:03 12/21/2024
-- Design Name:
-- Module Name: C:/Users/Tim/Downloads/FIFO/FIFO/fifo_tb.vhd
-- Project Name: FIFO
-- Target Device:
-- Tool versions:
-- Description:
--
-- VHDL Test Bench Created by ISE for module: fifo
--
-- Dependencies:
--
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
--
-- Notes:
-- This testbench has been automatically generated using types std_logic and
-- std_logic_vector for the ports of the unit under test. Xilinx recommends
-- that these types always be used for the top-level I/O of a design in order
-- to guarantee that the testbench will bind correctly to the post-implementation
-- simulation model.
--      --      --      --      --      --      --      --      --      --      --      --      --      --      --      --      --
--      --      --      --      --      --      --      --      --      --      --      --      --      --      --      --      --
--      --      --      --      --      --
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;

```

```

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
-- USE ieee.numeric_std.ALL;

ENTITY fifo_tb IS
    generic(
        fifo_width: natural := 4; -- dolina vhodnega podatka
        fifo_size: natural := 8 ); -- teviló hranjenih podatkov
END fifo_tb;

ARCHITECTURE behavior OF fifo_tb IS

    -- Component Declaration for the Unit Under Test ( UUT )

    COMPONENT fifo
        generic(
            fifo_width: natural := 4; -- dolina vhodnega podatka
            fifo_size: natural := 8 ); -- teviló hranjenih podatkov
    PORT(
        clk : IN std_logic;
        nCLR : IN std_logic;
        nEnable : IN std_logic;
        LOAD : IN std_logic;
        fifo_in : IN std_logic_vector( 3 downto 0 );
        fifo_out : OUT std_logic_vector( 3 downto 0 )
    );
    END COMPONENT;

    -- Inputs
    signal      clk : std_logic := '0';
    signal      nCLR : std_logic := '1';
    signal      nEnable : std_logic := '1';
    signal      LOAD : std_logic := '0';
    signal      fifo_in : std_logic_vector( 3 downto 0 ) := ( others => '0' );

    -- Outputs
    signal      fifo_out : std_logic_vector( 3 downto 0 );

    -- Clock period definitions
    constant    clk_period : time := 10 ns;

BEGIN

```

```

    -- Instantiate the Unit Under Test ( UUT )
uut: fifo
    GENERIC MAP ( fifo_width => fifo_width,          fifo_size => fifo_size )
    PORT MAP (
clk => clk,
nCLR => nCLR,
nEnable => nEnable,
LOAD => LOAD,
fifo_in => fifo_in,
fifo_out => fifo_out
);

    -- Clock process definitions
clk_process :process
begin
    clk    <= '0';
    wait for clk_period/2;
    clk    <= '1';
    wait for clk_period/2;
end process;

    -- Stimulus process
stim_proc: process
begin
    -- hold reset state for 100 ns.
    wait for 100 ns;

    wait for clk_period*10;

    -- insert stimulus here
    nEnable    <= '0';
    LOAD    <= '1';
    fifo_in    <= "0001";
    wait for clk_period;
    fifo_in    <= "0010";
    wait for clk_period;
    fifo_in    <= "0011";
    wait for clk_period;
    fifo_in    <= "0100";

```

```
wait for clk_period;
fifo_in    <= "0101";
wait for clk_period;
fifo_in    <= "0110";
wait for clk_period;
fifo_in    <= "0111";
wait for clk_period;
fifo_in    <= "1000";
wait for clk_period*3;
fifo_in    <= "1001";
wait for clk_period;
fifo_in    <= "1010";
nENABLE    <= '1';
wait for clk_period*3;
fifo_in    <= "0000";
nENABLE    <= '0';
wait for clk_period*3;
nCLR       <= '0';
wait for clk_period;
nCLR       <= '1';

wait;
end process;

END;
```

```

-- *****
-- **** STUDENT: 64200385
-- *****
-- KOMENTARJI K OCENI NALOGE
-- Matej Možek: Ni pripomb
-- *****
-- TestBench Template

LIBRARY ieee;
USE ieee.std_logic_1164.ALL;
USE ieee.numeric_std.ALL;

ENTITY fifo_tb IS
    generic(
        fifo_width: natural := 4; -- dolžina vhodnega podatka
        fifo_size: natural := 8 );
END fifo_tb;

ARCHITECTURE behavior OF fifo_tb IS

    -- Component Declaration for the Unit Under Test ( UUT )

    COMPONENT fifo
        generic(
            fifo_width: natural := 4; -- dolžina vhodnega podatka
            fifo_size: natural := 8 );
    PORT(
        clk : IN std_logic;
        nCLR : IN std_logic;
        nEnable : IN std_logic;
        LOAD : IN std_logic;
        fifo_in : IN std_logic_vector( fifo_width - 1 downto 0 );
        fifo_out : OUT std_logic_vector( fifo_width - 1 downto 0 )
    );
    END COMPONENT;

    -- Inputs
    signal
        clk : std_logic := '0';
        nCLR : std_logic := '0';
        nEnable : std_logic := '0';
        LOAD : std_logic := '0';
        fifo_in : std_logic_vector( fifo_width - 1 downto 0 ) := ( others => '0' );

```

```

    -- Outputs
    signal          fifo_out : std_logic_vector( fifo_width - 1 downto 0 );

    -- Clock period definitions
    constant        clk_period : time := 10 ns;

BEGIN

    -- Instantiate the Unit Under Test ( UUT )
    uut: fifo PORT MAP (
        clk => clk,
        nCLR => nCLR,
        nEnable => nEnable,
        LOAD => LOAD,
        fifo_in => fifo_in,
        fifo_out => fifo_out
    );

    -- Clock process definitions
    clk_process :process
    begin
        clk    <= '0';
        wait for clk_period/2;
        clk    <= '1';
        wait for clk_period/2;
    end process;

    -- Stimulus process
    stim_proc: process
    begin
        -- hold reset state for 100 ns.
        wait for 100 ns;

        wait for clk_period*10;

        -- insert stimulus here
        fifo_in    <= "1001";
        wait for clk_period;
    end process;

```

```
nCLR    <= '1';
nEnable    <= '0';
LOAD    <= '1';
fifo_in    <= "0001";
wait for clk_period;

fifo_in    <= "0010";
wait for clk_period;

fifo_in    <= "0011";
wait for clk_period;

fifo_in    <= "0100";
wait for clk_period;

fifo_in    <= "0101";
wait for clk_period;

fifo_in    <= "0110";
wait for clk_period;

fifo_in    <= "1101";
wait for clk_period;

fifo_in    <= "1001";
wait for clk_period;

fifo_in    <= "0110";
wait for clk_period;

fifo_in    <= "0111";
nENABLE    <= '1';
wait for clk_period*3;

nENABLE    <= '0';
wait for clk_period;

fifo_in    <= "1111";
wait for clk_period*3;
```



```
nCLR   <= '0';  
fifo_in   <= "1100";  
wait for clk_period;
```

```
nCLR   <= '1';  
fifo_in   <= "1110";  
wait for clk_period;
```

```
wait;  
end process;
```

```
END;
```

```

-- *****
-- **** STUDENT: 64210113
-- *****
-- KOMENTARJI K OCENI NALOGE
-- Matej Možek: Ni pripomb
-- *****
--      --      --      --      --      --      --      --      --      --      --      --      --      --      --      --      --
--      --      --      --      --      --      --      --      --      --      --      --      --      --      --      --      --
--      --      --      --      --      --
-- Company:
-- Engineer:
--
-- Create Date: 12:23:47 12/18/2024
-- Design Name:
-- Module Name: C:/Users/Mihaheh/Downloads/Trash/FIFO/FIFO/fifo_tb.vhd
-- Project Name: FIFO
-- Target Device:
-- Tool versions:
-- Description:
--
-- VHDL Test Bench Created by ISE for module: fifo
--
-- Dependencies:
--
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
--
-- Notes:
-- This testbench has been automatically generated using types std_logic and
-- std_logic_vector for the ports of the unit under test. Xilinx recommends
-- that these types always be used for the top-level I/O of a design in order
-- to guarantee that the testbench will bind correctly to the post-implementation
-- simulation model.
--      --      --      --      --      --      --      --      --      --      --      --      --      --      --      --      --
--      --      --      --      --      --      --      --      --      --      --      --      --      --      --      --      --
--      --      --      --      --      --
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;

```

```

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
USE ieee.numeric_std.ALL;

ENTITY fifo_tb IS
generic( fifo_width: natural := 4;
         fifo_size: natural := 8 );
END fifo_tb;

ARCHITECTURE behavior OF fifo_tb IS

    -- Component Declaration for the Unit Under Test ( UUT )

    COMPONENT fifo
        generic( fifo_width: natural := 4;    -- dolžina vhodnega podatka
                 fifo_size: natural := 8 );
    PORT(
        clk : IN std_logic;
        nCLR : IN std_logic;
        nEnable : IN std_logic;
        LOAD : IN std_logic;
        fifo_in : IN std_logic_vector( 3 downto 0 );
        fifo_out : OUT std_logic_vector( 3 downto 0 )
    );
    END COMPONENT;

    -- Inputs
    signal      clk : std_logic := '0';
    signal      nCLR : std_logic := '1';
    signal      nEnable : std_logic := '1';
    signal      LOAD : std_logic := '0';
    signal      fifo_in : std_logic_vector( 3 downto 0 ) := ( others => '0' );

    -- Outputs
    signal      fifo_out : std_logic_vector( 3 downto 0 );

    -- Clock period definitions
    constant    clk_period : time := 10 ns;

BEGIN

```

```

    -- Instantiate the Unit Under Test ( UUT )
uut: fifo
    GENERIC MAP ( fifo_width => fifo_width,          fifo_size => fifo_size )
    PORT MAP (
clk => clk,
nCLR => nCLR,
nEnable => nEnable,
LOAD => LOAD,
fifo_in => fifo_in,
fifo_out => fifo_out
);

    -- Clock process definitions
clk_process :process
begin
    clk    <= '0';
    wait for clk_period/2;
    clk    <= '1';
    wait for clk_period/2;
end process;

    -- Stimulus process
stim_proc: process
begin
    -- hold reset state for 100 ns.
    wait for 100 ns;

    wait for clk_period*10;

    -- Initialize control signals and FIFO input
        nEnable    <= '0';
        LOAD    <= '1';

        fifo_in    <= "0000"; wait for clk_period;
        fifo_in    <= "0001"; wait for clk_period;
        fifo_in    <= "0010"; wait for clk_period;
        fifo_in    <= "0100"; wait for clk_period;
        fifo_in    <= "0101"; wait for clk_period;
        fifo_in    <= "0101"; wait for clk_period;
        fifo_in    <= "0011"; wait for clk_period;

```

```
fifo_in    <= "1101"; wait for clk_period;
fifo_in    <= "0110"; wait for clk_period;
fifo_in    <= "1111"; wait for clk_period;

nEnable    <= '1'; wait for clk_period * 2;
nEnable    <= '0'; wait for clk_period * 2;

fifo_in    <= "0000"; wait for clk_period * 4;
nCLR       <= '0'; wait for clk_period;
nCLR       <= '1'; wait for clk_period;
```

```
wait;
end process;
```

```
END;
```

```

-- *****
-- **** STUDENT: 64210132
-- *****
-- KOMENTARJI K OCENI NALOGE
-- Matej Možek: Ni pripomb
-- *****
--      --      --      --      --      --      --      --      --      --      --      --      --      --      --      --      --
--      --      --      --      --      --      --      --      --      --      --      --      --      --      --      --      --
--      --      --      --      --      --
-- Company:
-- Engineer:
--
-- Create Date: 04:02:24 12/23/2024
-- Design Name:
-- Module Name: C:/Users/blazk/Desktop/NDV/DN/fifo/fifo/fifo_tb.vhd
-- Project Name: fifo
-- Target Device:
-- Tool versions:
-- Description:
--
-- VHDL Test Bench Created by ISE for module: fifo
--
-- Dependencies:
--
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
--
-- Notes:
-- This testbench has been automatically generated using types std_logic and
-- std_logic_vector for the ports of the unit under test. Xilinx recommends
-- that these types always be used for the top-level I/O of a design in order
-- to guarantee that the testbench will bind correctly to the post-implementation
-- simulation model.
--      --      --      --      --      --      --      --      --      --      --      --      --      --      --      --      --
--      --      --      --      --      --      --      --      --      --      --      --      --      --      --      --      --
--      --      --      --      --      --
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;
use ieee.numeric_std.all;

```

```
-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
-- USE ieee.numeric_std.ALL;
```

```
ENTITY fifo_tb IS
END fifo_tb;
```

```
ARCHITECTURE behavior OF fifo_tb IS
```

```
    -- Component Declaration for the Unit Under Test ( UUT )
```

```
    COMPONENT fifo
    PORT(
        clk : IN std_logic;
        nCLR : IN std_logic;
        nEnable : IN std_logic;
        LOAD : IN std_logic;
        fifo_in : IN std_logic_vector( 3 downto 0 );
        fifo_out : OUT std_logic_vector( 3 downto 0 )
    );
    END COMPONENT;
```

```
    -- Inputs
```

```
    signal      clk : std_logic := '0';
    signal      nCLR : std_logic := '1';
    signal      nEnable : std_logic := '0';
    signal      LOAD : std_logic := '1';
    signal      fifo_in : std_logic_vector( 3 downto 0 ) := ( others => '0' );
```

```
    -- Outputs
```

```
    signal      fifo_out : std_logic_vector( 3 downto 0 );
```

```
    -- Clock period definitions
```

```
    constant    clk_period : time := 10 ns;
```

```
BEGIN
```

```
    -- Clock process definitions
```

```
    clk_process :process
```

```

begin
    clk    <= '0';
    wait for clk_period/2;
    clk    <= '1';
    wait for clk_period/2;
end process;

    -- Instantiate the Unit Under Test ( UUT )
 uut: fifo PORT MAP (
    clk => clk,
    nCLR => nCLR,
    nEnable => nEnable,
    LOAD => LOAD,
    fifo_in => fifo_in,
    fifo_out => fifo_out
  );

    -- Stimulus process
 stim_proc: process
 begin
    -- hold reset state for 100 ns.
    wait for 100 ns;
    -- insert stimulus here

    for i in 0 to 16 loop
        fifo_in    <= std_logic_vector( to_unsigned( i,4 ) );
        wait for clk_period;
    end loop;

    for i in 0 to 16 loop
        fifo_in    <= std_logic_vector( to_unsigned( i,4 ) );
        if( i > 4 ) then
            nCLR    <= '0';
        end if;
        wait for clk_period;
    end loop;

wait;
end process;

```


END;

```

-- *****
-- **** STUDENT: 64210290
-- *****
-- KOMENTARJI K OCENI NALOGE
-- Matej Možek: Ni pripomb
-- *****
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;
USE ieee.numeric_std.ALL;

ENTITY fifo_tb IS
END fifo_tb;

ARCHITECTURE behavior OF fifo_tb IS

    -- Component Declaration for the Unit Under Test ( UUT )

    COMPONENT fifo
    PORT(
        clk : IN std_logic;
        nCLR : IN std_logic;
        nEnable : IN std_logic;
        LOAD : IN std_logic;
        fifo_in : IN std_logic_vector( 3 downto 0 );
        fifo_out : OUT std_logic_vector( 3 downto 0 )
    );
    END COMPONENT;

    -- Inputs
    signal      clk : std_logic := '0';
    signal      nCLR : std_logic := '0';
    signal      nEnable : std_logic := '0';
    signal      LOAD : std_logic := '0';
    signal      fifo_in : std_logic_vector( 3 downto 0 ) := ( others => '0' );

    -- Outputs
    signal      fifo_out : std_logic_vector( 3 downto 0 );

    -- Clock period definitions
    constant    clk_period : time := 10 ns;

```

```
BEGIN
```

```
    -- Instantiate the Unit Under Test ( UUT )
```

```
    uut: fifo PORT MAP (  
        clk => clk,  
        nCLR => nCLR,  
        nEnable => nEnable,  
        LOAD => LOAD,  
        fifo_in => fifo_in,  
        fifo_out => fifo_out  
    );
```

```
    -- Clock process definitions
```

```
    clk_process :process  
    begin  
        clk    <= '0';  
        wait for clk_period/2;  
        clk    <= '1';  
        wait for clk_period/2;  
    end process;
```

```
    -- Stimulus process
```

```
    stim_proc: process  
    begin  
        -- hold reset state for 100 ns.  
        wait for 100 ns;  
  
        wait for clk_period*10;
```

```
        nCLR <= '1';  
        nEnable    <= '0';  
        LOAD  <= '1';  
        wait for clk_period;  
  
        fifo_in    <= "1010";  
        wait for clk_period;  
        fifo_in    <= "0101";  
        wait for clk_period;  
        fifo_in    <= "1010";
```

```
wait for clk_period;
fifo_in    <= "0101";
wait for clk_period;
fifo_in    <= "0000";
wait for clk_period*10;

for idi in 0 to 7 loop
    fifo_in    <= std_logic_vector( to_unsigned( idi, fifo_in'length ) );
    wait for clk_period;
end loop;
wait for clk_period*10;

nEnable    <= '1';
wait for clk_period;

fifo_in    <= "1010";
wait for clk_period;
fifo_in    <= "0101";
wait for clk_period;
fifo_in    <= "1010";
wait for clk_period;
fifo_in    <= "0101";
wait for clk_period;
```

```
wait;
end process;
```

```
END;
```

```
-- *****
-- **** STUDENT: 64210382
-- *****
-- KOMENTARJI K OCENI NALOGE
-- Matej Možek: Ni pripomb
-- *****
```

```
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;
```

```
ENTITY fifo_tb IS
    generic(
        fifo_width: natural := 4;
        fifo_size: natural := 8 );
    END fifo_tb;
```

```
ARCHITECTURE behavior OF fifo_tb IS
```

```
    COMPONENT fifo
        generic(
            fifo_width: natural := 4;
            fifo_size: natural := 8 );
```

```
    PORT(
        clk : IN std_logic;
        nCLR : IN std_logic;
        nEnable : IN std_logic;
        LOAD : IN std_logic;
        fifo_in : IN std_logic_vector( 3 downto 0 );
        fifo_out : OUT std_logic_vector( 3 downto 0 )
    );
    END COMPONENT;
```

```
    signal        clk : std_logic := '0';
    signal        nCLR : std_logic := '1';
    signal        nEnable : std_logic := '1';
    signal        LOAD : std_logic := '0';
    signal        fifo_in : std_logic_vector( 3 downto 0 ) := ( others => '0' );
```

```
    signal        fifo_out : std_logic_vector( 3 downto 0 );
```

```
    constant      clk_period : time := 10 ns;
```

BEGIN

```
uut: fifo
    GENERIC MAP ( fifo_width => fifo_width,          fifo_size => fifo_size )
    PORT MAP (
clk => clk,
nCLR => nCLR,
nEnable => nEnable,
LOAD => LOAD,
fifo_in => fifo_in,
fifo_out => fifo_out
);

clk_process :process
begin
    clk    <= '0';
    wait for clk_period/2;
    clk    <= '1';
    wait for clk_period/2;
end process;

stim_proc: process
begin
    wait for 100 ns;

    wait for clk_period*10;

    nEnable    <= '0';
    LOAD    <= '1';
    fifo_in    <= "0001";
    wait for clk_period;
    fifo_in    <= "0010";
    wait for clk_period;
    fifo_in    <= "0100";
    wait for clk_period;
    fifo_in    <= "1000";
    wait for clk_period;
    fifo_in    <= "0101";
    wait for clk_period;
    fifo_in    <= "0011";
```

```
wait for clk_period;
fifo_in    <= "1101";
wait for clk_period;
fifo_in    <= "1001";
wait for clk_period;
fifo_in    <= "0110";
wait for clk_period;
fifo_in    <= "0111";
nENABLE    <= '1';
wait for clk_period*3;
nENABLE    <= '0';
wait for clk_period;
fifo_in    <= "0000";
wait for clk_period*3;
nCLR       <= '0';
wait for clk_period;
nCLR       <= '1';

wait;
end process;

END;
```

```

-- *****
-- **** STUDENT: 64210384
-- *****
-- KOMENTARJI K OCENI NALOGE
-- Matej Možek: Ni pripomb
-- *****
--      --      --      --      --      --      --      --      --      --      --      --      --      --      --      --
--      --      --      --      --      --      --      --      --      --      --      --      --      --      --
--      --      --      --      --      --
-- Company:
-- Engineer:
--
-- Create Date: 21:05:25 12/20/2024
-- Design Name:
-- Module Name: C:/NDV/DN4/fifo_tb.vhd
-- Project Name: DN4
-- Target Device:
-- Tool versions:
-- Description:
--
-- VHDL Test Bench Created by ISE for module: fifo
--
-- Dependencies:
--
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
--
-- Notes:
-- This testbench has been automatically generated using types std_logic and
-- std_logic_vector for the ports of the unit under test. Xilinx recommends
-- that these types always be used for the top-level I/O of a design in order
-- to guarantee that the testbench will bind correctly to the post-implementation
-- simulation model.
--      --      --      --      --      --      --      --      --      --      --      --      --      --      --      --
--      --      --      --      --      --      --      --      --      --      --      --      --      --      --
--      --      --      --      --      --
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;

```



```

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
-- USE ieee.numeric_std.ALL;

ENTITY fifo_tb IS
    generic(
        fifo_width: natural := 4; -- dolžina vhodnega podatka
        fifo_size: natural := 8 ); -- število hranjenih podatkov
END fifo_tb;

ARCHITECTURE behavior OF fifo_tb IS

    -- Component Declaration for the Unit Under Test ( UUT )

    COMPONENT fifo
        generic( fifo_width: natural := 4;    -- dolžina vhodnega podatka
                 fifo_size: natural := 8 ); -- število hranjenih podatkov
    PORT(
        clk : IN std_logic;
        nCLR : IN std_logic;
        nEnable : IN std_logic;
        LOAD : IN std_logic;
        fifo_in : IN std_logic_vector( 3 downto 0 );
        fifo_out : OUT std_logic_vector( 3 downto 0 )
    );
    END COMPONENT;

    -- Inputs
    signal      clk : std_logic := '0';
    signal      nCLR : std_logic := '1';
    signal      nEnable : std_logic := '1';
    signal      LOAD : std_logic := '0';
    signal      fifo_in : std_logic_vector( 3 downto 0 ) := ( others => '0' );

    -- Outputs
    signal      fifo_out : std_logic_vector( 3 downto 0 );

    -- Clock period definitions
    constant    clk_period : time := 10 ns;

BEGIN

```

```

    -- Instantiate the Unit Under Test ( UUT )
uut: fifo
    GENERIC MAP ( fifo_width => fifo_width,          fifo_size => fifo_size )
    PORT MAP (
clk => clk,
nCLR => nCLR,
nEnable => nEnable,
LOAD => LOAD,
fifo_in => fifo_in,
fifo_out => fifo_out
);

    -- Clock process definitions
clk_process :process
begin
    clk    <= '0';
    wait for clk_period/2;
    clk    <= '1';
    wait for clk_period/2;
end process;

    -- Stimulus process
stim_proc: process
begin
    -- hold reset state for 100 ns.
    wait for 100 ns;

    wait for clk_period*10;

    -- insert stimulus here
    nEnable    <= '0';
    LOAD    <= '1';
    fifo_in    <= "0001";
    wait for clk_period;
    fifo_in    <= "0010";
    wait for clk_period;
    fifo_in    <= "0100";
    wait for clk_period;
    fifo_in    <= "1000";

```

```
wait for clk_period;
fifo_in    <= "0101";
wait for clk_period;
fifo_in    <= "0011";
wait for clk_period;
fifo_in    <= "1101";
wait for clk_period;
fifo_in    <= "1001";
wait for clk_period;
fifo_in    <= "0110";
wait for clk_period;
fifo_in    <= "0111";
nENABLE    <= '1';
wait for clk_period*3;
nENABLE    <= '0';
wait for clk_period;
fifo_in    <= "0000";
wait for clk_period*3;
nCLR       <= '0';
wait for clk_period;
nCLR       <= '1';

wait;
end process;

END;
```

```

-- *****
-- **** STUDENT: 64210386
-- *****
-- KOMENTARJI K OCENI NALOGE
-- Matej Možek: Ni pripomb
-- *****
--      --      --      --      --      --      --      --      --      --      --      --      --      --      --      --
--      --      --      --      --      --      --      --      --      --      --      --      --      --      --      --
--      --      --      --      --      --
-- Company:
-- Engineer:
--
-- Create Date: 20:16:02 12/16/2024
-- Design Name:
-- Module Name: /home/ise/Xilinx_shared/domaca_naloga_4/fifo_tb.vhd
-- Project Name: domaca_naloga_4
-- Target Device:
-- Tool versions:
-- Description:
--
-- VHDL Test Bench Created by ISE for module: fifo
--
-- Dependencies:
--
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
--
-- Notes:
-- This testbench has been automatically generated using types std_logic and
-- std_logic_vector for the ports of the unit under test. Xilinx recommends
-- that these types always be used for the top-level I/O of a design in order
-- to guarantee that the testbench will bind correctly to the post-implementation
-- simulation model.
--      --      --      --      --      --      --      --      --      --      --      --      --      --      --      --
--      --      --      --      --      --      --      --      --      --      --      --      --      --      --      --
--      --      --      --      --      --
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;

```

```
-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
-- USE ieee.numeric_std.ALL;
```

```
ENTITY fifo_tb IS
    generic(
        fifo_width: natural := 4; -- dolÅžina vhodnega podatka
        fifo_size: natural := 8 ); -- Å¡tevílo hranjenih podatkov
END fifo_tb;
```

```
ARCHITECTURE behavior OF fifo_tb IS
```

```
    -- Component Declaration for the Unit Under Test ( UUT )
```

```
    COMPONENT fifo
        generic(
            fifo_width: natural := 4; -- dolÅžina vhodnega podatka
            fifo_size: natural := 8 ); -- Å¡tevílo hranjenih podatkov
```

```
    PORT(
        clk : IN std_logic;
        nCLR : IN std_logic;
        nEnable : IN std_logic;
        LOAD : IN std_logic;
        fifo_in : IN std_logic_vector( fifo_width - 1 downto 0 );
        fifo_out : OUT std_logic_vector( fifo_width - 1 downto 0 )
    );
END COMPONENT;
```

```
    -- Inputs
```

```
    signal      clk : std_logic := '0';
    signal      nCLR : std_logic := '1';
    signal      nEnable : std_logic := '1';
    signal      LOAD : std_logic := '0';
    signal      fifo_in : std_logic_vector( fifo_width - 1 downto 0 ) := ( others => '0' );
```

```
    -- Outputs
```

```
    signal      fifo_out : std_logic_vector( fifo_width - 1 downto 0 );
```

```
    -- Clock period definitions
```

```
    constant    clk_period : time := 10 ns;
```

```
BEGIN
```

```

    -- Instantiate the Unit Under Test ( UUT )
    uut: fifo
        GENERIC MAP ( fifo_width => fifo_width,
                       PORT MAP (
clk => clk,
nCLR => nCLR,
nEnable => nEnable,
LOAD => LOAD,
fifo_in => fifo_in,
fifo_out => fifo_out
);

    -- Clock process definitions
    clk_process :process
begin
    clk    <= '0';
    wait for clk_period/2;
    clk    <= '1';
    wait for clk_period/2;
end process;

    -- Stimulus process
    stim_proc: process
begin
    -- hold reset state for 100 ns.
    wait for 100 ns;

    wait for clk_period*10;

    -- insert stimulus here
    nEnable    <= '0';
    LOAD    <= '1';
    fifo_in    <= "0001";
    wait for clk_period;
    fifo_in    <= "0010";
    wait for clk_period;
    fifo_in    <= "0100";
    wait for clk_period;
    fifo_in    <= "1000";

```

```
wait for clk_period;
fifo_in    <= "0101";
wait for clk_period;
fifo_in    <= "0011";
wait for clk_period;
fifo_in    <= "1101";
wait for clk_period;
fifo_in    <= "1001";
wait for clk_period;
fifo_in    <= "0110";
wait for clk_period;
fifo_in    <= "0111";
nENABLE    <= '1';
wait for clk_period*3;
nENABLE    <= '0';
wait for clk_period;
fifo_in    <= "0000";
wait for clk_period*3;
nCLR       <= '0';
wait for clk_period;
nCLR       <= '1';

wait;
end process;

END;
```

```

-- *****
-- **** STUDENT: 64210445
-- *****
-- KOMENTARJI K OCENI NALOGE
-- Matej Možek: Ni pripomb
-- *****
--      --      --      --      --      --      --      --      --      --      --      --      --      --      --      --
--      --      --      --      --      --      --      --      --      --      --      --      --      --      --      --
--      --      --      --      --      --
-- Company:
-- Engineer:
--
-- Create Date: 10:52:50 12/21/2024
-- Design Name:
-- Module Name: C:/UN-LJ/NDV/DVaja4/FIFO/fifo_tb.vhd
-- Project Name: FIFO
-- Target Device:
-- Tool versions:
-- Description:
--
-- VHDL Test Bench Created by ISE for module: fifo
--
-- Dependencies:
--
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
--
-- Notes:
-- This testbench has been automatically generated using types std_logic and
-- std_logic_vector for the ports of the unit under test. Xilinx recommends
-- that these types always be used for the top-level I/O of a design in order
-- to guarantee that the testbench will bind correctly to the post-implementation
-- simulation model.
--      --      --      --      --      --      --      --      --      --      --      --      --      --      --      --
--      --      --      --      --      --      --      --      --      --      --      --      --      --      --      --
--      --      --      --      --      --
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;

```



```
-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
-- USE ieee.numeric_std.ALL;
```

```
ENTITY fifo_tb IS
END fifo_tb;
```

```
ARCHITECTURE behavior OF fifo_tb IS
```

```
    -- Component Declaration for the Unit Under Test ( UUT )
```

```
    COMPONENT fifo
    PORT(
        clk : IN std_logic;
        nCLR : IN std_logic;
        nEnable : IN std_logic;
        LOAD : IN std_logic;
        fifo_in : IN std_logic_vector( 3 downto 0 );
        fifo_out : OUT std_logic_vector( 3 downto 0 )
    );
    END COMPONENT;
```

```
    -- Inputs
```

```
    signal      clk : std_logic := '0';
    signal      nCLR : std_logic := '0';
    signal      nEnable : std_logic := '0';
    signal      LOAD : std_logic := '0';
    signal      fifo_in : std_logic_vector( 3 downto 0 ) := ( others => '0' );
```

```
    -- Outputs
```

```
    signal      fifo_out : std_logic_vector( 3 downto 0 );
```

```
    -- Clock period definitions
```

```
    constant    clk_period : time := 10 ns;
```

```
BEGIN
```

```
    -- Instantiate the Unit Under Test ( UUT )
```

```
    uut: fifo PORT MAP (
        clk => clk,
```

```

nCLR => nCLR,
nEnable => nEnable,
LOAD => LOAD,
fifo_in => fifo_in,
fifo_out => fifo_out
);

    -- Clock process definitions
clk_process :process
begin
    clk    <= '0';
    wait for clk_period/2;
    clk    <= '1';
    wait for clk_period/2;
end process;

    -- Stimulus process
stim_proc: process
begin
    -- hold reset state for 100 ns.
    wait for 100 ns;

    -- insert stimulus here
nEnable    <= '0';
    LOAD    <= '1';
    nCLR    <= '0';
    wait for clk_period;

    nCLR    <= '1';

    fifo_in    <= "0001";
    wait for clk_period;

    fifo_in    <= "0010";
    wait for clk_period;

    fifo_in    <= "0100";
    wait for clk_period;

    fifo_in    <= "1000";

```

```
wait for clk_period;

fifo_in      <= "0101";
wait for clk_period;

fifo_in      <= "0011";
wait for clk_period;

fifo_in      <= "1101";
wait for clk_period;

fifo_in      <= "1001";
wait for clk_period;

fifo_in      <= "0110";
wait for clk_period;

fifo_in      <= "0111";
nENABLE      <= '1';
wait for clk_period;

nENABLE      <= '0';
wait for clk_period;

fifo_in      <= "0000";
wait for clk_period;
```

```
wait;
end process;
```

```
END;
```

```

-- *****
-- **** STUDENT: 64210455
-- *****
-- KOMENTARJI K OCENI NALOGE
-- Matej Možek: Ni pripomb
-- *****
--      --      --      --      --      --      --      --      --      --      --      --      --      --      --      --      --
--      --      --      --      --      --      --      --      --      --      --      --      --      --      --      --      --
--      --      --      --      --      --
-- Company:
-- Engineer:
--
-- Create Date: 20:10:53 11/28/2022
-- Design Name:
-- Module Name: C:/Users/Saso/Documents/Xilinx_Projects/dn4/FIFO/fifo_tb.vhd
-- Project Name: FIFO
-- Target Device:
-- Tool versions:
-- Description:
--
-- VHDL Test Bench Created by ISE for module: fifo
--
-- Dependencies:
--
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
--
-- Notes:
-- This testbench has been automatically generated using types std_logic and
-- std_logic_vector for the ports of the unit under test. Xilinx recommends
-- that these types always be used for the top-level I/O of a design in order
-- to guarantee that the testbench will bind correctly to the post-implementation
-- simulation model.
--      --      --      --      --      --      --      --      --      --      --      --      --      --      --      --      --
--      --      --      --      --      --      --      --      --      --      --      --      --      --      --      --      --
--      --      --      --      --      --
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;

```

```

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
-- USE ieee.numeric_std.ALL;

ENTITY fifo_tb IS
    generic(
        fifo_width: natural := 4; -- dolžina vhodnega podatka
        fifo_size: natural := 8 ); -- število hranjenih podatkov
END fifo_tb;

ARCHITECTURE behavior OF fifo_tb IS

    -- Component Declaration for the Unit Under Test ( UUT )

    COMPONENT fifo
        generic(
            fifo_width: natural := 4; -- dolžina vhodnega podatka
            fifo_size: natural := 8 ); -- število hranjenih podatkov
    PORT(
        clk : IN std_logic;
        nCLR : IN std_logic;
        nEnable : IN std_logic;
        LOAD : IN std_logic;
        fifo_in : IN std_logic_vector( 3 downto 0 );
        fifo_out : OUT std_logic_vector( 3 downto 0 )
    );
    END COMPONENT;

    -- Inputs
    signal      clk : std_logic := '0';
    signal      nCLR : std_logic := '1';
    signal      nEnable : std_logic := '1';
    signal      LOAD : std_logic := '0';
    signal      fifo_in : std_logic_vector( 3 downto 0 ) := ( others => '0' );

    -- Outputs
    signal      fifo_out : std_logic_vector( 3 downto 0 );

    -- Clock period definitions
    constant    clk_period : time := 10 ns;

BEGIN

```

```

    -- Instantiate the Unit Under Test ( UUT )
uut: fifo
    GENERIC MAP ( fifo_width => fifo_width,          fifo_size => fifo_size )
    PORT MAP (
clk => clk,
nCLR => nCLR,
nEnable => nEnable,
LOAD => LOAD,
fifo_in => fifo_in,
fifo_out => fifo_out
);

    -- Clock process definitions
clk_process :process
begin
    clk    <= '0';
    wait for clk_period/2;
    clk    <= '1';
    wait for clk_period/2;
end process;

    -- Stimulus process
stim_proc: process
begin
    -- hold reset state for 100 ns.
    wait for 100 ns;

    wait for clk_period*10;

    -- insert stimulus here
    nEnable    <= '0';
    LOAD    <= '1';
    fifo_in    <= "0001";
    wait for clk_period;
    fifo_in    <= "0010";
    wait for clk_period;
    fifo_in    <= "0100";
    wait for clk_period;
    fifo_in    <= "1000";

```

```
wait for clk_period;
fifo_in    <= "0101";
wait for clk_period;
fifo_in    <= "0011";
wait for clk_period;
fifo_in    <= "1101";
wait for clk_period;
fifo_in    <= "1001";
wait for clk_period;
fifo_in    <= "0110";
wait for clk_period;
fifo_in    <= "0111";
nENABLE    <= '1';
wait for clk_period*3;
nENABLE    <= '0';
wait for clk_period;
fifo_in    <= "0000";
wait for clk_period*3;
nCLR       <= '0';
wait for clk_period;
nCLR       <= '1';

wait;
end process;

END;
```

```

-- *****
-- **** STUDENT: 64210457
-- *****
-- KOMENTARJI K OCENI NALOGE
-- Matej Možek: Ni pripomb
-- *****

```

```

LIBRARY ieee;
USE ieee.std_logic_1164.ALL;

```

```

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
-- USE ieee.numeric_std.ALL;

```

```

ENTITY fifo_tb IS
    generic(
        fifo_width: natural := 4; -- dolina vhodnega podatka
        fifo_size: natural := 8 ); -- tevilno hranjenih podatkov
END fifo_tb;

```

```

ARCHITECTURE behavior OF fifo_tb IS

```

```

    -- Component Declaration for the Unit Under Test ( UUT )

```

```

    COMPONENT fifo
        generic(
            fifo_width: natural := 4; -- dolina vhodnega podatka
            fifo_size: natural := 8 ); -- tevilno hranjenih podatkov

```

```

    PORT(
        clk : IN std_logic;
        nCLR : IN std_logic;
        nEnable : IN std_logic;
        LOAD : IN std_logic;
        fifo_in : IN std_logic_vector( 3 downto 0 );
        fifo_out : OUT std_logic_vector( 3 downto 0 )
    );
END COMPONENT;

```

```

    -- Inputs

```

```

    signal clk : std_logic := '0';
    signal nCLR : std_logic := '1';
    signal nEnable : std_logic := '1';

```



```

signal          LOAD : std_logic := '0';
signal          fifo_in : std_logic_vector( 3 downto 0 ) := ( others => '0' );

    -- Outputs
signal          fifo_out : std_logic_vector( 3 downto 0 );

    -- Clock period definitions
constant       clk_period : time := 10 ns;

BEGIN

    -- Instantiate the Unit Under Test ( UUT )
    uut: fifo
        GENERIC MAP ( fifo_width => fifo_width,          fifo_size => fifo_size )
        PORT MAP (
            clk => clk,
            nCLR => nCLR,
            nEnable => nEnable,
            LOAD => LOAD,
            fifo_in => fifo_in,
            fifo_out => fifo_out
        );

    -- Clock process definitions
    clk_process :process
    begin
        clk    <= '0';
        wait for clk_period/2;
        clk    <= '1';
        wait for clk_period/2;
    end process;

    -- Stimulus process
    stim_proc: process
    begin
        -- hold reset state for 100 ns.
        wait for 100 ns;

        wait for clk_period*10;

```

```

-- insert stimulus here
    nEnable    <= '0';
    LOAD    <= '1';
    fifo_in    <= "0001";
    wait for clk_period;
    fifo_in    <= "0010";
    wait for clk_period;
    fifo_in    <= "0100";
    wait for clk_period;
    fifo_in    <= "1000";
    wait for clk_period;
    fifo_in    <= "0101";
    wait for clk_period;
    fifo_in    <= "0011";
    wait for clk_period;
    fifo_in    <= "1101";
    wait for clk_period;
    fifo_in    <= "1001";
    wait for clk_period;
    fifo_in    <= "0110";
    wait for clk_period;
    fifo_in    <= "0111";
    nENABLE    <= '1';
    wait for clk_period*3;
    nENABLE    <= '0';
    wait for clk_period;
    fifo_in    <= "0000";
    wait for clk_period*3;
    nCLR    <= '0';
    wait for clk_period;
    nCLR    <= '1';

wait;
end process;

END;

```

```

-- *****
-- **** STUDENT: 64240430
-- *****
-- KOMENTARJI K OCENI NALOGE
-- Matej Možek: Ni pripomb
-- *****
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;
use ieee.numeric_std.all;

ENTITY fifo_tb IS
    generic ( fifo_width : natural := 4;
              fifo_size : natural := 8 );
END fifo_tb;

ARCHITECTURE behavior OF fifo_tb IS

    -- Component Declaration for the Unit Under Test ( UUT )

    COMPONENT fifo
        generic ( fifo_width : natural := 4;
                  fifo_size : natural := 8 );
    PORT(
        clk : IN std_logic;
        nCLR : IN std_logic;
        nEnable : IN std_logic;
        LOAD : IN std_logic;
        fifo_in : IN std_logic_vector( fifo_width - 1 downto 0 );
        fifo_out : OUT std_logic_vector( fifo_width - 1 downto 0 )
    );
    END COMPONENT;

    -- Inputs
    -- signal
    signal      clk : std_logic := '0';
    signal      nCLR : std_logic := '1';
    signal      nEnable : std_logic := '1';
    signal      LOAD : std_logic := '0';
    signal      fifo_in : std_logic_vector( fifo_width - 1 downto 0 ) := ( others => '0' );

    -- Outputs

```

```

signal          fifo_out : std_logic_vector( fifo_width - 1 downto 0 );

    -- Clock period definitions
    signal      clock : std_logic;
    constant    clock_period : time := 100 ns;

BEGIN

    -- Instantiate the Unit Under Test ( UUT )
    uut: fifo PORT MAP (
    clk => clock,
    nCLR => nCLR,
    nEnable => nEnable,
    LOAD => LOAD,
    fifo_in => fifo_in,
    fifo_out => fifo_out
    );

    -- Clock process definitions
    clock_process : process
    begin
        clock <= '0';
        wait for clock_period/2;
        clock <= '1';
        wait for clock_period/2;
    end process;

    -- Stimulus process
    stimulus_process: process
    begin

        -- wait for 100 ns;
        -- case s = 10
        nEnable    <= '0';
        LOAD       <= '1';
        for i in 0 to 1 loop
            for j in 0 to 1 loop
                -- testiramo vrednosti od 1 do 13
                -- testiramo slucajeve nEnable  <= '0' in LOAD      <= '1'
                -- testiramo slucajeve nEnable  <= '0' in LOAD      <= '0'
            end loop;
        end loop;
    end process;

```

```

-- testiramo slucajeve nEnable  <= '1' in LOAD      <= '1'
-- testiramo slucajeve nEnable  <= '1' in LOAD      <= '0'
    for k in 1 + i to 13 loop
        fifo_in      <= std_logic_vector( to_unsigned( k, fifo_in'length ) );
        wait for clock_period;
    end loop;
    LOAD  <= not LOAD;
    end loop;
    nEnable      <= not nEnable;
end loop;
nCLR  <= not nCLR;
wait;
end process;

END;

```

