

ERROR:HDLParers:164 - "64000225/cpu\_datapath.vhd" Line 128. parse error, unexpected END  
ERROR:HDLParers:850 - "64200100/cpu\_datapath.vhd" Line 78. Formal port desS does not exist in C  
ERROR:HDLParers:3010 - "64210455/cpu\_datapath.vhd" Line 1. Entity cpu\_datapath does not exist.  
ERROR:HDLParers:3312 - "64210455/cpu\_datapath.vhd" Line 2. Undefined symbol 'std\_logic\_vector'  
ERROR:HDLParers:1209 - "64210455/cpu\_datapath.vhd" Line 2. std\_logic\_vector: Undefined symbol  
ERROR:HDLParers:3312 - "64210455/cpu\_datapath.vhd" Line 2. Undefined symbol 'reg\_width'.  
ERROR:HDLParers:1209 - "64210455/cpu\_datapath.vhd" Line 2. reg\_width: Undefined symbol (last re  
ERROR:HDLParers:3312 - "64210455/cpu\_datapath.vhd" Line 3. Undefined symbol 'mux\_vector\_arra  
ERROR:HDLParers:1209 - "64210455/cpu\_datapath.vhd" Line 3. mux\_vector\_array\_type: Undefined :  
ERROR:HDLParers:842 - "64210455/cpu\_datapath.vhd" Line 3. The type of the element in aggregate  
ERROR:HDLParers:3312 - "64210455/cpu\_datapath.vhd" Line 4. Undefined symbol 'muxnto1\_bus\_ty  
ERROR:HDLParers:1209 - "64210455/cpu\_datapath.vhd" Line 4. muxnto1\_bus\_type: Undefined symt  
ERROR:HDLParers:842 - "64210455/cpu\_datapath.vhd" Line 4. The type of the element in aggregate  
ERROR:HDLParers:3312 - "64210455/cpu\_datapath.vhd" Line 12. Undefined symbol 'muxnto1\_bus'.  
ERROR:HDLParers:3312 - "64210455/cpu\_datapath.vhd" Line 14. Undefined symbol 'MB\_vector'.  
ERROR:HDLParers:1209 - "64210455/cpu\_datapath.vhd" Line 14. MB\_vector: Undefined symbol (last  
ERROR:HDLParers:3312 - "64210455/cpu\_datapath.vhd" Line 14. Undefined symbol 'b\_mux\_2d\_bit\_  
ERROR:HDLParers:1209 - "64210455/cpu\_datapath.vhd" Line 14. b\_mux\_2d\_bit\_array: Undefined sy  
ERROR:HDLParers:3312 - "64210455/cpu\_datapath.vhd" Line 15. Undefined symbol 'B\_muxed'.  
ERROR:HDLParers:1209 - "64210455/cpu\_datapath.vhd" Line 15. B\_muxed: Undefined symbol (last  
ERROR:HDLParers:1209 - "64210455/cpu\_datapath.vhd" Line 19. muxnto1\_bus: Undefined symbol (l  
ERROR:HDLParers:3312 - "64210455/cpu\_datapath.vhd" Line 21. Undefined symbol 'MD\_vector'.  
ERROR:HDLParers:1209 - "64210455/cpu\_datapath.vhd" Line 21. MD\_vector: Undefined symbol (las  
ERROR:HDLParers:3312 - "64210455/cpu\_datapath.vhd" Line 21. Undefined symbol 'd\_mux\_2d\_bit\_  
ERROR:HDLParers:1209 - "64210455/cpu\_datapath.vhd" Line 21. d\_mux\_2d\_bit\_array: Undefined sy  
ERROR:HDLParers:3312 - "64210455/cpu\_datapath.vhd" Line 22. Undefined symbol 'D\_data'.  
ERROR:HDLParers:1209 - "64210455/cpu\_datapath.vhd" Line 22. D\_data: Undefined symbol (last rep  
ERROR:HDLParers:3312 - "64210455/cpu\_datapath.vhd" Line 26. Undefined symbol 'ndn\_alu'.  
ERROR:HDLParers:3312 - "64210455/cpu\_datapath.vhd" Line 28. Undefined symbol 'ALU\_mode'.  
ERROR:HDLParers:1209 - "64210455/cpu\_datapath.vhd" Line 28. ALU\_mode: Undefined symbol (las  
ERROR:HDLParers:3312 - "64210455/cpu\_datapath.vhd" Line 28. Undefined symbol 'ALU\_function'.  
ERROR:HDLParers:1209 - "64210455/cpu\_datapath.vhd" Line 28. ALU\_function: Undefined symbol (l  
ERROR:HDLParers:3312 - "64210455/cpu\_datapath.vhd" Line 28. Undefined symbol 'A\_data'.  
ERROR:HDLParers:1209 - "64210455/cpu\_datapath.vhd" Line 28. A\_data: Undefined symbol (last rep  
ERROR:HDLParers:3312 - "64210455/cpu\_datapath.vhd" Line 28. Undefined symbol 'ALU\_result'.  
ERROR:HDLParers:1209 - "64210455/cpu\_datapath.vhd" Line 28. ALU\_result: Undefined symbol (las  
ERROR:HDLParers:3312 - "64210455/cpu\_datapath.vhd" Line 29. Undefined symbol 'ALU\_N\_bit'.  
ERROR:HDLParers:1209 - "64210455/cpu\_datapath.vhd" Line 29. ALU\_N\_bit: Undefined symbol (las  
ERROR:HDLParers:3312 - "64210455/cpu\_datapath.vhd" Line 29. Undefined symbol 'ALU\_C\_bit'.  
ERROR:HDLParers:1209 - "64210455/cpu\_datapath.vhd" Line 29. ALU\_C\_bit: Undefined symbol (las  
ERROR:HDLParers:3312 - "64210455/cpu\_datapath.vhd" Line 29. Undefined symbol 'ALU\_V\_bit'.  
ERROR:HDLParers:1209 - "64210455/cpu\_datapath.vhd" Line 29. ALU\_V\_bit: Undefined symbol (last  
ERROR:HDLParers:3312 - "64210455/cpu\_datapath.vhd" Line 30. Undefined symbol 'ALU\_Z\_bit'.  
ERROR:HDLParers:1209 - "64210455/cpu\_datapath.vhd" Line 30. ALU\_Z\_bit: Undefined symbol (last  
ERROR:HDLParers:3312 - "64210455/cpu\_datapath.vhd" Line 33. Undefined symbol 'Address\_out'.  
ERROR:HDLParers:3312 - "64210455/cpu\_datapath.vhd" Line 34. Undefined symbol 'Data\_out'.

Component 'reg\_file'.

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y\_type'.  
symbol (last report in this block)  
does not correspond to any array type.  
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does not correspond to any array type.

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```

>xst -ifn cpu_datapath.xst
Release 14.7 - xst P.20131013 (nt64)
Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.
--> Parameter TMPDIR set to ./xst/projnav.tmp
Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.44 secs

--> WARNING:Xst:3164 - Option "-debug" found multiple times in the command line. Only the first occurrence
*          HDL Compilation          *
Compiling vhdl file "/muxnto1.vhd" in Library work.
Entity <muxnto1> compiled.
Entity <muxnto1> (Architecture <>) compiled.
Compiling vhdl file "/dff.vhd" in Library work.
Entity <dff> compiled.
Entity <dff> (Architecture <>) compiled.
Compiling vhdl file "/cla_gp.vhd" in Library work.
Entity <cla_gp> compiled.
Entity <cla_gp> (Architecture <>) compiled.
Compiling vhdl file "/muxdff.vhd" in Library work.
Entity <muxdff> compiled.
Entity <muxdff> (Architecture <>) compiled.
Compiling vhdl file "/reg_file_functions.vhd" in Library work.
Package <reg_file_functions> compiled.
Package body <reg_file_functions> compiled.
Compiling vhdl file "/cla_add_n_bit.vhd" in Library work.
Entity <cla_add_n_bit> compiled.
Entity <cla_add_n_bit> (Architecture <>) compiled.
Compiling vhdl file "/dmuxnto1.vhd" in Library work.
Entity <dmuxnto1> compiled.
Entity <dmuxnto1> (Architecture <>) compiled.
Compiling vhdl file "/muxnto1_bus.vhd" in Library work.
Entity <muxnto1_bus> compiled.
Entity <muxnto1_bus> (Architecture <>) compiled.
Compiling vhdl file "/shift_reg.vhd" in Library work.
Entity <shift_reg> compiled.
Entity <shift_reg> (Architecture <>) compiled.
Compiling vhdl file "/cpu_datapath_functions.vhd" in Library work.
Package <cpu_datapath_functions> compiled.
Compiling vhdl file "/reg_file.vhd" in Library work.
Entity <reg_file> compiled.
Entity <reg_file> (Architecture <>) compiled.
Compiling vhdl file "/ndn_alu_cla.vhd" in Library work.
Entity <ndn_alu> compiled.
Entity <ndn_alu> (Architecture <>) compiled.
Compiling vhdl file "/cpu_datapath.vhd" in Library work.
Entity <cpu_datapath> compiled.
Entity <cpu_datapath> (Architecture <>) compiled.
Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.69 secs

-->
Total memory usage is 4477104 kilobytes
Number of errors   : 0 ( 0 filtered)
Number of warnings : 1 ( 0 filtered)
Number of infos    : 0 ( 0 filtered)
>fuse -incremental -o cpu_datapath_tb_isim_beh.exe -prj cpu_datapath_tb.prj -top cpu_datapath_tb
ISim P.20131013 (signature 0x7708f090)
Number of CPUs detected in this system: 8

```

Turning on mult-threading, number of parallel sub-compilation jobs: 16  
 Determining compilation order of HDL files  
 Parsing VHDL file "reg\_file\_functions.vhd" into library work  
 Parsing VHDL file "dff.vhd" into library work  
 Parsing VHDL file "dmuxnto1.vhd" into library work  
 Parsing VHDL file "muxnto1.vhd" into library work  
 Parsing VHDL file "muxdff.vhd" into library work  
 Parsing VHDL file "muxnto1\_bus.vhd" into library work  
 Parsing VHDL file "cla\_gp.vhd" into library work  
 Parsing VHDL file "cla\_add\_n\_bit.vhd" into library work  
 Parsing VHDL file "ndn\_alu\_cla.vhd" into library work  
 Parsing VHDL file "reg\_file\_\_logging.vhd" into library work  
 Parsing VHDL file "reg\_file\_functions.vhd" into library work  
 Parsing VHDL file "shift\_reg.vhd" into library work  
 Parsing VHDL file "cpu\_datapath\_functions.vhd" into library work  
 Parsing VHDL file "cpu\_datapath.vhd" into library work  
 Parsing VHDL file "cpu\_datapath\_tb.vhd" into library work  
 Starting static elaboration  
 Completed static elaboration  
 Compiling package standard  
 Compiling package std\_logic\_1164  
 Compiling package numeric\_std  
 Compiling package textio  
 Compiling package reg\_file\_functions  
 Compiling package cpu\_datapath\_functions  
 Compiling package std\_logic\_textio  
 Compiling package math\_real  
 Compiling package std\_logic\_arith  
 Compiling package std\_logic\_unsigned  
 Compiling architecture of entity dmuxnto1 [dmuxnto1(3)]  
 Compiling architecture of entity muxnto1 [muxnto1(3)]  
 Compiling architecture of entity muxnto1\_bus [muxnto1\_bus(3,16)]  
 Compiling architecture of entity muxnto1 [muxnto1(2)]  
 Compiling architecture of entity dff [dff\_default]  
 Compiling architecture of entity muxdff [muxdff(2)]  
 Compiling architecture of entity shift\_reg [shift\_reg(16)]  
 Compiling architecture of entity reg\_file [reg\_file(8,16)]  
 Compiling architecture of entity muxnto1 [muxnto1(1)]  
 Compiling architecture of entity muxnto1\_bus [muxnto1\_bus(1,16)]  
 Compiling architecture of entity cla\_gp [cla\_gp\_default]  
 Compiling architecture of entity cla\_add\_n\_bit [cla\_add\_n\_bit(16)]  
 Compiling architecture of entity ndn\_alu [ndn\_alu(16)]  
 Compiling architecture of entity cpu\_datapath [cpu\_datapath(8,16)]  
 Compiling architecture of entity cpu\_datapath\_tb  
 Time Resolution for simulation is 1ps.  
 Waiting for 3 sub-compilation(s) to finish...  
 Compiled 39 VHDL Units  
 Built simulation executable cpu\_datapath\_tb\_isim\_beh.exe  
 Fuse Memory Usage: 40056 KB  
 Fuse CPU Usage: 1421 ms  
 >cpu\_datapath\_tb\_isim\_beh.exe -tclbatch isim.tcl -wdb cpu\_datapath\_tb\_isim\_beh.wdb  
 ISim P.20131013 (signature 0x7708f090)  
 WARNING: A WEBPACK license was found.  
 WARNING: Please use Xilinx License Configuration Manager to check out a full ISim license.  
 WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for more information on t  
 This is a Lite version of ISim.  
 Time resolution is 1 ps  
 Simulator is doing circuit initialization process.  
 at 0 ps: Note: clkctrl\_wordRWDAABAMBMDALU\_mode ALU\_functionNCVZConst\_inData\_inAddress\_

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at 300 ns(1): Note: REG FILE:00000000 (/cpu\_datapath\_tb/UUT/REG\_FILE1/).

at 700 ns(1): Note: REG FILE:00000000 REG FILE:00000000 (/cpu\_datapath\_tb/UUT/REG\_FILE1/).

at 800 ns: Note: 10x000000x00x00x00x00x00x000000x00010x000B0x00000x0000RESET (/cpu\_datapath\_

at 1100 ns(1): Note: REG FILE:00000000 REG FILE:00000000 REG FILE:00000000 (/cpu\_datapath\_tb/

at 1200 ns: Note: 10x001B10x00x00x0010x600000x00010x000B0x000B0x000BLOAD R(0) <= MEM(R

at 1500 ns(1): Note: REG FILE:00000000 REG FILE:00000000 REG FILE:00000000 REG FILE:00000000

at 1600 ns: Note: 10x805B10x40x00x0110x600000x00010x00160x000B0x0001LOAD R(4) <= MEM(R

at 1900 ns(1): Note: REG FILE:00000000 REG FILE:00000000 REG FILE:00000000 REG FILE:00000000

at 2 us: Note: 10xA20110x50x00x4000x000000x00010x00160x000B0x0016ADD R(5) <= R(0) + R(4) (/

at 2300 ns(1): Note: REG FILE:00000000 REG FILE:00000000 REG FILE:00000000 REG FILE:00000000

at 2400 ns: Note: 10xD04110x60x40x0100x000000x001B0x00160x00160x001BADI R(6) <= R(4) + Co

at 2700 ns(1): Note: REG FILE:00000000 REG FILE:00000000 REG FILE:00000000 REG FILE:00000000

at 2800 ns: Note: 10xF03910x70x40x0000xE00000x001B0x00160x00160x000BMOVE A R(7) <= R(4) )

at 3100 ns(1): Note: REG FILE:00000000 REG FILE:00000000 REG FILE:00000000 REG FILE:00000000

at 3200 ns: Note: 10x63BD10x30x00x7000xF00000x001B0x00160x000B0x0016MOVE B R(3) <= R(7)

at 3500 ns(1): Note: REG FILE:00000000 REG FILE:00000000 REG FILE:00000000 REG FILE:00000000

at 3600 ns: Note: 10x0F9800x00x30x7000x600000x001B0x00160x00160x0016STORE B MEM(R(3)) <

at 3900 ns(1): Note: REG FILE:00000000 REG FILE:00000000 REG FILE:00000000 REG FILE:00000000

at 4 us: Note: 10x0FD800x00x30x7100x600000x005F0x00160x00160x005FSTORE CONST MEM(R(3

at 4300 ns(1): Note: REG FILE:00000000 REG FILE:00000000 REG FILE:00000000 REG FILE:00000000

at 4400 ns: Note: 10x044000x00x10x0100x000010x00000x00160x00000x0000TEST R(1) using bus A:

at 4700 ns(1): Note: REG FILE:00000000 REG FILE:00000000 REG FILE:00000000 REG FILE:00000000

at 4800 ns: Note: 10xD23110x60x40x4000xC00000x00000x00160x00160x0016R(6) <= R(4) xor R(4) (

at 5100 ns(1): Note: REG FILE:00000000 REG FILE:00000000 REG FILE:00000000 REG FILE:00000000

at 5200 ns: Note: 10xC4F800x60x10x1100xE00010x00000x00160x00000x0000TEST R(1) using bus A

at 5500 ns(1): Note: REG FILE:00000000 REG FILE:00000000 REG FILE:00000000 REG FILE:00000000

at 5600 ns: Note: 10xFFCD10x70x70x7100x301000x005F0x00160x00150x005FR(7) <= R(7) - 1 (/cpu\_

at 5900 ns(1): Note: REG FILE:00000000 REG FILE:00000000 REG FILE:00000000 REG FILE:00000000

at 6 us: Note: 10xDBC910x60x60x7100x200000x005F0x00160x00010x005FR(6) <= R(6) + 1 (/cpu\_da

at 6300 ns(1): Note: REG FILE:00000000 REG FILE:00000000 REG FILE:00000000 REG FILE:00000000

at 6400 ns: Note: 10xFFD800x70x70x7100x600000x005F0x00160x00150x005FSET ALU NOP, DA=R(

at 6700 ns(1): Note: REG FILE:00000000 REG FILE:00000000 REG FILE:00000000 REG FILE:00000000

at 7100 ns(1): Note: REG FILE:00000000 REG FILE:00000000 REG FILE:00000000 REG FILE:00000000

at 7500 ns(1): Note: REG FILE:00000000 REG FILE:00000000 REG FILE:00000000 REG FILE:00000000

at 7900 ns(1): Note: REG FILE:00000000 REG FILE:00000000 REG FILE:00000000 REG FILE:00000000

at 8300 ns(1): Note: REG FILE:00000000 REG FILE:00000000 REG FILE:00000000 REG FILE:00000000

at 8700 ns(1): Note: REG FILE:00000000 REG FILE:00000000 REG FILE:00000000 REG FILE:00000000

at 9100 ns(1): Note: REG FILE:00000000 REG FILE:00000000 REG FILE:00000000 REG FILE:00000000

at 9500 ns(1): Note: REG FILE:00000000 REG FILE:00000000 REG FILE:00000000 REG FILE:00000000

at 9900 ns(1): Note: REG FILE:00000000 REG FILE:00000000 REG FILE:00000000 REG FILE:00000000

rence is considered.

the differences between the Lite and the Full version.

\_outData\_outComment (/cpu\_datapath\_tb/).

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)/UUT/REG\_FILE1/).

```
22220011 (/cpu_datapath_tb/UUT/REG_FILE1/).
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22220011REG FILE:2203322220011 (/cpu_datapath_tb/UUT/REG_FILE1/).
```

```
2220011REG FILE:2203322220011REG FILE:2203322220011 (/cpu_datapath_tb/UUT/REG_FILE1/).
```

22220011REG FILE:2203322220011REG FILE:2203322220011REG FILE:2103322220011 (/cpu\_datap

22220011REG FILE:220332220011REG FILE:220332220011REG FILE:210332220011REG FILE:2

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datapath\_tb/UUT/REG\_FILE1/).

113322220011 (/cpu\_datapath\_tb/UUT/REG\_FILE1/).

113322220011 REG FILE:2113322220011 (/cpu\_datapath\_tb/UUT/REG\_FILE1/).

113322220011 REG FILE:2113322220011 REG FILE:2113322220011 (/cpu\_datapath\_tb/UUT/REG\_FIL

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E1/).

datapath\_tb/UUT/REG\_FILE1/).

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ILE:2113322220011 (/cpu_datapath_tb/UUT/REG_FILE1/).
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```
ILE:2113322220011 REG FILE:2113322220011 (/cpu_datapath_tb/UUT/REG_FILE1/).
```

```
ILE:2113322220011REG FILE:2113322220011REG FILE:2113322220011 (/cpu_datapath_tb/UUT/REG
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ILE:2113322220011REG FILE:2113322220011REG FILE:2113322220011REG FILE:2113322220011 (/)

ILE:2113322220011REG FILE:2113322220011REG FILE:2113322220011REG FILE:2113322220011RE

ILE:2113322220011REG FILE:2113322220011REG FILE:2113322220011REG FILE:2113322220011REG





















i\_FILE1/).

cpu\_datapath\_tb/UUT/REG\_FILE1/).

≡G FILE:2113322220011 (/cpu\_datapath\_tb/UUT/REG\_FILE1/).

≡G FILE:2113322220011 REG FILE:2113322220011 (/cpu\_datapath\_tb/UUT/REG\_FILE1/).















































































