

ERROR:HDLParasers:1418 - "CPU\_BRANCH\_CTRL/64200100/branch\_ctrl.vhd" Line 81. Formal generi  
ERROR:HDLParasers:3264 - Can't read file "CPU\_BRANCH\_CTRL/64200238/./branch\_ctrl.vhd": No su  
ERROR:HDLParasers:851 - "CPU\_BRANCH\_CTRL/64210113/branch\_ctrl.vhd" Line 71. Formal x of cou  
ERROR:HDLParasers:3010 - "CPU\_BRANCH\_CTRL/64210455/branch\_ctrl.vhd" Line 1. Entity branch\_c  
ERROR:HDLParasers:3312 - "CPU\_BRANCH\_CTRL/64210455/branch\_ctrl.vhd" Line 2. Undefined sym  
ERROR:HDLParasers:1209 - "CPU\_BRANCH\_CTRL/64210455/branch\_ctrl.vhd" Line 2. mux\_vector\_ar  
ERROR:HDLParasers:842 - "CPU\_BRANCH\_CTRL/64210455/branch\_ctrl.vhd" Line 2. The type of the €  
ERROR:HDLParasers:3312 - "CPU\_BRANCH\_CTRL/64210455/branch\_ctrl.vhd" Line 3. Undefined sym  
ERROR:HDLParasers:1209 - "CPU\_BRANCH\_CTRL/64210455/branch\_ctrl.vhd" Line 3. muxnto1\_bus\_l  
ERROR:HDLParasers:3312 - "CPU\_BRANCH\_CTRL/64210455/branch\_ctrl.vhd" Line 3. Undefined sym  
ERROR:HDLParasers:1209 - "CPU\_BRANCH\_CTRL/64210455/branch\_ctrl.vhd" Line 3. ctr\_width: Unde  
ERROR:HDLParasers:842 - "CPU\_BRANCH\_CTRL/64210455/branch\_ctrl.vhd" Line 3. The type of the €  
ERROR:HDLParasers:3312 - "CPU\_BRANCH\_CTRL/64210455/branch\_ctrl.vhd" Line 4. Undefined sym  
ERROR:HDLParasers:1209 - "CPU\_BRANCH\_CTRL/64210455/branch\_ctrl.vhd" Line 4. std\_logic\_vectc  
ERROR:HDLParasers:3312 - "CPU\_BRANCH\_CTRL/64210455/branch\_ctrl.vhd" Line 6. Undefined sym  
ERROR:HDLParasers:1209 - "CPU\_BRANCH\_CTRL/64210455/branch\_ctrl.vhd" Line 6. std\_logic: Unde  
ERROR:HDLParasers:3312 - "CPU\_BRANCH\_CTRL/64210455/branch\_ctrl.vhd" Line 11. Undefined syr  
ERROR:HDLParasers:3312 - "CPU\_BRANCH\_CTRL/64210455/branch\_ctrl.vhd" Line 13. Undefined syr  
ERROR:HDLParasers:1209 - "CPU\_BRANCH\_CTRL/64210455/branch\_ctrl.vhd" Line 13. branch\_mux\_  
ERROR:HDLParasers:3312 - "CPU\_BRANCH\_CTRL/64210455/branch\_ctrl.vhd" Line 13. Undefined syr  
ERROR:HDLParasers:1209 - "CPU\_BRANCH\_CTRL/64210455/branch\_ctrl.vhd" Line 13. branch\_mux\_  
ERROR:HDLParasers:3312 - "CPU\_BRANCH\_CTRL/64210455/branch\_ctrl.vhd" Line 14. Undefined syr  
ERROR:HDLParasers:1209 - "CPU\_BRANCH\_CTRL/64210455/branch\_ctrl.vhd" Line 14. PC\_load\_addi  
ERROR:HDLParasers:3312 - "CPU\_BRANCH\_CTRL/64210455/branch\_ctrl.vhd" Line 17. Undefined syr  
ERROR:HDLParasers:3312 - "CPU\_BRANCH\_CTRL/64210455/branch\_ctrl.vhd" Line 17. Undefined syr  
ERROR:HDLParasers:808 - "CPU\_BRANCH\_CTRL/64210455/branch\_ctrl.vhd" Line 17. not can not hav  
ERROR:HDLParasers:3312 - "CPU\_BRANCH\_CTRL/64210455/branch\_ctrl.vhd" Line 18. Undefined syr  
ERROR:HDLParasers:1209 - "CPU\_BRANCH\_CTRL/64210455/branch\_ctrl.vhd" Line 18. nBRANCH: U  
ERROR:HDLParasers:3312 - "CPU\_BRANCH\_CTRL/64210455/branch\_ctrl.vhd" Line 22. Undefined syr  
ERROR:HDLParasers:3312 - "CPU\_BRANCH\_CTRL/64210455/branch\_ctrl.vhd" Line 23. Undefined syr  
ERROR:HDLParasers:1209 - "CPU\_BRANCH\_CTRL/64210455/branch\_ctrl.vhd" Line 23. clk: Undefinec  
ERROR:HDLParasers:3312 - "CPU\_BRANCH\_CTRL/64210455/branch\_ctrl.vhd" Line 23. Undefined syr  
ERROR:HDLParasers:1209 - "CPU\_BRANCH\_CTRL/64210455/branch\_ctrl.vhd" Line 23. nRST: Undefi  
ERROR:HDLParasers:1209 - "CPU\_BRANCH\_CTRL/64210455/branch\_ctrl.vhd" Line 23. CE: Undefinec  
ERROR:HDLParasers:3312 - "CPU\_BRANCH\_CTRL/64210455/branch\_ctrl.vhd" Line 23. Undefined syr  
ERROR:HDLParasers:1209 - "CPU\_BRANCH\_CTRL/64210455/branch\_ctrl.vhd" Line 23. PC\_sig: Unde  
ERROR:HDLParasers:3312 - "CPU\_BRANCH\_CTRL/64210455/branch\_ctrl.vhd" Line 27. Undefined syr  
ERROR:HDLParasers:3312 - "CPU\_BRANCH\_CTRL/64210455/branch\_ctrl.vhd" Line 28. Undefined syr  
ERROR:HDLParasers:1209 - "CPU\_BRANCH\_CTRL/64210455/branch\_ctrl.vhd" Line 28. JB\_address: l  
ERROR:HDLParasers:3312 - "CPU\_BRANCH\_CTRL/64210455/branch\_ctrl.vhd" Line 28. Undefined syr  
ERROR:HDLParasers:1209 - "CPU\_BRANCH\_CTRL/64210455/branch\_ctrl.vhd" Line 28. Adder\_result:  
ERROR:HDLParasers:3312 - "CPU\_BRANCH\_CTRL/64210455/branch\_ctrl.vhd" Line 31. Undefined syr  
ERROR:HDLParasers:1209 - "CPU\_BRANCH\_CTRL/64210455/branch\_ctrl.vhd" Line 31. branch\_mux\_  
ERROR:HDLParasers:3312 - "CPU\_BRANCH\_CTRL/64210455/branch\_ctrl.vhd" Line 33. Undefined syr  
ERROR:HDLParasers:1209 - "CPU\_BRANCH\_CTRL/64210455/branch\_ctrl.vhd" Line 33. JB: Undefined  
ERROR:HDLParasers:3312 - "CPU\_BRANCH\_CTRL/64210455/branch\_ctrl.vhd" Line 35. Undefined syr

c busS does not exist in muxnto1\_bus.  
 ch file or directory  
 inter with no default value must be associated with an actual value.  
 :trl does not exist.  
 bol 'mux\_vector\_array\_type'.  
 ray\_type: Undefined symbol (last report in this block)  
 element in aggregate does not correspond to any array type.  
 bol 'muxnto1\_bus\_type'.  
 type: Undefined symbol (last report in this block)  
 bol 'ctr\_width'.  
 defined symbol (last report in this block)  
 element in aggregate does not correspond to any array type.  
 bol 'std\_logic\_vector'.  
 r: Undefined symbol (last report in this block)  
 bol 'std\_logic'.  
 defined symbol (last report in this block)  
 nbol 'muxnto1\_bus'.  
 nbol 'branch\_mux\_vector'.  
 vector: Undefined symbol (last report in this block)  
 nbol 'branch\_mux\_2d\_bit\_array'.  
 2d\_bit\_array: Undefined symbol (last report in this block)  
 nbol 'PC\_load\_addr'.  
 r: Undefined symbol (last report in this block)  
 nbol 'nBRANCH'.  
 nbol 'N'.  
 e such operands in this context.  
 nbol 'CE'.  
 ndefined symbol (last report in this block)  
 nbol 'counter'.  
 nbol 'clk'.  
 f symbol (last report in this block)  
 nbol 'nRST'.  
 ned symbol (last report in this block)  
 d symbol (last report in this block)  
 nbol 'PC\_sig'.  
 fined symbol (last report in this block)  
 nbol 'cla\_add\_n\_bit'.  
 nbol 'JB\_address'.  
 Jndefined symbol (last report in this block)  
 nbol 'Adder\_result'.  
 Undefined symbol (last report in this block)  
 nbol 'branch\_mux\_vector\_array'.  
 vector\_array: Undefined symbol (last report in this block)  
 nbol 'JB'.  
 l symbol (last report in this block)  
 nbol 'PC'.

>xst -ifn branch_ctrl.xst	>xst -ifn branch_ctrl.xst
Release 14.7 - xst P.20131013 (n64)	Release 14.7 - xst P.20131013 (n64)
Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.	Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.
--> Parameter TMPDIR set to ./xst/projnav.tmp	--> Parameter TMPDIR set to ./xst/projnav.tmp
Total REAL time to Xst completion: 0.00 secs	Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.25 secs	Total CPU time to Xst completion: 0.24 secs
--> WARNING:Xst3164 - Option "-debug" found multiple times in the command line. Only the first occurrence is considered.	--> WARNING:Xst3164 - Option "-debug" found multiple times in the command line. Only the first occurrence is considered.
* HDL Compilation *	* HDL Compilation *
Compiling vhdl file "CPU_BRANCH_CTRL/muxnto1.vhd" in Library work.	Compiling vhdl file "CPU_BRANCH_CTRL/muxnto1.vhd" in Library work.
Entity <muxnto1> compiled.	Entity <muxnto1> compiled.
Entity <muxnto1> (Architecture <ideal>) compiled.	Entity <muxnto1> (Architecture <=>) compiled.
Compiling vhdl file "CPU_BRANCH_CTRL/dff.vhd" in Library work.	Compiling vhdl file "CPU_BRANCH_CTRL/dff.vhd" in Library work.
Entity <dff> compiled.	Entity <dff> compiled.
Entity <dff> (Architecture <ideal>) compiled.	Entity <dff> (Architecture <=>) compiled.
Compiling vhdl file "CPU_BRANCH_CTRL/reg_file_functions.vhd" in Library work.	Compiling vhdl file "CPU_BRANCH_CTRL/cia_qp.vhd" in Library work.
Package <reg_file_functions> compiled.	Entity <cia_qp> compiled.
Package body <reg_file_functions> compiled.	Entity <cia_qp> (Architecture <=>) compiled.
Compiling vhdl file "CPU_BRANCH_CTRL/cia_qp.vhd" in Library work.	Compiling vhdl file "CPU_BRANCH_CTRL/reg_file_functions.vhd" in Library work.
Entity <cia_qp> compiled.	Package <reg_file_functions> compiled.
Entity <cia_qp> (Architecture <ideal>) compiled.	Package body <reg_file_functions> compiled.
Compiling vhdl file "CPU_BRANCH_CTRL/muxdff.vhd" in Library work.	Compiling vhdl file "CPU_BRANCH_CTRL/muxdff.vhd" in Library work.
Entity <muxdff> compiled.	Entity <muxdff> compiled.
Entity <muxdff> (Architecture <ideal>) compiled.	Entity <muxdff> (Architecture <=>) compiled.
Compiling vhdl file "CPU_BRANCH_CTRL/branch_ctrl_functions.vhd" in Library work.	Compiling vhdl file "CPU_BRANCH_CTRL/branch_ctrl_functions.vhd" in Library work.
Package <branch_ctrl_functions> compiled.	Package <branch_ctrl_functions> compiled.
Package body <branch_ctrl_functions> compiled.	Package body <branch_ctrl_functions> compiled.
Compiling vhdl file "CPU_BRANCH_CTRL/counter.vhd" in Library work.	Compiling vhdl file "CPU_BRANCH_CTRL/counter.vhd" in Library work.
Entity <counter> compiled.	Entity <counter> compiled.
Entity <counter> (Architecture <ideal>) compiled.	Entity <counter> (Architecture <=>) compiled.
Compiling vhdl file "CPU_BRANCH_CTRL/cia_add_n_bit.vhd" in Library work.	Compiling vhdl file "CPU_BRANCH_CTRL/muxnto1_bus.vhd" in Library work.
Entity <cia_add_n_bit> compiled.	Entity <muxnto1_bus> compiled.
Entity <cia_add_n_bit> (Architecture <ideal>) compiled.	Entity <muxnto1_bus> (Architecture <=>) compiled.
Compiling vhdl file "CPU_BRANCH_CTRL/muxnto1_bus.vhd" in Library work.	Compiling vhdl file "CPU_BRANCH_CTRL/cia_add_n_bit.vhd" in Library work.
Entity <muxnto1_bus> compiled.	Entity <cia_add_n_bit> compiled.
Entity <muxnto1_bus> (Architecture <ideal>) compiled.	Entity <cia_add_n_bit> (Architecture <=>) compiled.
Compiling vhdl file "CPU_BRANCH_CTRL/branch_ctrl.vhd" in Library work.	Compiling vhdl file "CPU_BRANCH_CTRL/branch_ctrl.vhd" in Library work.
Entity <branch_ctrl> compiled.	Entity <branch_ctrl> compiled.
Entity <branch_ctrl> (Architecture <ideal>) compiled.	Entity <branch_ctrl> (Architecture <=>) compiled.
Total REAL time to Xst completion: 0.00 secs	Total REAL time to Xst completion: 4.00 secs
Total CPU time to Xst completion: 0.56 secs	Total CPU time to Xst completion: 3.27 secs
-->	-->
Total memory usage is 4477332 kilobytes	Total memory usage is 4477120 kilobytes
Number of errors : 0 ( 0 filtered)	Number of errors : 0 ( 0 filtered)
Number of warnings : 1 ( 0 filtered)	Number of warnings : 1 ( 0 filtered)
Number of infos : 0 ( 0 filtered)	Number of infos : 0 ( 0 filtered)
>fuse -incremental -o branch_ctrl_tb.isim beh.exe -prj branch_ctrl_tb.prj -top branch_ctrl_tb	>fuse -incremental -o branch_ctrl_tb.isim beh.exe -prj branch_ctrl_tb.prj -top branch_ctrl_tb
ISim P.20131013 (signature 0x7708f090)	ISim P.20131013 (signature 0x7708f090)
Number of CPUs detected in this system: 8	Number of CPUs detected in this system: 8
Turning on multi-threading, number of parallel sub-compilation jobs: 16	Turning on multi-threading, number of parallel sub-compilation jobs: 16
Determining compilation order of HDL files	Determining compilation order of HDL files
Parsing VHDL file "muxnto1.vhd" into library work	Parsing VHDL file "muxnto1.vhd" into library work
Parsing VHDL file "dff.vhd" into library work	Parsing VHDL file "dff.vhd" into library work
Parsing VHDL file "reg_file_functions.vhd" into library work	Parsing VHDL file "reg_file_functions.vhd" into library work
Parsing VHDL file "muxdff.vhd" into library work	Parsing VHDL file "muxdff.vhd" into library work
Parsing VHDL file "cia_qp.vhd" into library work	Parsing VHDL file "cia_qp.vhd" into library work
Parsing VHDL file "muxnto1_bus.vhd" into library work	Parsing VHDL file "muxnto1_bus.vhd" into library work
Parsing VHDL file "counter.vhd" into library work	Parsing VHDL file "counter.vhd" into library work
Parsing VHDL file "cia_add_n_bit.vhd" into library work	Parsing VHDL file "cia_add_n_bit.vhd" into library work
Parsing VHDL file "branch_ctrl_functions.vhd" into library work	Parsing VHDL file "branch_ctrl_functions.vhd" into library work
Parsing VHDL file "branch_ctrl.vhd" into library work	Parsing VHDL file "branch_ctrl.vhd" into library work
Parsing VHDL file "branch_ctrl_tb.vhd" into library work	Parsing VHDL file "branch_ctrl_tb.vhd" into library work
Starting static elaboration	Starting static elaboration
Completed static elaboration	Completed static elaboration
Compiling package standard	Compiling package standard

<pre> &gt;xst -fin branch_ctrl.xst Release 14.7 - xst P.20131013 (nt64) Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved. --&gt; Parameter TMPDIR set to /xst/projnav.tmp <b>Total REAL time to Xst completion: 1.00 secs</b> <b>Total CPU time to Xst completion: 0.23 secs</b>  --&gt; WARNING:Xst:3164 - Option "-debug" found multiple times in the command line. Only the first occurrence is considered. *          HDL Compilation          * Compiling vhdl file "CPU_BRANCH_CTRL/muxnto1.vhd" in Library work. Entity &lt;muxnto1&gt; compiled. <b>Entity &lt;muxnto1&gt; (Architecture &lt;ideal&gt;) compiled.</b> Compiling vhdl file "CPU_BRANCH_CTRL/dff.vhd" in Library work. Entity &lt;dff&gt; compiled. <b>Entity &lt;dff&gt; (Architecture &lt;ideal&gt;) compiled.</b> Compiling vhdl file "CPU_BRANCH_CTRL/req_file_functions.vhd" in Library work. Package &lt;req_file_functions&gt; compiled. <b>Package body &lt;req_file_functions&gt; compiled.</b> Compiling vhdl file "CPU_BRANCH_CTRL/cia_gp.vhd" in Library work. Entity &lt;cia_gp&gt; compiled. <b>Entity &lt;cia_gp&gt; (Architecture &lt;ideal&gt;) compiled.</b> Compiling vhdl file "CPU_BRANCH_CTRL/muxdff.vhd" in Library work. Entity &lt;muxdff&gt; compiled. <b>Entity &lt;muxdff&gt; (Architecture &lt;ideal&gt;) compiled.</b> Compiling vhdl file "CPU_BRANCH_CTRL/branch_ctrl_functions.vhd" in Library work. Package &lt;branch_ctrl_functions&gt; compiled. Package body &lt;branch_ctrl_functions&gt; compiled. Compiling vhdl file "CPU_BRANCH_CTRL/counter.vhd" in Library work. Entity &lt;counter&gt; compiled. <b>Entity &lt;counter&gt; (Architecture &lt;ideal&gt;) compiled.</b> Compiling vhdl file "CPU_BRANCH_CTRL/cia_add_n_bit.vhd" in Library work. Entity &lt;cia_add_n_bit&gt; compiled. <b>Entity &lt;cia_add_n_bit&gt; (Architecture &lt;ideal&gt;) compiled.</b> Compiling vhdl file "CPU_BRANCH_CTRL/muxnto1_bus.vhd" in Library work. Entity &lt;muxnto1_bus&gt; compiled. <b>Entity &lt;muxnto1_bus&gt; (Architecture &lt;ideal&gt;) compiled.</b> Compiling vhdl file "CPU_BRANCH_CTRL/branch_ctrl.vhd" in Library work. Entity &lt;branch_ctrl&gt; compiled. <b>ERROR:HDLParasys:1418 - "CPU_BRANCH_CTRL/branch_ctrl.vhd" Line 81. Formal generic busS does not exist in muxnto1_bus.</b> <b>Total REAL time to Xst completion: 1.00 secs</b> <b>Total CPU time to Xst completion: 0.70 secs</b>  --&gt; <b>Total memory usage is 4477140 kilobytes</b> Number of errors : 1 ( 0 filtered) Number of warnings : 1 ( 0 filtered) Number of infos : 0 ( 0 filtered) *Use incremental -o branch_ctrl.tb isim_beh.exe -prj branch_ctrl.tb.prj -top branch_ctrl.tb (ISim P.20131013 (signature 0x7708090)) Number of CPUs detected in this system: 8 Turning on multi-threading, number of parallel sub-compilation jobs: 16 Determining compilation order of HDL files Parsing VHDL file "muxnto1.vhd" into library work Parsing VHDL file "dff.vhd" into library work Parsing VHDL file "req_file_functions.vhd" into library work Parsing VHDL file "muxdff.vhd" into library work Parsing VHDL file "cia_gp.vhd" into library work Parsing VHDL file "muxnto1_bus.vhd" into library work Parsing VHDL file "counter.vhd" into library work Parsing VHDL file "cia_add_n_bit.vhd" into library work Parsing VHDL file "branch_ctrl_functions.vhd" into library work Parsing VHDL file "branch_ctrl.vhd" into library work <b>VHDL file branch_ctrl.vhd ignored due to errors</b> -&gt;branch_ctrl.tb isim_beh.exe -sbatch isim.tcl -wdb branch_ctrl.tb isim_beh.wdb  </pre>	<pre> &gt;xst -fin branch_ctrl.xst Release 14.7 - xst P.20131013 (nt64) Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved. --&gt; Parameter TMPDIR set to /xst/projnav.tmp <b>Total REAL time to Xst completion: 0.00 secs</b> <b>Total CPU time to Xst completion: 0.24 secs</b>  --&gt; WARNING:Xst:3164 - Option "-debug" found multiple times in the command line. Only the first occurrence is considered. *          HDL Compilation          * Compiling vhdl file "CPU_BRANCH_CTRL/muxnto1.vhd" in Library work. Entity &lt;muxnto1&gt; compiled. Entity &lt;muxnto1&gt; (Architecture &lt;=&gt;) compiled. Compiling vhdl file "CPU_BRANCH_CTRL/dff.vhd" in Library work. Entity &lt;dff&gt; compiled. Entity &lt;dff&gt; (Architecture &lt;=&gt;) compiled. Compiling vhdl file "CPU_BRANCH_CTRL/cia_gp.vhd" in Library work. Entity &lt;cia_gp&gt; compiled. Entity &lt;cia_gp&gt; (Architecture &lt;=&gt;) compiled. Compiling vhdl file "CPU_BRANCH_CTRL/req_file_functions.vhd" in Library work. Package &lt;req_file_functions&gt; compiled. Package body &lt;req_file_functions&gt; compiled. Compiling vhdl file "CPU_BRANCH_CTRL/muxdff.vhd" in Library work. Entity &lt;muxdff&gt; compiled. Entity &lt;muxdff&gt; (Architecture &lt;=&gt;) compiled. Compiling vhdl file "CPU_BRANCH_CTRL/branch_ctrl_functions.vhd" in Library work. Package &lt;branch_ctrl_functions&gt; compiled. Package body &lt;branch_ctrl_functions&gt; compiled. Compiling vhdl file "CPU_BRANCH_CTRL/counter.vhd" in Library work. Entity &lt;counter&gt; compiled. Entity &lt;counter&gt; (Architecture &lt;=&gt;) compiled. Compiling vhdl file "CPU_BRANCH_CTRL/muxnto1_bus.vhd" in Library work. Entity &lt;muxnto1_bus&gt; compiled. Entity &lt;muxnto1_bus&gt; (Architecture &lt;=&gt;) compiled. Compiling vhdl file "CPU_BRANCH_CTRL/cia_add_n_bit.vhd" in Library work. Entity &lt;cia_add_n_bit&gt; compiled. Entity &lt;cia_add_n_bit&gt; (Architecture &lt;=&gt;) compiled. Compiling vhdl file "CPU_BRANCH_CTRL/branch_ctrl.vhd" in Library work. Entity &lt;branch_ctrl&gt; compiled. Entity &lt;branch_ctrl&gt; (Architecture &lt;=&gt;) compiled. <b>Total REAL time to Xst completion: 4.00 secs</b> <b>Total CPU time to Xst completion: 3.27 secs</b>  --&gt; <b>Total memory usage is 4477120 kilobytes</b> Number of errors : 0 ( 0 filtered) Number of warnings : 1 ( 0 filtered) Number of infos : 0 ( 0 filtered) *Use incremental -o branch_ctrl.tb isim_beh.exe -prj branch_ctrl.tb.prj -top branch_ctrl.tb (ISim P.20131013 (signature 0x7708090)) Number of CPUs detected in this system: 8 Turning on multi-threading, number of parallel sub-compilation jobs: 16 Determining compilation order of HDL files Parsing VHDL file "muxnto1.vhd" into library work Parsing VHDL file "dff.vhd" into library work Parsing VHDL file "req_file_functions.vhd" into library work Parsing VHDL file "muxdff.vhd" into library work Parsing VHDL file "cia_gp.vhd" into library work Parsing VHDL file "muxnto1_bus.vhd" into library work Parsing VHDL file "counter.vhd" into library work Parsing VHDL file "cia_add_n_bit.vhd" into library work Parsing VHDL file "branch_ctrl_functions.vhd" into library work Parsing VHDL file "branch_ctrl.vhd" into library work Parsing VHDL file "branch_ctrl.tb.vhd" into library work Starting static elaboration Completed static elaboration Compiling package standard  </pre>
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>xst -fHn branch_ctrl.xst	>xst -fHn branch_ctrl.xst
Release 14.7 - xst P.20131013 (n64)	Release 14.7 - xst P.20131013 (n64)
Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.	Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.
-> Parameter TMPDIR set to /xstprojdir/tmp	-> Parameter TMPDIR set to /xstprojdir/tmp
Total REAL time to Xst completion: 0.00 secs	Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.23 secs	Total CPU time to Xst completion: 0.24 secs
-> WARNING:Xst:3164 - Option "-debug" found multiple times in the command line. Only the first occurrence is considered.	-> WARNING:Xst:3164 - Option "-debug" found multiple times in the command line. Only the first occurrence is considered.
HDL Compiler	HDL Compiler
Compiling vhdl file "CPU_BRANCH_CTRL/muxento1.vhd" in Library work.	Compiling vhdl file "CPU_BRANCH_CTRL/muxento1.vhd" in Library work.
Entity <muxento1> compiled.	Entity <muxento1> compiled.
Entity <muxento1> (Architecture <ideal>) compiled.	Entity <muxento1> (Architecture <=>) compiled.
Compiling vhdl file "CPU_BRANCH_CTRL/dff.vhd" in Library work.	Compiling vhdl file "CPU_BRANCH_CTRL/dff.vhd" in Library work.
Entity <dff> compiled.	Entity <dff> compiled.
Entity <dff> (Architecture <ideal>) compiled.	Entity <dff> (Architecture <=>) compiled.
Compiling vhdl file "CPU_BRANCH_CTRL/req_file_functions.vhd" in Library work.	Compiling vhdl file "CPU_BRANCH_CTRL/cia_gp.vhd" in Library work.
Package <req_file_functions> compiled.	Entity <cia_gp> compiled.
Package body <req_file_functions> compiled.	Entity <cia_gp> (Architecture <=>) compiled.
Compiling vhdl file "CPU_BRANCH_CTRL/cia_gp.vhd" in Library work.	Compiling vhdl file "CPU_BRANCH_CTRL/req_file_functions.vhd" in Library work.
Entity <cia_gp> compiled.	Package <req_file_functions> compiled.
Entity <cia_gp> (Architecture <ideal>) compiled.	Package body <req_file_functions> compiled.
Compiling vhdl file "CPU_BRANCH_CTRL/muxdff.vhd" in Library work.	Compiling vhdl file "CPU_BRANCH_CTRL/muxdff.vhd" in Library work.
Entity <muxdff> compiled.	Entity <muxdff> compiled.
Entity <muxdff> (Architecture <ideal>) compiled.	Entity <muxdff> (Architecture <=>) compiled.
Compiling vhdl file "CPU_BRANCH_CTRL/branch_ctrl_functions.vhd" in Library work.	Compiling vhdl file "CPU_BRANCH_CTRL/branch_ctrl_functions.vhd" in Library work.
Package <branch_ctrl_functions> compiled.	Package <branch_ctrl_functions> compiled.
Package body <branch_ctrl_functions> compiled.	Package body <branch_ctrl_functions> compiled.
Compiling vhdl file "CPU_BRANCH_CTRL/counter.vhd" in Library work.	Compiling vhdl file "CPU_BRANCH_CTRL/counter.vhd" in Library work.
Entity <counter> compiled.	Entity <counter> compiled.
Entity <counter> (Architecture <ideal>) compiled.	Entity <counter> (Architecture <=>) compiled.
Compiling vhdl file "CPU_BRANCH_CTRL/cia_add_n_bit.vhd" in Library work.	Compiling vhdl file "CPU_BRANCH_CTRL/muxento1_bus.vhd" in Library work.
Entity <cia_add_n_bit> compiled.	Entity <muxento1_bus> compiled.
Entity <cia_add_n_bit> (Architecture <ideal>) compiled.	Entity <muxento1_bus> (Architecture <=>) compiled.
Compiling vhdl file "CPU_BRANCH_CTRL/muxento1_bus.vhd" in Library work.	Compiling vhdl file "CPU_BRANCH_CTRL/cia_add_n_bit.vhd" in Library work.
Entity <muxento1_bus> compiled.	Entity <cia_add_n_bit> compiled.
Entity <muxento1_bus> (Architecture <ideal>) compiled.	Entity <cia_add_n_bit> (Architecture <=>) compiled.
Compiling vhdl file "CPU_BRANCH_CTRL/branch_ctrl.vhd" in Library work.	Compiling vhdl file "CPU_BRANCH_CTRL/branch_ctrl.vhd" in Library work.
Entity <branch_ctrl> compiled.	Entity <branch_ctrl> compiled.
Entity <branch_ctrl> (Architecture <ideal>) compiled.	Entity <branch_ctrl> (Architecture <=>) compiled.
Total REAL time to Xst completion: 0.00 secs	Total REAL time to Xst completion: 4.00 secs
Total CPU time to Xst completion: 0.38 secs	Total CPU time to Xst completion: 3.27 secs
->	->
Total memory usage is 4477132 kilobytes	Total memory usage is 4477120 kilobytes
Number of errors : 0 ( 0 filtered)	Number of errors : 0 ( 0 filtered)
Number of warnings : 1 ( 0 filtered)	Number of warnings : 1 ( 0 filtered)
Number of infos : 0 ( 0 filtered)	Number of infos : 0 ( 0 filtered)
*Use incremental -o branch_ctrl tb isim beh.exe -pri branch_ctrl tb.pri -top branch_ctrl tb	*Use incremental -o branch_ctrl tb isim beh.exe -pri branch_ctrl tb.pri -top branch_ctrl tb
(Sim P.20131013 (signature 0x7708090))	(Sim P.20131013 (signature 0x7708090))
Number of CPUs detected in this system: 8	Number of CPUs detected in this system: 8
Turning on multi-threading, number of parallel sub-compilation jobs: 16	Turning on multi-threading, number of parallel sub-compilation jobs: 16
Determining compilation order of HDL files	Determining compilation order of HDL files
Parsing VHDL file "muxento1.vhd" into library work	Parsing VHDL file "muxento1.vhd" into library work
Parsing VHDL file "dff.vhd" into library work	Parsing VHDL file "dff.vhd" into library work
Parsing VHDL file "req_file_functions.vhd" into library work	Parsing VHDL file "req_file_functions.vhd" into library work
Parsing VHDL file "muxdff.vhd" into library work	Parsing VHDL file "muxdff.vhd" into library work
Parsing VHDL file "cia_gp.vhd" into library work	Parsing VHDL file "cia_gp.vhd" into library work
Parsing VHDL file "muxento1_bus.vhd" into library work	Parsing VHDL file "muxento1_bus.vhd" into library work
Parsing VHDL file "counter.vhd" into library work	Parsing VHDL file "counter.vhd" into library work
Parsing VHDL file "cia_add_n_bit.vhd" into library work	Parsing VHDL file "cia_add_n_bit.vhd" into library work
Parsing VHDL file "branch_ctrl_functions.vhd" into library work	Parsing VHDL file "branch_ctrl_functions.vhd" into library work
Parsing VHDL file "branch_ctrl.vhd" into library work	Parsing VHDL file "branch_ctrl.vhd" into library work
Parsing VHDL file "branch_ctrl_tb.vhd" into library work	Parsing VHDL file "branch_ctrl_tb.vhd" into library work
Starting static elaboration	Starting static elaboration
Completed static elaboration	Completed static elaboration
Compiling package standard	Compiling package standard

>xst -ifn branch_ctrl.xst	>xst -ifn branch_ctrl.xst
Release 14.7 - xst P.20131013 (n64)	Release 14.7 - xst P.20131013 (n64)
Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.	Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.
--> Parameter TMPDIR set to ./xst/projnav.tmp	--> Parameter TMPDIR set to ./xst/projnav.tmp
Total REAL time to Xst completion: 1.00 secs	Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.27 secs	Total CPU time to Xst completion: 0.24 secs
--> WARNING:Xst3164 - Option "-debug" found multiple times in the command line. Only the first occurrence is considered.	--> WARNING:Xst3164 - Option "-debug" found multiple times in the command line. Only the first occurrence is considered.
* HDL Compilation	* HDL Compilation
Compiling vhdl file "CPU_BRANCH_CTRL/muxnto1.vhd" in Library work.	Compiling vhdl file "CPU_BRANCH_CTRL/muxnto1.vhd" in Library work.
Entity <muxnto1> compiled.	Entity <muxnto1> compiled.
Entity <muxnto1> (Architecture <ideal>) compiled.	Entity <muxnto1> (Architecture <>) compiled.
Compiling vhdl file "CPU_BRANCH_CTRL/dff.vhd" in Library work.	Compiling vhdl file "CPU_BRANCH_CTRL/dff.vhd" in Library work.
Entity <dff> compiled.	Entity <dff> compiled.
Entity <dff> (Architecture <ideal>) compiled.	Entity <dff> (Architecture <>) compiled.
Compiling vhdl file "CPU_BRANCH_CTRL/reg_file_functions.vhd" in Library work.	Compiling vhdl file "CPU_BRANCH_CTRL/cia_gp.vhd" in Library work.
Package <reg_file_functions> compiled.	Entity <cia_gp> compiled.
Package body <reg_file_functions> compiled.	Entity <cia_gp> (Architecture <>) compiled.
Compiling vhdl file "CPU_BRANCH_CTRL/muxdff.vhd" in Library work.	Compiling vhdl file "CPU_BRANCH_CTRL/reg_file_functions.vhd" in Library work.
Entity <muxdff> compiled.	Package <reg_file_functions> compiled.
Entity <muxdff> (Architecture <ideal>) compiled.	Package body <reg_file_functions> compiled.
Compiling vhdl file "CPU_BRANCH_CTRL/cia_gp.vhd" in Library work.	Compiling vhdl file "CPU_BRANCH_CTRL/muxdff.vhd" in Library work.
Entity <cia_gp> compiled.	Entity <muxdff> compiled.
Entity <cia_gp> (Architecture <ideal>) compiled.	Entity <muxdff> (Architecture <>) compiled.
Compiling vhdl file "CPU_BRANCH_CTRL/muxnto1_bus.vhd" in Library work.	Compiling vhdl file "CPU_BRANCH_CTRL/branch_ctrl_functions.vhd" in Library work.
Entity <muxnto1_bus> compiled.	Package <branch_ctrl_functions> compiled.
Entity <muxnto1_bus> (Architecture <ideal>) compiled.	Package body <branch_ctrl_functions> compiled.
Compiling vhdl file "CPU_BRANCH_CTRL/counter.vhd" in Library work.	Compiling vhdl file "CPU_BRANCH_CTRL/counter.vhd" in Library work.
Entity <counter> compiled.	Entity <counter> compiled.
Entity <counter> (Architecture <ideal>) compiled.	Entity <counter> (Architecture <>) compiled.
Compiling vhdl file "CPU_BRANCH_CTRL/cia_add_n_bit.vhd" in Library work.	Compiling vhdl file "CPU_BRANCH_CTRL/muxnto1_bus.vhd" in Library work.
Entity <cia_add_n_bit> compiled.	Entity <muxnto1_bus> compiled.
Entity <cia_add_n_bit> (Architecture <ideal>) compiled.	Entity <muxnto1_bus> (Architecture <>) compiled.
Compiling vhdl file "CPU_BRANCH_CTRL/branch_ctrl_functions.vhd" in Library work.	Compiling vhdl file "CPU_BRANCH_CTRL/cia_add_n_bit.vhd" in Library work.
Package <branch_ctrl_functions> compiled.	Entity <cia_add_n_bit> compiled.
Package body <branch_ctrl_functions> compiled.	Entity <cia_add_n_bit> (Architecture <>) compiled.
Compiling vhdl file "CPU_BRANCH_CTRL/branch_ctrl.vhd" in Library work.	Compiling vhdl file "CPU_BRANCH_CTRL/branch_ctrl.vhd" in Library work.
ERROR:HDLParasers:3264 - Can't read file "CPU_BRANCH_CTRL//branch_ctrl.vhd": No such file or directory	Entity <branch_ctrl> compiled.
Total REAL time to Xst completion: 1.00 secs	Entity <branch_ctrl> (Architecture <>) compiled.
Total CPU time to Xst completion: 0.44 secs	Total REAL time to Xst completion: 4.00 secs
-->	Total CPU time to Xst completion: 3.27 secs
-->	-->
Total memory usage is 4477120 kilobytes	Total memory usage is 4477120 kilobytes
Number of errors : 1 ( 0 filtered)	Number of errors : 0 ( 0 filtered)
Number of warnings : 1 ( 0 filtered)	Number of warnings : 1 ( 0 filtered)
Number of infos : 0 ( 0 filtered)	Number of infos : 0 ( 0 filtered)
-fuse -incremental -o branch_ctrl_tb.isim beh.exe -prj branch_ctrl_tb.prj -top branch_ctrl_tb	-fuse -incremental -o branch_ctrl_tb.isim beh.exe -prj branch_ctrl_tb.prj -top branch_ctrl_tb
(ISim P.20131013 (signature 0x7708f090))	(ISim P.20131013 (signature 0x7708f090))
Number of CPUs detected in this system: 8	Number of CPUs detected in this system: 8
Turning on multi-threading, number of parallel sub-compilation jobs: 16	Turning on multi-threading, number of parallel sub-compilation jobs: 16
Determining compilation order of HDL files	Determining compilation order of HDL files
>branch_ctrl_tb.isim beh.exe -tclbatch isim.tcl -wdb branch_ctrl_tb.isim beh.wdb	Parsing VHDL file "muxnto1.vhd" into library work
	Parsing VHDL file "dff.vhd" into library work
	Parsing VHDL file "reg_file_functions.vhd" into library work
	Parsing VHDL file "muxdff.vhd" into library work
	Parsing VHDL file "cia_gp.vhd" into library work
	Parsing VHDL file "muxnto1_bus.vhd" into library work
	Parsing VHDL file "counter.vhd" into library work
	Parsing VHDL file "cia_add_n_bit.vhd" into library work
	Parsing VHDL file "branch_ctrl_functions.vhd" into library work
	Parsing VHDL file "branch_ctrl.vhd" into library work
	Parsing VHDL file "branch_ctrl_tb.vhd" into library work
	Starting static elaboration
	Completed static elaboration
	Compiling package standard

>xst -fhn branch_ctrl.xst	>xst -fhn branch_ctrl.xst
Release 14.7 - xst P.20131013 (n64)	Release 14.7 - xst P.20131013 (n64)
Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.	Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.
-> Parameter TMPDIR set to /xstprojdir/tmp	-> Parameter TMPDIR set to /xstprojdir/tmp
Total REAL time to Xst completion: 1.68 secs	Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.22 secs	Total CPU time to Xst completion: 0.24 secs
-> WARNING:Xst:3164 - Option "-debug" found multiple times in the command line. Only the first occurrence is considered.	-> WARNING:Xst:3164 - Option "-debug" found multiple times in the command line. Only the first occurrence is considered.
HDL Compiler	HDL Compiler
Compiling vhdl file "CPU_BRANCH_CTRL/muxento1.vhd" in Library work.	Compiling vhdl file "CPU_BRANCH_CTRL/muxento1.vhd" in Library work.
Entity <muxento1> compiled.	Entity <muxento1> compiled.
Entity <muxento1> (Architecture <ideal>) compiled.	Entity <muxento1> (Architecture <=>) compiled.
Compiling vhdl file "CPU_BRANCH_CTRL/gf1.vhd" in Library work.	Compiling vhdl file "CPU_BRANCH_CTRL/gf1.vhd" in Library work.
Entity <gf1> compiled.	Entity <gf1> compiled.
Entity <gf1> (Architecture <ideal>) compiled.	Entity <gf1> (Architecture <=>) compiled.
Compiling vhdl file "CPU_BRANCH_CTRL/req_file_functions.vhd" in Library work.	Compiling vhdl file "CPU_BRANCH_CTRL/req_file_functions.vhd" in Library work.
Package <req_file_functions> compiled.	Package <req_file_functions> compiled.
Package body <req_file_functions> compiled.	Package body <req_file_functions> compiled.
Compiling vhdl file "CPU_BRANCH_CTRL/cia_gp.vhd" in Library work.	Compiling vhdl file "CPU_BRANCH_CTRL/cia_gp.vhd" in Library work.
Entity <cia_gp> compiled.	Entity <cia_gp> compiled.
Entity <cia_gp> (Architecture <ideal>) compiled.	Entity <cia_gp> (Architecture <=>) compiled.
Compiling vhdl file "CPU_BRANCH_CTRL/muxdff.vhd" in Library work.	Compiling vhdl file "CPU_BRANCH_CTRL/muxdff.vhd" in Library work.
Entity <muxdff> compiled.	Entity <muxdff> compiled.
Entity <muxdff> (Architecture <ideal>) compiled.	Entity <muxdff> (Architecture <=>) compiled.
Compiling vhdl file "CPU_BRANCH_CTRL/branch_ctrl_functions.vhd" in Library work.	Compiling vhdl file "CPU_BRANCH_CTRL/branch_ctrl_functions.vhd" in Library work.
Package <branch_ctrl_functions> compiled.	Package <branch_ctrl_functions> compiled.
Package body <branch_ctrl_functions> compiled.	Package body <branch_ctrl_functions> compiled.
Compiling vhdl file "CPU_BRANCH_CTRL/counter.vhd" in Library work.	Compiling vhdl file "CPU_BRANCH_CTRL/counter.vhd" in Library work.
Entity <counter> compiled.	Entity <counter> compiled.
Entity <counter> (Architecture <ideal>) compiled.	Entity <counter> (Architecture <=>) compiled.
Compiling vhdl file "CPU_BRANCH_CTRL/cia_add_n_bit.vhd" in Library work.	Compiling vhdl file "CPU_BRANCH_CTRL/cia_add_n_bit.vhd" in Library work.
Entity <cia_add_n_bit> compiled.	Entity <cia_add_n_bit> compiled.
Entity <cia_add_n_bit> (Architecture <ideal>) compiled.	Entity <cia_add_n_bit> (Architecture <=>) compiled.
Compiling vhdl file "CPU_BRANCH_CTRL/muxento1_bus.vhd" in Library work.	Compiling vhdl file "CPU_BRANCH_CTRL/muxento1_bus.vhd" in Library work.
Entity <muxento1_bus> compiled.	Entity <muxento1_bus> compiled.
Entity <muxento1_bus> (Architecture <ideal>) compiled.	Entity <muxento1_bus> (Architecture <=>) compiled.
Compiling vhdl file "CPU_BRANCH_CTRL/branch_ctrl.vhd" in Library work.	Compiling vhdl file "CPU_BRANCH_CTRL/branch_ctrl.vhd" in Library work.
Entity <branch_ctrl> compiled.	Entity <branch_ctrl> compiled.
Entity <branch_ctrl> (Architecture <ideal>) compiled.	Entity <branch_ctrl> (Architecture <=>) compiled.
Total REAL time to Xst completion: 1.68 secs	Total REAL time to Xst completion: 4.00 secs
Total CPU time to Xst completion: 0.40 secs	Total CPU time to Xst completion: 3.27 secs
->	->
Total memory usage is 4477148 kilobytes	Total memory usage is 4477120 kilobytes
Number of errors : 0 ( 0 filtered)	Number of errors : 0 ( 0 filtered)
Number of warnings : 1 ( 0 filtered)	Number of warnings : 1 ( 0 filtered)
Number of infos : 0 ( 0 filtered)	Number of infos : 0 ( 0 filtered)
*Use incremental -o branch_ctrl.tb isim beh.exe -pri branch_ctrl.tb.pri -top branch_ctrl.tb	*Use incremental -o branch_ctrl.tb isim beh.exe -pri branch_ctrl.tb.pri -top branch_ctrl.tb
(Sim P.20131013 (signature 0x7708090))	(Sim P.20131013 (signature 0x7708090))
Number of CPUs detected in this system: 8	Number of CPUs detected in this system: 8
Turning on multi-threading, number of parallel sub-compilation jobs: 16	Turning on multi-threading, number of parallel sub-compilation jobs: 16
Determining compilation order of HDL files	Determining compilation order of HDL files
Parsing VHDL file "muxento1.vhd" into library work	Parsing VHDL file "muxento1.vhd" into library work
Parsing VHDL file "gf1.vhd" into library work	Parsing VHDL file "gf1.vhd" into library work
Parsing VHDL file "req_file_functions.vhd" into library work	Parsing VHDL file "req_file_functions.vhd" into library work
Parsing VHDL file "muxdff.vhd" into library work	Parsing VHDL file "muxdff.vhd" into library work
Parsing VHDL file "cia_gp.vhd" into library work	Parsing VHDL file "cia_gp.vhd" into library work
Parsing VHDL file "muxento1_bus.vhd" into library work	Parsing VHDL file "muxento1_bus.vhd" into library work
Parsing VHDL file "counter.vhd" into library work	Parsing VHDL file "counter.vhd" into library work
Parsing VHDL file "cia_add_n_bit.vhd" into library work	Parsing VHDL file "cia_add_n_bit.vhd" into library work
Parsing VHDL file "branch_ctrl_functions.vhd" into library work	Parsing VHDL file "branch_ctrl_functions.vhd" into library work
Parsing VHDL file "branch_ctrl.vhd" into library work	Parsing VHDL file "branch_ctrl.vhd" into library work
Parsing VHDL file "branch_ctrl_tb.vhd" into library work	Parsing VHDL file "branch_ctrl_tb.vhd" into library work
Starting static elaboration	Starting static elaboration
Completed static elaboration	Completed static elaboration
Compiling package standard	Compiling package standard

>xst -fhn branch_ctrl.xst	>xst -fhn branch_ctrl.xst
Release 14.7 - xst P.20131013 (n64)	Release 14.7 - xst P.20131013 (n64)
Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.	Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.
-> Parameter TMPDIR set to /xstprocnar/tmp	-> Parameter TMPDIR set to /xstprocnar/tmp
Total REAL time to Xst completion: 0.00 secs	Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.25 secs	Total CPU time to Xst completion: 0.24 secs
-> WARNING:Xst:3164 - Option "-debug" found multiple times in the command line. Only the first occurrence is considered.	-> WARNING:Xst:3164 - Option "-debug" found multiple times in the command line. Only the first occurrence is considered.
HDL Compiler	HDL Compiler
Compiling vhdl file "CPU_BRANCH_CTRL/muxento1.vhd" in Library work.	Compiling vhdl file "CPU_BRANCH_CTRL/muxento1.vhd" in Library work.
Entity <muxento1> compiled.	Entity <muxento1> compiled.
Entity <muxento1> (Architecture <ideal>) compiled.	Entity <muxento1> (Architecture <=>) compiled.
Compiling vhdl file "CPU_BRANCH_CTRL/gff.vhd" in Library work.	Compiling vhdl file "CPU_BRANCH_CTRL/gff.vhd" in Library work.
Entity <gff> compiled.	Entity <gff> compiled.
Entity <gff> (Architecture <ideal>) compiled.	Entity <gff> (Architecture <=>) compiled.
Compiling vhdl file "CPU_BRANCH_CTRL/cia_ap.vhd" in Library work.	Compiling vhdl file "CPU_BRANCH_CTRL/cia_ap.vhd" in Library work.
Entity <cia_ap> compiled.	Entity <cia_ap> compiled.
Entity <cia_ap> (Architecture <ideal>) compiled.	Entity <cia_ap> (Architecture <=>) compiled.
Compiling vhdl file "CPU_BRANCH_CTRL/req_file_functions.vhd" in Library work.	Compiling vhdl file "CPU_BRANCH_CTRL/req_file_functions.vhd" in Library work.
Package <req_file_functions> compiled.	Package <req_file_functions> compiled.
Package body <req_file_functions> compiled.	Package body <req_file_functions> compiled.
Compiling vhdl file "CPU_BRANCH_CTRL/muxdff.vhd" in Library work.	Compiling vhdl file "CPU_BRANCH_CTRL/muxdff.vhd" in Library work.
Entity <muxdff> compiled.	Entity <muxdff> compiled.
Entity <muxdff> (Architecture <ideal>) compiled.	Entity <muxdff> (Architecture <=>) compiled.
Compiling vhdl file "CPU_BRANCH_CTRL/branch_ctrl_functions.vhd" in Library work.	Compiling vhdl file "CPU_BRANCH_CTRL/branch_ctrl_functions.vhd" in Library work.
Package <branch_ctrl_functions> compiled.	Package <branch_ctrl_functions> compiled.
Package body <branch_ctrl_functions> compiled.	Package body <branch_ctrl_functions> compiled.
Compiling vhdl file "CPU_BRANCH_CTRL/counter.vhd" in Library work.	Compiling vhdl file "CPU_BRANCH_CTRL/counter.vhd" in Library work.
Entity <counter> compiled.	Entity <counter> compiled.
Entity <counter> (Architecture <ideal>) compiled.	Entity <counter> (Architecture <=>) compiled.
Compiling vhdl file "CPU_BRANCH_CTRL/muxento1_bus.vhd" in Library work.	Compiling vhdl file "CPU_BRANCH_CTRL/muxento1_bus.vhd" in Library work.
Entity <muxento1_bus> compiled.	Entity <muxento1_bus> compiled.
Entity <muxento1_bus> (Architecture <ideal>) compiled.	Entity <muxento1_bus> (Architecture <=>) compiled.
Compiling vhdl file "CPU_BRANCH_CTRL/cia_add_n_bit.vhd" in Library work.	Compiling vhdl file "CPU_BRANCH_CTRL/cia_add_n_bit.vhd" in Library work.
Entity <cia_add_n_bit> compiled.	Entity <cia_add_n_bit> compiled.
Entity <cia_add_n_bit> (Architecture <ideal>) compiled.	Entity <cia_add_n_bit> (Architecture <=>) compiled.
Compiling vhdl file "CPU_BRANCH_CTRL/branch_ctrl.vhd" in Library work.	Compiling vhdl file "CPU_BRANCH_CTRL/branch_ctrl.vhd" in Library work.
Entity <branch_ctrl> compiled.	Entity <branch_ctrl> compiled.
Entity <branch_ctrl> (Architecture <ideal>) compiled.	Entity <branch_ctrl> (Architecture <=>) compiled.
Total REAL time to Xst completion: 0.00 secs	Total REAL time to Xst completion: 4.00 secs
Total CPU time to Xst completion: 0.41 secs	Total CPU time to Xst completion: 3.27 secs
->	->
Total memory usage is 4477124 kilobytes	Total memory usage is 4477120 kilobytes
Number of errors : 0 ( 0 filtered)	Number of errors : 0 ( 0 filtered)
Number of warnings : 1 ( 0 filtered)	Number of warnings : 1 ( 0 filtered)
Number of infos : 0 ( 0 filtered)	Number of infos : 0 ( 0 filtered)
*Use incremental -o branch_ctrl_tb isim beh.exe -pri branch_ctrl_tb.pri -top branch_ctrl_tb	*Use incremental -o branch_ctrl_tb isim beh.exe -pri branch_ctrl_tb.pri -top branch_ctrl_tb
(SIm P.20131013 (signature 0x7708090))	(SIm P.20131013 (signature 0x7708090))
Number of CPUs detected in this system: 8	Number of CPUs detected in this system: 8
Turning on multi-threading, number of parallel sub-compilation jobs: 16	Turning on multi-threading, number of parallel sub-compilation jobs: 16
Determining compilation order of HDL files	Determining compilation order of HDL files
Parsing VHDL file "muxento1.vhd" into library work	Parsing VHDL file "muxento1.vhd" into library work
Parsing VHDL file "gff.vhd" into library work	Parsing VHDL file "gff.vhd" into library work
Parsing VHDL file "cia_ap.vhd" into library work	Parsing VHDL file "cia_ap.vhd" into library work
Parsing VHDL file "muxdff.vhd" into library work	Parsing VHDL file "muxdff.vhd" into library work
Parsing VHDL file "cia_add_n_bit.vhd" into library work	Parsing VHDL file "cia_add_n_bit.vhd" into library work
Parsing VHDL file "counter.vhd" into library work	Parsing VHDL file "counter.vhd" into library work
Parsing VHDL file "branch_ctrl_functions.vhd" into library work	Parsing VHDL file "branch_ctrl_functions.vhd" into library work
Parsing VHDL file "branch_ctrl.vhd" into library work	Parsing VHDL file "branch_ctrl.vhd" into library work
Starting static elaboration	Starting static elaboration
Completed static elaboration	Completed static elaboration
Compiling package standard	Compiling package standard



>xst -fhn branch_ctrl.xst	>xst -fhn branch_ctrl.xst
Release 14.7 - xst P.20131013 (n64)	Release 14.7 - xst P.20131013 (n64)
Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.	Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.
-> Parameter TMPDIR set to /xstprojdir/tmp	-> Parameter TMPDIR set to /xstprojdir/tmp
Total REAL time to Xst completion: 0.00 secs	Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.22 secs	Total CPU time to Xst completion: 0.24 secs
-> WARNING:Xst:3164 - Option "-debug" found multiple times in the command line. Only the first occurrence is considered.	-> WARNING:Xst:3164 - Option "-debug" found multiple times in the command line. Only the first occurrence is considered.
HDL Compiler	HDL Compiler
Compiling vhdl file "CPU_BRANCH_CTRL/muxento1.vhd" in Library work.	Compiling vhdl file "CPU_BRANCH_CTRL/muxento1.vhd" in Library work.
Entity <muxento1> compiled.	Entity <muxento1> compiled.
Entity <muxento1> (Architecture <ideal>) compiled.	Entity <muxento1> (Architecture <=>) compiled.
Compiling vhdl file "CPU_BRANCH_CTRL/gff.vhd" in Library work.	Compiling vhdl file "CPU_BRANCH_CTRL/gff.vhd" in Library work.
Entity <gff> compiled.	Entity <gff> compiled.
Entity <gff> (Architecture <ideal>) compiled.	Entity <gff> (Architecture <=>) compiled.
Compiling vhdl file "CPU_BRANCH_CTRL/req_file_functions.vhd" in Library work.	Compiling vhdl file "CPU_BRANCH_CTRL/req_file_functions.vhd" in Library work.
Package <req_file_functions> compiled.	Package <req_file_functions> compiled.
Package body <req_file_functions> compiled.	Package body <req_file_functions> compiled.
Compiling vhdl file "CPU_BRANCH_CTRL/cia_gp.vhd" in Library work.	Compiling vhdl file "CPU_BRANCH_CTRL/cia_gp.vhd" in Library work.
Entity <cia_gp> compiled.	Entity <cia_gp> compiled.
Entity <cia_gp> (Architecture <ideal>) compiled.	Entity <cia_gp> (Architecture <=>) compiled.
Compiling vhdl file "CPU_BRANCH_CTRL/muxdff.vhd" in Library work.	Compiling vhdl file "CPU_BRANCH_CTRL/muxdff.vhd" in Library work.
Entity <muxdff> compiled.	Entity <muxdff> compiled.
Entity <muxdff> (Architecture <ideal>) compiled.	Entity <muxdff> (Architecture <=>) compiled.
Compiling vhdl file "CPU_BRANCH_CTRL/branch_ctrl_functions.vhd" in Library work.	Compiling vhdl file "CPU_BRANCH_CTRL/branch_ctrl_functions.vhd" in Library work.
Package <branch_ctrl_functions> compiled.	Package <branch_ctrl_functions> compiled.
Package body <branch_ctrl_functions> compiled.	Package body <branch_ctrl_functions> compiled.
Compiling vhdl file "CPU_BRANCH_CTRL/counter.vhd" in Library work.	Compiling vhdl file "CPU_BRANCH_CTRL/counter.vhd" in Library work.
Entity <counter> compiled.	Entity <counter> compiled.
Entity <counter> (Architecture <ideal>) compiled.	Entity <counter> (Architecture <=>) compiled.
Compiling vhdl file "CPU_BRANCH_CTRL/cia_add_n_bit.vhd" in Library work.	Compiling vhdl file "CPU_BRANCH_CTRL/cia_add_n_bit.vhd" in Library work.
Entity <cia_add_n_bit> compiled.	Entity <cia_add_n_bit> compiled.
Entity <cia_add_n_bit> (Architecture <ideal>) compiled.	Entity <cia_add_n_bit> (Architecture <=>) compiled.
Compiling vhdl file "CPU_BRANCH_CTRL/muxento1_bus.vhd" in Library work.	Compiling vhdl file "CPU_BRANCH_CTRL/muxento1_bus.vhd" in Library work.
Entity <muxento1_bus> compiled.	Entity <muxento1_bus> compiled.
Entity <muxento1_bus> (Architecture <ideal>) compiled.	Entity <muxento1_bus> (Architecture <=>) compiled.
Compiling vhdl file "CPU_BRANCH_CTRL/branch_ctrl.vhd" in Library work.	Compiling vhdl file "CPU_BRANCH_CTRL/branch_ctrl.vhd" in Library work.
Entity <branch_ctrl> compiled.	Entity <branch_ctrl> compiled.
Entity <branch_ctrl> (Architecture <ideal>) compiled.	Entity <branch_ctrl> (Architecture <=>) compiled.
Total REAL time to Xst completion: 1.66 secs	Total REAL time to Xst completion: 4.00 secs
Total CPU time to Xst completion: 1.67 secs	Total CPU time to Xst completion: 3.27 secs
->	->
Total memory usage is 4477132 kilobytes	Total memory usage is 4477120 kilobytes
Number of errors : 0 ( 0 filtered)	Number of errors : 0 ( 0 filtered)
Number of warnings : 1 ( 0 filtered)	Number of warnings : 1 ( 0 filtered)
Number of infos : 0 ( 0 filtered)	Number of infos : 0 ( 0 filtered)
*Use incremental -o branch_ctrl_tb isim beh.exe -pri branch_ctrl_tb.pri -top branch_ctrl_tb	*Use incremental -o branch_ctrl_tb isim beh.exe -pri branch_ctrl_tb.pri -top branch_ctrl_tb
(Sim P.20131013 (signature 0x7708090))	(Sim P.20131013 (signature 0x7708090))
Number of CPUs detected in this system: 8	Number of CPUs detected in this system: 8
Turning on multi-threading, number of parallel sub-compilation jobs: 16	Turning on multi-threading, number of parallel sub-compilation jobs: 16
Determining compilation order of HDL files	Determining compilation order of HDL files
Parsing VHDL file "muxento1.vhd" into library work	Parsing VHDL file "muxento1.vhd" into library work
Parsing VHDL file "req_file_functions.vhd" into library work	Parsing VHDL file "req_file_functions.vhd" into library work
Parsing VHDL file "muxdff.vhd" into library work	Parsing VHDL file "muxdff.vhd" into library work
Parsing VHDL file "cia_gp.vhd" into library work	Parsing VHDL file "cia_gp.vhd" into library work
Parsing VHDL file "muxento1_bus.vhd" into library work	Parsing VHDL file "muxento1_bus.vhd" into library work
Parsing VHDL file "counter.vhd" into library work	Parsing VHDL file "counter.vhd" into library work
Parsing VHDL file "cia_add_n_bit.vhd" into library work	Parsing VHDL file "cia_add_n_bit.vhd" into library work
Parsing VHDL file "branch_ctrl_functions.vhd" into library work	Parsing VHDL file "branch_ctrl_functions.vhd" into library work
Parsing VHDL file "branch_ctrl.vhd" into library work	Parsing VHDL file "branch_ctrl.vhd" into library work
Parsing VHDL file "branch_ctrl_tb.vhd" into library work	Parsing VHDL file "branch_ctrl_tb.vhd" into library work
Starting static elaboration	Starting static elaboration
Completed static elaboration	Completed static elaboration
Compiling package standard	Compiling package standard

>xst -fh branch ctrl.xst	>xst -fh branch ctrl.xst
Release 14.7 - xst P 20131013 (n64)	Release 14.7 - xst P 20131013 (n64)
Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.	Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.
-> Parameter TMPDIR set to /xstprojdir/tmp	-> Parameter TMPDIR set to /xstprojdir/tmp
Total REAL time to Xst completion: 0.00 secs	Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.25 secs	Total CPU time to Xst completion: 0.24 secs
-> WARNING:Xst:3164 - Option "-debug" found multiple times in the command line. Only the first occurrence is considered.	-> WARNING:Xst:3164 - Option "-debug" found multiple times in the command line. Only the first occurrence is considered.
* HDL Compilation *	* HDL Compilation *
Compiling vhdl file "CPU_BRANCH_CTRL/muxnto1.vhd" in Library work.	Compiling vhdl file "CPU_BRANCH_CTRL/muxnto1.vhd" in Library work.
Entity <muxnto1> compiled.	Entity <muxnto1> compiled.
Entity <muxnto1? (Architecture <ideaab>) compiled.	Entity <muxnto1? (Architecture <=>) compiled.
Compiling vhdl file "CPU_BRANCH_CTRL/iff.vhd" in Library work.	Compiling vhdl file "CPU_BRANCH_CTRL/iff.vhd" in Library work.
Entity <iff> compiled.	Entity <iff> compiled.
Entity <iff? (Architecture <ideaab>) compiled.	Entity <iff? (Architecture <=>) compiled.
Compiling vhdl file "CPU_BRANCH_CTRL/ireq file functions.vhd" in Library work.	Compiling vhdl file "CPU_BRANCH_CTRL/ireq file functions.vhd" in Library work.
Package <ireq file functions> compiled.	Entity <ia_ireq> compiled.
Package body <ireq file functions> compiled.	Entity <ia_ireq? (Architecture <=>) compiled.
Compiling vhdl file "CPU_BRANCH_CTRL/icla_ireq.vhd" in Library work.	Compiling vhdl file "CPU_BRANCH_CTRL/ireq file functions.vhd" in Library work.
Entity <icla_ireq> compiled.	Package <ireq file functions> compiled.
Entity <icla_ireq? (Architecture <ideaab>) compiled.	Package body <ireq file functions> compiled.
Compiling vhdl file "CPU_BRANCH_CTRL/muxdff.vhd" in Library work.	Compiling vhdl file "CPU_BRANCH_CTRL/muxdff.vhd" in Library work.
Entity <muxdff> compiled.	Entity <muxdff? compiled.
Entity <muxdff? (Architecture <ideaab>) compiled.	Entity <muxdff? (Architecture <=>) compiled.
Compiling vhdl file "CPU_BRANCH_CTRL/branch_ctrl functions.vhd" in Library work.	Compiling vhdl file "CPU_BRANCH_CTRL/branch_ctrl functions.vhd" in Library work.
Package <branch_ctrl functions> compiled.	Package <branch_ctrl functions> compiled.
Package body <branch_ctrl functions> compiled.	Package body <branch_ctrl functions> compiled.
Compiling vhdl file "CPU_BRANCH_CTRL/counter.vhd" in Library work.	Compiling vhdl file "CPU_BRANCH_CTRL/counter.vhd" in Library work.
Entity <counter> compiled.	Entity <counter> compiled.
Entity <counter? (Architecture <ideaab>) compiled.	Entity <counter? (Architecture <=>) compiled.
Compiling vhdl file "CPU_BRANCH_CTRL/icla_add_n_bit.vhd" in Library work.	Compiling vhdl file "CPU_BRANCH_CTRL/muxnto1_bus.vhd" in Library work.
Entity <icla_add_n_bit> compiled.	Entity <muxnto1_bus> compiled.
Entity <icla_add_n_bit? (Architecture <ideaab>) compiled.	Entity <muxnto1_bus? (Architecture <=>) compiled.
Compiling vhdl file "CPU_BRANCH_CTRL/muxnto1_bus.vhd" in Library work.	Compiling vhdl file "CPU_BRANCH_CTRL/icla_add_n_bit.vhd" in Library work.
Entity <muxnto1_bus> compiled.	Entity <icla_add_n_bit> compiled.
Entity <muxnto1_bus? (Architecture <ideaab>) compiled.	Entity <icla_add_n_bit? (Architecture <=>) compiled.
Compiling vhdl file "CPU_BRANCH_CTRL/branch_ctrl.vhd" in Library work.	Compiling vhdl file "CPU_BRANCH_CTRL/branch_ctrl.vhd" in Library work.
Entity <branch_ctrl> compiled.	Entity <branch_ctrl> compiled.
ERROR:HDLParasim:351 - "CPU_BRANCH_CTRL/branch_ctrl.vhd" Line 71: Formal x of counter with no default value must be associated with an actual value.	Entity <branch_ctrl? (Architecture <=>) compiled.
Total REAL time to Xst completion: 2.00 secs	Total REAL time to Xst completion: 4.00 secs
Total CPU time to Xst completion: 1.56 secs	Total CPU time to Xst completion: 3.27 secs
->	->
Total memory usage is 4477100 kilobytes	Total memory usage is 4477120 kilobytes
Number of errors : 1 ( 0 filtered)	Number of errors : 0 ( 0 filtered)
Number of warnings : 1 ( 0 filtered)	Number of warnings : 1 ( 0 filtered)
Number of infos : 0 ( 0 filtered)	Number of infos : 0 ( 0 filtered)
->Use incremental ->branch_ctrl.tb.isim_beh.exe -pri branch_ctrl.tb.pri -top branch_ctrl.tb	->Use incremental ->branch_ctrl.tb.isim_beh.exe -pri branch_ctrl.tb.pri -top branch_ctrl.tb
(Sim P 20131013 signature 0a7708d90)	(Sim P 20131013 signature 0a7708d90)
Number of CPUs detected in this system: 8	Number of CPUs detected in this system: 8
Turning on multi-threading: number of parallel sub-compilation jobs: 16	Turning on multi-threading: number of parallel sub-compilation jobs: 16
Determining compilation order of HDL files	Determining compilation order of HDL files
Parsing VHDL file "muxnto1.vhd" into library work	Parsing VHDL file "muxnto1.vhd" into library work
Parsing VHDL file "iff.vhd" into library work	Parsing VHDL file "iff.vhd" into library work
Parsing VHDL file "ireq file functions.vhd" into library work	Parsing VHDL file "ireq file functions.vhd" into library work
Parsing VHDL file "muxdff.vhd" into library work	Parsing VHDL file "muxdff.vhd" into library work
Parsing VHDL file "icla_ireq.vhd" into library work	Parsing VHDL file "icla_ireq.vhd" into library work
Parsing VHDL file "muxnto1_bus.vhd" into library work	Parsing VHDL file "muxnto1_bus.vhd" into library work
Parsing VHDL file "counter.vhd" into library work	Parsing VHDL file "counter.vhd" into library work
Parsing VHDL file "icla_add_n_bit.vhd" into library work	Parsing VHDL file "icla_add_n_bit.vhd" into library work
Parsing VHDL file "branch_ctrl functions.vhd" into library work	Parsing VHDL file "branch_ctrl functions.vhd" into library work
Parsing VHDL file "branch_ctrl.vhd" into library work	Parsing VHDL file "branch_ctrl.vhd" into library work
VHDL file branch_ctrl.vhd ignored due to errors	Parsing VHDL file "branch_ctrl.tb.vhd" into library work
->branch_ctrl.tb.isim_beh.exe -sbatch isim.tcl -with branch_ctrl.tb.isim_beh.wdb	Starting static elaboration
	Completed static elaboration
	Compiling package standard

>xst -fHn branch_ctrl.xst	>xst -fHn branch_ctrl.xst
Release 14.7 - xst P.20131013 (n64)	Release 14.7 - xst P.20131013 (n64)
Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.	Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.
-> Parameter TMPDIR set to /xst/bin/par/tmp	-> Parameter TMPDIR set to /xst/bin/par/tmp
Total REAL time to Xst completion: 0.00 secs	Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.24 secs	Total CPU time to Xst completion: 0.24 secs
-> WARNING:Xst:3164 - Option "-debug" found multiple times in the command line. Only the first occurrence is considered.	-> WARNING:Xst:3164 - Option "-debug" found multiple times in the command line. Only the first occurrence is considered.
HDL Compiler	HDL Compiler
Compiling vhdl file "CPU_BRANCH_CTRL/muxento1.vhd" in Library work.	Compiling vhdl file "CPU_BRANCH_CTRL/muxento1.vhd" in Library work.
Entity <muxento1> compiled.	Entity <muxento1> compiled.
Entity <muxento1> (Architecture <ideal>) compiled.	Entity <muxento1> (Architecture <=>) compiled.
Compiling vhdl file "CPU_BRANCH_CTRL/gff.vhd" in Library work.	Compiling vhdl file "CPU_BRANCH_CTRL/gff.vhd" in Library work.
Entity <gff> compiled.	Entity <gff> compiled.
Entity <gff> (Architecture <ideal>) compiled.	Entity <gff> (Architecture <=>) compiled.
Compiling vhdl file "CPU_BRANCH_CTRL/req_file_functions.vhd" in Library work.	Compiling vhdl file "CPU_BRANCH_CTRL/icla_gp.vhd" in Library work.
Package <req_file_functions> compiled.	Entity <icla_gp> compiled.
Package body <req_file_functions> compiled.	Entity <icla_gp> (Architecture <=>) compiled.
Compiling vhdl file "CPU_BRANCH_CTRL/icla_gp.vhd" in Library work.	Compiling vhdl file "CPU_BRANCH_CTRL/req_file_functions.vhd" in Library work.
Entity <icla_gp> compiled.	Package <req_file_functions> compiled.
Entity <icla_gp> (Architecture <ideal>) compiled.	Package body <req_file_functions> compiled.
Compiling vhdl file "CPU_BRANCH_CTRL/muxdff.vhd" in Library work.	Compiling vhdl file "CPU_BRANCH_CTRL/muxdff.vhd" in Library work.
Entity <muxdff> compiled.	Entity <muxdff> compiled.
Entity <muxdff> (Architecture <ideal>) compiled.	Entity <muxdff> (Architecture <=>) compiled.
Compiling vhdl file "CPU_BRANCH_CTRL/branch_ctrl_functions.vhd" in Library work.	Compiling vhdl file "CPU_BRANCH_CTRL/branch_ctrl_functions.vhd" in Library work.
Package <branch_ctrl_functions> compiled.	Package <branch_ctrl_functions> compiled.
Package body <branch_ctrl_functions> compiled.	Package body <branch_ctrl_functions> compiled.
Compiling vhdl file "CPU_BRANCH_CTRL/counter.vhd" in Library work.	Compiling vhdl file "CPU_BRANCH_CTRL/counter.vhd" in Library work.
Entity <counter> compiled.	Entity <counter> compiled.
Entity <counter> (Architecture <ideal>) compiled.	Entity <counter> (Architecture <=>) compiled.
Compiling vhdl file "CPU_BRANCH_CTRL/icla_add_n_bit.vhd" in Library work.	Compiling vhdl file "CPU_BRANCH_CTRL/muxento1_bus.vhd" in Library work.
Entity <icla_add_n_bit> compiled.	Entity <muxento1_bus> compiled.
Entity <icla_add_n_bit> (Architecture <ideal>) compiled.	Entity <muxento1_bus> (Architecture <=>) compiled.
Compiling vhdl file "CPU_BRANCH_CTRL/muxento1_bus.vhd" in Library work.	Compiling vhdl file "CPU_BRANCH_CTRL/icla_add_n_bit.vhd" in Library work.
Entity <muxento1_bus> compiled.	Entity <icla_add_n_bit> compiled.
Entity <muxento1_bus> (Architecture <ideal>) compiled.	Entity <icla_add_n_bit> (Architecture <=>) compiled.
Compiling vhdl file "CPU_BRANCH_CTRL/branch_ctrl.vhd" in Library work.	Compiling vhdl file "CPU_BRANCH_CTRL/branch_ctrl.vhd" in Library work.
Entity <branch_ctrl> compiled.	Entity <branch_ctrl> compiled.
Entity <branch_ctrl> (Architecture <ideal>) compiled.	Entity <branch_ctrl> (Architecture <=>) compiled.
Total REAL time to Xst completion: 1.66 secs	Total REAL time to Xst completion: 4.00 secs
Total CPU time to Xst completion: 1.22 secs	Total CPU time to Xst completion: 3.27 secs
->	->
Total memory usage is 4477136 kilobytes	Total memory usage is 4477120 kilobytes
Number of errors : 0 ( 0 filtered)	Number of errors : 0 ( 0 filtered)
Number of warnings : 1 ( 0 filtered)	Number of warnings : 1 ( 0 filtered)
Number of infos : 0 ( 0 filtered)	Number of infos : 0 ( 0 filtered)
*Use incremental -o branch_ctrl_tb isim beh.exe -pri branch_ctrl_tb.pri -top branch_ctrl_tb	*Use incremental -o branch_ctrl_tb isim beh.exe -pri branch_ctrl_tb.pri -top branch_ctrl_tb
(Sim P.20131013 (signature 0x7708090))	(Sim P.20131013 (signature 0x7708090))
Number of CPUs detected in this system: 8	Number of CPUs detected in this system: 8
Turning on multi-threading, number of parallel sub-compilation jobs: 16	Turning on multi-threading, number of parallel sub-compilation jobs: 16
Determining compilation order of HDL files	Determining compilation order of HDL files
Parsing VHDL file "muxento1.vhd" into library work	Parsing VHDL file "muxento1.vhd" into library work
Parsing VHDL file "gff.vhd" into library work	Parsing VHDL file "gff.vhd" into library work
Parsing VHDL file "req_file_functions.vhd" into library work	Parsing VHDL file "req_file_functions.vhd" into library work
Parsing VHDL file "muxdff.vhd" into library work	Parsing VHDL file "muxdff.vhd" into library work
Parsing VHDL file "icla_gp.vhd" into library work	Parsing VHDL file "icla_gp.vhd" into library work
Parsing VHDL file "muxento1_bus.vhd" into library work	Parsing VHDL file "muxento1_bus.vhd" into library work
Parsing VHDL file "counter.vhd" into library work	Parsing VHDL file "counter.vhd" into library work
Parsing VHDL file "icla_add_n_bit.vhd" into library work	Parsing VHDL file "icla_add_n_bit.vhd" into library work
Parsing VHDL file "branch_ctrl_functions.vhd" into library work	Parsing VHDL file "branch_ctrl_functions.vhd" into library work
Parsing VHDL file "branch_ctrl.vhd" into library work	Parsing VHDL file "branch_ctrl.vhd" into library work
Parsing VHDL file "branch_ctrl_tb.vhd" into library work	Parsing VHDL file "branch_ctrl_tb.vhd" into library work
Starting static elaboration	Starting static elaboration
Completed static elaboration	Completed static elaboration
Compiling package standard	Compiling package standard

>xst -fHn branch_ctrl.xst	>xst -fHn branch_ctrl.xst
Release 14.7 - xst P.20131013 (n64)	Release 14.7 - xst P.20131013 (n64)
Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.	Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.
-> Parameter TMPDIR set to /xstprojdir/tmp	-> Parameter TMPDIR set to /xstprojdir/tmp
Total REAL time to Xst completion: 1.68 secs	Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.27 secs	Total CPU time to Xst completion: 0.24 secs
-> WARNING:Xst:3164 - Option "-debug" found multiple times in the command line. Only the first occurrence is considered.	-> WARNING:Xst:3164 - Option "-debug" found multiple times in the command line. Only the first occurrence is considered.
HDL Compiler	HDL Compiler
Compiling vhdl file "CPU_BRANCH_CTRL/muxento1.vhd" in Library work.	Compiling vhdl file "CPU_BRANCH_CTRL/muxento1.vhd" in Library work.
Entity <muxento1> compiled.	Entity <muxento1> compiled.
Entity <muxento1> (Architecture <ideal>) compiled.	Entity <muxento1> (Architecture <=>) compiled.
Compiling vhdl file "CPU_BRANCH_CTRL/gf1.vhd" in Library work.	Compiling vhdl file "CPU_BRANCH_CTRL/gf1.vhd" in Library work.
Entity <gf1> compiled.	Entity <gf1> compiled.
Entity <gf1> (Architecture <ideal>) compiled.	Entity <gf1> (Architecture <=>) compiled.
Compiling vhdl file "CPU_BRANCH_CTRL/req_file_functions.vhd" in Library work.	Compiling vhdl file "CPU_BRANCH_CTRL/req_file_functions.vhd" in Library work.
Package <req_file_functions> compiled.	Package <req_file_functions> compiled.
Package body <req_file_functions> compiled.	Package body <req_file_functions> compiled.
Compiling vhdl file "CPU_BRANCH_CTRL/cia_gp.vhd" in Library work.	Compiling vhdl file "CPU_BRANCH_CTRL/cia_gp.vhd" in Library work.
Entity <cia_gp> compiled.	Entity <cia_gp> compiled.
Entity <cia_gp> (Architecture <ideal>) compiled.	Entity <cia_gp> (Architecture <=>) compiled.
Compiling vhdl file "CPU_BRANCH_CTRL/muxdff.vhd" in Library work.	Compiling vhdl file "CPU_BRANCH_CTRL/muxdff.vhd" in Library work.
Entity <muxdff> compiled.	Entity <muxdff> compiled.
Entity <muxdff> (Architecture <ideal>) compiled.	Entity <muxdff> (Architecture <=>) compiled.
Compiling vhdl file "CPU_BRANCH_CTRL/branch_ctrl_functions.vhd" in Library work.	Compiling vhdl file "CPU_BRANCH_CTRL/branch_ctrl_functions.vhd" in Library work.
Package <branch_ctrl_functions> compiled.	Package <branch_ctrl_functions> compiled.
Package body <branch_ctrl_functions> compiled.	Package body <branch_ctrl_functions> compiled.
Compiling vhdl file "CPU_BRANCH_CTRL/counter.vhd" in Library work.	Compiling vhdl file "CPU_BRANCH_CTRL/counter.vhd" in Library work.
Entity <counter> compiled.	Entity <counter> compiled.
Entity <counter> (Architecture <ideal>) compiled.	Entity <counter> (Architecture <=>) compiled.
Compiling vhdl file "CPU_BRANCH_CTRL/cia_add_n_bit.vhd" in Library work.	Compiling vhdl file "CPU_BRANCH_CTRL/cia_add_n_bit.vhd" in Library work.
Entity <cia_add_n_bit> compiled.	Entity <cia_add_n_bit> compiled.
Entity <cia_add_n_bit> (Architecture <ideal>) compiled.	Entity <cia_add_n_bit> (Architecture <=>) compiled.
Compiling vhdl file "CPU_BRANCH_CTRL/muxento1_bus.vhd" in Library work.	Compiling vhdl file "CPU_BRANCH_CTRL/muxento1_bus.vhd" in Library work.
Entity <muxento1_bus> compiled.	Entity <muxento1_bus> compiled.
Entity <muxento1_bus> (Architecture <ideal>) compiled.	Entity <muxento1_bus> (Architecture <=>) compiled.
Compiling vhdl file "CPU_BRANCH_CTRL/branch_ctrl.vhd" in Library work.	Compiling vhdl file "CPU_BRANCH_CTRL/branch_ctrl.vhd" in Library work.
Entity <branch_ctrl> compiled.	Entity <branch_ctrl> compiled.
Entity <branch_ctrl> (Architecture <ideal>) compiled.	Entity <branch_ctrl> (Architecture <=>) compiled.
Total REAL time to Xst completion: 3.68 secs	Total REAL time to Xst completion: 4.00 secs
Total CPU time to Xst completion: 2.38 secs	Total CPU time to Xst completion: 3.27 secs
->	->
Total memory usage is 4477112 kilobytes	Total memory usage is 4477120 kilobytes
Number of errors : 0 ( 0 filtered)	Number of errors : 0 ( 0 filtered)
Number of warnings : 1 ( 0 filtered)	Number of warnings : 1 ( 0 filtered)
Number of infos : 0 ( 0 filtered)	Number of infos : 0 ( 0 filtered)
*Use incremental -o branch_ctrl_tb isim beh.exe -pri branch_ctrl_tb.pri -top branch_ctrl_tb	*Use incremental -o branch_ctrl_tb isim beh.exe -pri branch_ctrl_tb.pri -top branch_ctrl_tb
(Sim P.20131013 (signature 0x7708090))	(Sim P.20131013 (signature 0x7708090))
Number of CPUs detected in this system: 8	Number of CPUs detected in this system: 8
Turning on multi-threading, number of parallel sub-compilation jobs: 16	Turning on multi-threading, number of parallel sub-compilation jobs: 16
Determining compilation order of HDL files	Determining compilation order of HDL files
Parsing VHDL file "muxento1.vhd" into library work	Parsing VHDL file "muxento1.vhd" into library work
Parsing VHDL file "gf1.vhd" into library work	Parsing VHDL file "gf1.vhd" into library work
Parsing VHDL file "req_file_functions.vhd" into library work	Parsing VHDL file "req_file_functions.vhd" into library work
Parsing VHDL file "muxdff.vhd" into library work	Parsing VHDL file "muxdff.vhd" into library work
Parsing VHDL file "cia_gp.vhd" into library work	Parsing VHDL file "cia_gp.vhd" into library work
Parsing VHDL file "muxento1_bus.vhd" into library work	Parsing VHDL file "muxento1_bus.vhd" into library work
Parsing VHDL file "counter.vhd" into library work	Parsing VHDL file "counter.vhd" into library work
Parsing VHDL file "cia_add_n_bit.vhd" into library work	Parsing VHDL file "cia_add_n_bit.vhd" into library work
Parsing VHDL file "branch_ctrl_functions.vhd" into library work	Parsing VHDL file "branch_ctrl_functions.vhd" into library work
Parsing VHDL file "branch_ctrl.vhd" into library work	Parsing VHDL file "branch_ctrl.vhd" into library work
Parsing VHDL file "branch_ctrl_tb.vhd" into library work	Parsing VHDL file "branch_ctrl_tb.vhd" into library work
Starting static elaboration	Starting static elaboration
Completed static elaboration	Completed static elaboration
Compiling package standard	Compiling package standard

>set -fh branch ctrl.vst	>set -fh branch ctrl.vst
Release 14.7 - xst P 20131013 (n64)	Release 14.7 - xst P 20131013 (n64)
Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.	Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.
-> Parameter TMPDIR set to /xstprojdir/tmp	-> Parameter TMPDIR set to /xstprojdir/tmp
Total REAL time to Xst completion: 0.00 secs	Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.26 secs	Total CPU time to Xst completion: 0.24 secs
-> WARNING:Xst:3164 - Option "-debug" found multiple times in the command line. Only the first occurrence is considered.	-> WARNING:Xst:3164 - Option "-debug" found multiple times in the command line. Only the first occurrence is considered.
* HDL Compilation *	* HDL Compilation *
Compiling vhdl file "CPU_BRANCH_CTRL/muxonto1.vhd" in Library work.	Compiling vhdl file "CPU_BRANCH_CTRL/muxonto1.vhd" in Library work.
Entity <muxonto1> compiled.	Entity <muxonto1> compiled.
Entity <muxonto1? (Architecture <ideaab>) compiled.	Entity <muxonto1? (Architecture <=>) compiled.
Compiling vhdl file "CPU_BRANCH_CTRL/iddf.vhd" in Library work.	Compiling vhdl file "CPU_BRANCH_CTRL/iddf.vhd" in Library work.
Entity <iddf> compiled.	Entity <iddf> compiled.
Entity <iddf? (Architecture <ideaab>) compiled.	Entity <iddf? (Architecture <=>) compiled.
Compiling vhdl file "CPU_BRANCH_CTRL/ireq file functions.vhd" in Library work.	Compiling vhdl file "CPU_BRANCH_CTRL/ireq file functions.vhd" in Library work.
Package <ireq file functions> compiled.	Entity <icla ap> compiled.
Package body <ireq file functions> compiled.	Entity <icla ap> (Architecture <=>) compiled.
Compiling vhdl file "CPU_BRANCH_CTRL/icla ap.vhd" in Library work.	Compiling vhdl file "CPU_BRANCH_CTRL/ireq file functions.vhd" in Library work.
Entity <icla ap> compiled.	Package <ireq file functions> compiled.
Entity <icla ap> (Architecture <ideaab>) compiled.	Package body <ireq file functions> compiled.
Compiling vhdl file "CPU_BRANCH_CTRL/muxdff.vhd" in Library work.	Compiling vhdl file "CPU_BRANCH_CTRL/muxdff.vhd" in Library work.
Entity <muxdff> compiled.	Entity <muxdff> compiled.
Entity <muxdff? (Architecture <ideaab>) compiled.	Entity <muxdff? (Architecture <=>) compiled.
Compiling vhdl file "CPU_BRANCH_CTRL/branch ctrl functions.vhd" in Library work.	Compiling vhdl file "CPU_BRANCH_CTRL/branch ctrl functions.vhd" in Library work.
Package <branch ctrl functions> compiled.	Package <branch ctrl functions> compiled.
Package body <branch ctrl functions> compiled.	Package body <branch ctrl functions> compiled.
Compiling vhdl file "CPU_BRANCH_CTRL/counter.vhd" in Library work.	Compiling vhdl file "CPU_BRANCH_CTRL/counter.vhd" in Library work.
Entity <counter> compiled.	Entity <counter> compiled.
Entity <counter? (Architecture <ideaab>) compiled.	Entity <counter? (Architecture <=>) compiled.
Compiling vhdl file "CPU_BRANCH_CTRL/icla add n bit.vhd" in Library work.	Compiling vhdl file "CPU_BRANCH_CTRL/muxonto1 bus.vhd" in Library work.
Entity <icla add n bit> compiled.	Entity <muxonto1 bus> compiled.
Entity <icla add n bit? (Architecture <ideaab>) compiled.	Entity <muxonto1 bus? (Architecture <=>) compiled.
Compiling vhdl file "CPU_BRANCH_CTRL/muxonto1 bus.vhd" in Library work.	Compiling vhdl file "CPU_BRANCH_CTRL/icla add n bit.vhd" in Library work.
Entity <muxonto1 bus> compiled.	Entity <icla add n bit> compiled.
Entity <muxonto1 bus? (Architecture <ideaab>) compiled.	Entity <icla add n bit? (Architecture <=>) compiled.
Compiling vhdl file "CPU_BRANCH_CTRL/branch ctrl.vhd" in Library work.	Compiling vhdl file "CPU_BRANCH_CTRL/branch ctrl.vhd" in Library work.
Entity <branch ctrl> compiled.	Entity <branch ctrl> compiled.
Entity <branch ctrl? (Architecture <ideaab>) compiled.	Entity <branch ctrl? (Architecture <=>) compiled.
Total REAL time to Xst completion: 1.00 secs	Total REAL time to Xst completion: 4.00 secs
Total CPU time to Xst completion: 1.46 secs	Total CPU time to Xst completion: 3.27 secs
->	->
Total memory usage is 4477124 kilobytes	Total memory usage is 4477120 kilobytes
Number of errors : 0 ( 0 filtered)	Number of errors : 0 ( 0 filtered)
Number of warnings : 1 ( 0 filtered)	Number of warnings : 1 ( 0 filtered)
Number of infos : 0 ( 0 filtered)	Number of infos : 0 ( 0 filtered)
->Use incremental ->branch ctrl.tb aim beh exe -pri branch ctrl.tb pri -top branch ctrl.tb	->Use incremental ->branch ctrl.tb aim beh exe -pri branch ctrl.tb pri -top branch ctrl.tb
(Sim P 20131013 signature 0x7708090)	(Sim P 20131013 signature 0x7708090)
Number of CPUs detected in this system: 8	Number of CPUs detected in this system: 8
Turning on multi-threading: number of parallel sub-compilation jobs: 16	Turning on multi-threading: number of parallel sub-compilation jobs: 16
Determining compilation order of HDL files	Determining compilation order of HDL files
Parsing VHDL file "muxonto1.vhd" into library work	Parsing VHDL file "muxonto1.vhd" into library work
Parsing VHDL file "iddf.vhd" into library work	Parsing VHDL file "iddf.vhd" into library work
Parsing VHDL file "ireq file functions.vhd" into library work	Parsing VHDL file "ireq file functions.vhd" into library work
Parsing VHDL file "muxdff.vhd" into library work	Parsing VHDL file "muxdff.vhd" into library work
Parsing VHDL file "icla ap.vhd" into library work	Parsing VHDL file "icla ap.vhd" into library work
Parsing VHDL file "muxonto1 bus.vhd" into library work	Parsing VHDL file "muxonto1 bus.vhd" into library work
Parsing VHDL file "counter.vhd" into library work	Parsing VHDL file "counter.vhd" into library work
Parsing VHDL file "icla add n bit.vhd" into library work	Parsing VHDL file "icla add n bit.vhd" into library work
Parsing VHDL file "branch ctrl functions.vhd" into library work	Parsing VHDL file "branch ctrl functions.vhd" into library work
Parsing VHDL file "branch ctrl.vhd" into library work	Parsing VHDL file "branch ctrl.vhd" into library work
Parsing VHDL file "branch ctrl.tb.vhd" into library work	Parsing VHDL file "branch ctrl.tb.vhd" into library work
Starting static elaboration	Starting static elaboration
Completed static elaboration	Completed static elaboration
Compiling package standard	Compiling package standard

>xst -fHn branch_ctrl.xst	>xst -fHn branch_ctrl.xst
Release 14.7 - xst P.20131013 (n64)	Release 14.7 - xst P.20131013 (n64)
Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.	Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.
-> Parameter TMPDIR set to /xst/bin/par/tmp	-> Parameter TMPDIR set to /xst/bin/par/tmp
Total REAL time to Xst completion: 0.00 secs	Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.24 secs	Total CPU time to Xst completion: 0.24 secs
-> WARNING:Xst:3164 - Option "-debug" found multiple times in the command line. Only the first occurrence is considered.	-> WARNING:Xst:3164 - Option "-debug" found multiple times in the command line. Only the first occurrence is considered.
- HDL Compilation	- HDL Compilation
Compiling vhdl file "CPU_BRANCH_CTRL/muxento1.vhd" in Library work.	Compiling vhdl file "CPU_BRANCH_CTRL/muxento1.vhd" in Library work.
Entity <muxento1> compiled.	Entity <muxento1> compiled.
Entity <muxento1> (Architecture <ideal>) compiled.	Entity <muxento1> (Architecture <=>) compiled.
Compiling vhdl file "CPU_BRANCH_CTRL/gff.vhd" in Library work.	Compiling vhdl file "CPU_BRANCH_CTRL/gff.vhd" in Library work.
Entity <gff> compiled.	Entity <gff> compiled.
Entity <gff> (Architecture <ideal>) compiled.	Entity <gff> (Architecture <=>) compiled.
Compiling vhdl file "CPU_BRANCH_CTRL/req_file_functions.vhd" in Library work.	Compiling vhdl file "CPU_BRANCH_CTRL/icla_gp.vhd" in Library work.
Package <req_file_functions> compiled.	Entity <icla_gp> compiled.
Package body <req_file_functions> compiled.	Entity <icla_gp> (Architecture <=>) compiled.
Compiling vhdl file "CPU_BRANCH_CTRL/icla_gp.vhd" in Library work.	Compiling vhdl file "CPU_BRANCH_CTRL/req_file_functions.vhd" in Library work.
Entity <icla_gp> compiled.	Package <req_file_functions> compiled.
Entity <icla_gp> (Architecture <ideal>) compiled.	Package body <req_file_functions> compiled.
Compiling vhdl file "CPU_BRANCH_CTRL/muxdff.vhd" in Library work.	Compiling vhdl file "CPU_BRANCH_CTRL/muxdff.vhd" in Library work.
Entity <muxdff> compiled.	Entity <muxdff> compiled.
Entity <muxdff> (Architecture <ideal>) compiled.	Entity <muxdff> (Architecture <=>) compiled.
Compiling vhdl file "CPU_BRANCH_CTRL/branch_ctrl_functions.vhd" in Library work.	Compiling vhdl file "CPU_BRANCH_CTRL/branch_ctrl_functions.vhd" in Library work.
Package <branch_ctrl_functions> compiled.	Package <branch_ctrl_functions> compiled.
Package body <branch_ctrl_functions> compiled.	Package body <branch_ctrl_functions> compiled.
Compiling vhdl file "CPU_BRANCH_CTRL/counter.vhd" in Library work.	Compiling vhdl file "CPU_BRANCH_CTRL/counter.vhd" in Library work.
Entity <counter> compiled.	Entity <counter> compiled.
Entity <counter> (Architecture <ideal>) compiled.	Entity <counter> (Architecture <=>) compiled.
Compiling vhdl file "CPU_BRANCH_CTRL/icla_add_n_bit.vhd" in Library work.	Compiling vhdl file "CPU_BRANCH_CTRL/muxento1_bus.vhd" in Library work.
Entity <icla_add_n_bit> compiled.	Entity <muxento1_bus> compiled.
Entity <icla_add_n_bit> (Architecture <ideal>) compiled.	Entity <muxento1_bus> (Architecture <=>) compiled.
Compiling vhdl file "CPU_BRANCH_CTRL/muxento1_bus.vhd" in Library work.	Compiling vhdl file "CPU_BRANCH_CTRL/icla_add_n_bit.vhd" in Library work.
Entity <muxento1_bus> compiled.	Entity <icla_add_n_bit> compiled.
Entity <muxento1_bus> (Architecture <ideal>) compiled.	Entity <icla_add_n_bit> (Architecture <=>) compiled.
Compiling vhdl file "CPU_BRANCH_CTRL/branch_ctrl.vhd" in Library work.	Compiling vhdl file "CPU_BRANCH_CTRL/branch_ctrl.vhd" in Library work.
Entity <branch_ctrl> compiled.	Entity <branch_ctrl> compiled.
Entity <branch_ctrl> (Architecture <ideal>) compiled.	Entity <branch_ctrl> (Architecture <=>) compiled.
Total REAL time to Xst completion: 0.00 secs	Total REAL time to Xst completion: 4.00 secs
Total CPU time to Xst completion: 0.40 secs	Total CPU time to Xst completion: 3.27 secs
->	->
Total memory usage is 4477172 kilobytes	Total memory usage is 4477120 kilobytes
Number of errors : 0 ( 0 filtered)	Number of errors : 0 ( 0 filtered)
Number of warnings : 1 ( 0 filtered)	Number of warnings : 1 ( 0 filtered)
Number of infos : 0 ( 0 filtered)	Number of infos : 0 ( 0 filtered)
*Use incremental -o branch_ctrl tb isim beh.exe -pri branch_ctrl tb.pri -top branch_ctrl tb	*Use incremental -o branch_ctrl tb isim beh.exe -pri branch_ctrl tb.pri -top branch_ctrl tb
(Sim P.20131013 (signature 0x7708090))	(Sim P.20131013 (signature 0x7708090))
Number of CPUs detected in this system: 8	Number of CPUs detected in this system: 8
Turning on multi-threading, number of parallel sub-compilation jobs: 16	Turning on multi-threading, number of parallel sub-compilation jobs: 16
Determining compilation order of HDL files	Determining compilation order of HDL files
Parsing VHDL file "muxento1.vhd" into library work	Parsing VHDL file "muxento1.vhd" into library work
Parsing VHDL file "gff.vhd" into library work	Parsing VHDL file "gff.vhd" into library work
Parsing VHDL file "req_file_functions.vhd" into library work	Parsing VHDL file "req_file_functions.vhd" into library work
Parsing VHDL file "muxdff.vhd" into library work	Parsing VHDL file "muxdff.vhd" into library work
Parsing VHDL file "icla_gp.vhd" into library work	Parsing VHDL file "icla_gp.vhd" into library work
Parsing VHDL file "muxento1_bus.vhd" into library work	Parsing VHDL file "muxento1_bus.vhd" into library work
Parsing VHDL file "counter.vhd" into library work	Parsing VHDL file "counter.vhd" into library work
Parsing VHDL file "icla_add_n_bit.vhd" into library work	Parsing VHDL file "icla_add_n_bit.vhd" into library work
Parsing VHDL file "branch_ctrl_functions.vhd" into library work	Parsing VHDL file "branch_ctrl_functions.vhd" into library work
Parsing VHDL file "branch_ctrl.vhd" into library work	Parsing VHDL file "branch_ctrl.vhd" into library work
Parsing VHDL file "branch_ctrl_tb.vhd" into library work	Parsing VHDL file "branch_ctrl_tb.vhd" into library work
Starting static elaboration	Starting static elaboration
Completed static elaboration	Completed static elaboration
Compiling package standard	Compiling package standard

>set -fh branch_cdf.xst	>set -fh branch_cdf.xst
Release 14.7 - xst P 20131013 (n64)	Release 14.7 - xst P 20131013 (n64)
Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.	Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.
-> Parameter TMPDIR set to /xstprojav/tmp	-> Parameter TMPDIR set to /xstprojav/tmp
Total REAL time to Xst completion: 0.00 secs	Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.23 secs	Total CPU time to Xst completion: 0.24 secs
-> WARNING:Xst:3164 - Option "-debug" found multiple times in the command line. Only the first occurrence is considered.	-> WARNING:Xst:3164 - Option "-debug" found multiple times in the command line. Only the first occurrence is considered.
* HDL Compilation *	* HDL Compilation *
Compiling vhdl file "CPU_BRANCH_CTRL/muxmto1.vhd" in Library work.	Compiling vhdl file "CPU_BRANCH_CTRL/muxmto1.vhd" in Library work.
Entity <muxmto1> compiled.	Entity <muxmto1> compiled.
Entity <muxmto1? (Architecture <idea>)> compiled.	Entity <muxmto1? (Architecture <=>)> compiled.
Compiling vhdl file "CPU_BRANCH_CTRL/iddf.vhd" in Library work.	Compiling vhdl file "CPU_BRANCH_CTRL/iddf.vhd" in Library work.
Entity <iddf> compiled.	Entity <iddf> compiled.
Entity <iddf? (Architecture <idea>)> compiled.	Entity <iddf? (Architecture <=>)> compiled.
Compiling vhdl file "CPU_BRANCH_CTRL/ireq_file_functions.vhd" in Library work.	Compiling vhdl file "CPU_BRANCH_CTRL/ireq_file_functions.vhd" in Library work.
Package <ireq_file_functions> compiled.	Entity <ireq_file_functions> compiled.
Package body <ireq_file_functions> compiled.	Entity <ireq_file_functions> compiled.
Compiling vhdl file "CPU_BRANCH_CTRL/icla_gp.vhd" in Library work.	Compiling vhdl file "CPU_BRANCH_CTRL/ireq_file_functions.vhd" in Library work.
Entity <icla_gp> compiled.	Package <ireq_file_functions> compiled.
Entity <icla_gp? (Architecture <idea>)> compiled.	Package body <ireq_file_functions> compiled.
Compiling vhdl file "CPU_BRANCH_CTRL/muxdff.vhd" in Library work.	Compiling vhdl file "CPU_BRANCH_CTRL/muxdff.vhd" in Library work.
Entity <muxdff> compiled.	Entity <muxdff> compiled.
Entity <muxdff? (Architecture <idea>)> compiled.	Entity <muxdff? (Architecture <=>)> compiled.
Compiling vhdl file "CPU_BRANCH_CTRL/branch_ctrl_functions.vhd" in Library work.	Compiling vhdl file "CPU_BRANCH_CTRL/branch_ctrl_functions.vhd" in Library work.
Package <branch_ctrl_functions> compiled.	Package <branch_ctrl_functions> compiled.
Package body <branch_ctrl_functions> compiled.	Package body <branch_ctrl_functions> compiled.
Compiling vhdl file "CPU_BRANCH_CTRL/counter.vhd" in Library work.	Compiling vhdl file "CPU_BRANCH_CTRL/counter.vhd" in Library work.
Entity <counter> compiled.	Entity <counter> compiled.
Entity <counter? (Architecture <idea>)> compiled.	Entity <counter? (Architecture <=>)> compiled.
Compiling vhdl file "CPU_BRANCH_CTRL/icla_add_n_bit.vhd" in Library work.	Compiling vhdl file "CPU_BRANCH_CTRL/muxmto1_bus.vhd" in Library work.
Entity <icla_add_n_bit> compiled.	Entity <muxmto1_bus> compiled.
Entity <icla_add_n_bit? (Architecture <idea>)> compiled.	Entity <muxmto1? bus> (Architecture <=>)> compiled.
Compiling vhdl file "CPU_BRANCH_CTRL/muxmto1_bus.vhd" in Library work.	Compiling vhdl file "CPU_BRANCH_CTRL/icla_add_n_bit.vhd" in Library work.
Entity <muxmto1? bus> (Architecture <idea>)> compiled.	Entity <icla_add_n_bit> compiled.
Compiling vhdl file "CPU_BRANCH_CTRL/branch_ctrl.vhd" in Library work.	Entity <icla_add_n_bit? (Architecture <=>)> compiled.
Entity <branch_ctrl> compiled.	Compiling vhdl file "CPU_BRANCH_CTRL/branch_ctrl.vhd" in Library work.
Entity <branch_ctrl? (Architecture <idea>)> compiled.	Entity <branch_ctrl> compiled.
Total REAL time to Xst completion: 2.00 secs	Entity <branch_ctrl? (Architecture <=>)> compiled.
Total CPU time to Xst completion: 2.29 secs	Total REAL time to Xst completion: 4.00 secs
->	Total CPU time to Xst completion: 3.27 secs
->	->
Total memory usage is 4477124 kilobytes	Total memory usage is 4477120 kilobytes
Number of errors : 0 ( 0 filtered)	Number of errors : 0 ( 0 filtered)
Number of warnings : 1 ( 0 filtered)	Number of warnings : 1 ( 0 filtered)
Number of infos : 0 ( 0 filtered)	Number of infos : 0 ( 0 filtered)
->Use incremental -o branch_cdf.tb aim beh exe -pri branch_cdf.tb pri -top branch_cdf.tb	->Use incremental -o branch_cdf.tb aim beh exe -pri branch_cdf.tb pri -top branch_cdf.tb
(Sim P 20131013 signature 0x7708090)	(Sim P 20131013 signature 0x7708090)
Number of CPUs detected in this system: 8	Number of CPUs detected in this system: 8
Turning on multi-threading: number of parallel sub-compilation jobs: 16	Turning on multi-threading: number of parallel sub-compilation jobs: 16
Determining compilation order of HDL files	Determining compilation order of HDL files
Parsing VHDL file "muxmto1.vhd" into library work	Parsing VHDL file "muxmto1.vhd" into library work
Parsing VHDL file "iddf.vhd" into library work	Parsing VHDL file "iddf.vhd" into library work
Parsing VHDL file "ireq_file_functions.vhd" into library work	Parsing VHDL file "ireq_file_functions.vhd" into library work
Parsing VHDL file "muxdff.vhd" into library work	Parsing VHDL file "muxdff.vhd" into library work
Parsing VHDL file "icla_gp.vhd" into library work	Parsing VHDL file "icla_gp.vhd" into library work
Parsing VHDL file "muxmto1_bus.vhd" into library work	Parsing VHDL file "muxmto1_bus.vhd" into library work
Parsing VHDL file "counter.vhd" into library work	Parsing VHDL file "counter.vhd" into library work
Parsing VHDL file "icla_add_n_bit.vhd" into library work	Parsing VHDL file "icla_add_n_bit.vhd" into library work
Parsing VHDL file "branch_ctrl_functions.vhd" into library work	Parsing VHDL file "branch_ctrl_functions.vhd" into library work
Parsing VHDL file "branch_ctrl.vhd" into library work	Parsing VHDL file "branch_ctrl.vhd" into library work
Parsing VHDL file "branch_ctrl_tb.vhd" into library work	Parsing VHDL file "branch_ctrl_tb.vhd" into library work
Starting static elaboration	Starting static elaboration
Completed static elaboration	Completed static elaboration
Compiling package standard	Compiling package standard

>set -fth branch_crtl.vst	>set -fth branch_crtl.vst
Release 14.7 - vst P 20131013 (n64)	Release 14.7 - vst P 20131013 (n64)
Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.	Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.
-> Parameter TMPDIR set to /xstprojav/tmp	-> Parameter TMPDIR set to /xstprojav/tmp
Total REAL time to Xst completion: 0.00 secs	Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.23 secs	Total CPU time to Xst completion: 0.24 secs
-> WARNING:Xst3164 - Option "-debug" found multiple times in the command line. Only the first occurrence is considered.	-> WARNING:Xst3164 - Option "-debug" found multiple times in the command line. Only the first occurrence is considered.
* HDL Compilation	* HDL Compilation
Compiling vhdl file "CPU_BRANCH_CTRL/muxent01.vhd" in Library work.	Compiling vhdl file "CPU_BRANCH_CTRL/muxent01.vhd" in Library work.
Entity <muxent01> compiled.	Entity <muxent01> compiled.
Entity <muxent01> (Architecture <idea0>) compiled.	Entity <muxent01> (Architecture <=>) compiled.
Compiling vhdl file "CPU_BRANCH_CTRL/iff.vhd" in Library work.	Compiling vhdl file "CPU_BRANCH_CTRL/iff.vhd" in Library work.
Entity <iff> compiled.	Entity <iff> compiled.
Entity <iff> (Architecture <idea0>) compiled.	Entity <iff> (Architecture <=>) compiled.
Compiling vhdl file "CPU_BRANCH_CTRL/cia_ap.vhd" in Library work.	Compiling vhdl file "CPU_BRANCH_CTRL/cia_ap.vhd" in Library work.
Entity <cia_ap> compiled.	Entity <cia_ap> compiled.
Entity <cia_ap> (Architecture <idea0>) compiled.	Entity <cia_ap> (Architecture <=>) compiled.
Compiling vhdl file "CPU_BRANCH_CTRL/muxdff.vhd" in Library work.	Compiling vhdl file "CPU_BRANCH_CTRL/reg_file_functions.vhd" in Library work.
Entity <muxdff> compiled.	Package <reg_file_functions> compiled.
Entity <muxdff> (Architecture <idea0>) compiled.	Package body <reg_file_functions> compiled.
Compiling vhdl file "CPU_BRANCH_CTRL/reg_file_functions.vhd" in Library work.	Compiling vhdl file "CPU_BRANCH_CTRL/muxdff.vhd" in Library work.
Package <reg_file_functions> compiled.	Entity <muxdff> compiled.
Package body <reg_file_functions> compiled.	Entity <muxdff> (Architecture <=>) compiled.
Compiling vhdl file "CPU_BRANCH_CTRL/muxent01_bus.vhd" in Library work.	Compiling vhdl file "CPU_BRANCH_CTRL/branch_crtl_functions.vhd" in Library work.
Entity <muxent01_bus> compiled.	Package <branch_crtl_functions> compiled.
Entity <muxent01_bus> (Architecture <idea0>) compiled.	Package body <branch_crtl_functions> compiled.
Compiling vhdl file "CPU_BRANCH_CTRL/counter.vhd" in Library work.	Compiling vhdl file "CPU_BRANCH_CTRL/counter.vhd" in Library work.
Entity <counter> compiled.	Entity <counter> compiled.
Entity <counter> (Architecture <idea0>) compiled.	Entity <counter> (Architecture <=>) compiled.
Compiling vhdl file "CPU_BRANCH_CTRL/cia_add_n_bit.vhd" in Library work.	Compiling vhdl file "CPU_BRANCH_CTRL/muxent01_bus.vhd" in Library work.
Entity <cia_add_n_bit> compiled.	Entity <muxent01_bus> compiled.
Entity <cia_add_n_bit> (Architecture <idea0>) compiled.	Entity <muxent01_bus> (Architecture <=>) compiled.
Compiling vhdl file "CPU_BRANCH_CTRL/branch_crtl.vhd" in Library work.	Compiling vhdl file "CPU_BRANCH_CTRL/cia_add_n_bit.vhd" in Library work.
ERROR:HDLParas:3310 - "CPU_BRANCH_CTRL/branch_crtl.vhd" Line 1. Entity branch_crtl does not exist.	Entity <cia_add_n_bit> compiled.
ERROR:HDLParas:3312 - "CPU_BRANCH_CTRL/branch_crtl.vhd" Line 2. Undefined symbol 'mux_vector_array_type'.	Compiling vhdl file "CPU_BRANCH_CTRL/branch_crtl.vhd" in Library work.
ERROR:HDLParas:1209 - "CPU_BRANCH_CTRL/branch_crtl.vhd" Line 2. mux_vector_array_type: Undefined symbol (last report in this block)	Entity <branch_crtl> compiled.
ERROR:HDLParas:842 - "CPU_BRANCH_CTRL/branch_crtl.vhd" Line 2. The type of the element in aggregate does not correspond to any array type.	Entity <branch_crtl> (Architecture <=>) compiled.
ERROR:HDLParas:3312 - "CPU_BRANCH_CTRL/branch_crtl.vhd" Line 3. Undefined symbol 'muxent01_bus_type'.	Total REAL time to Xst completion: 4.00 secs
ERROR:HDLParas:1209 - "CPU_BRANCH_CTRL/branch_crtl.vhd" Line 3. muxent01_bus_type: Undefined symbol (last report in this block)	Total CPU time to Xst completion: 3.27 secs
ERROR:HDLParas:3314 - "CPU_BRANCH_CTRL/branch_crtl.vhd" Line 3. Undefined symbol 'ctr_width'.	->
ERROR:HDLParas:1209 - "CPU_BRANCH_CTRL/branch_crtl.vhd" Line 3. ctr_width: Undefined symbol (last report in this block)	Total memory usage is 4477120 kilobytes
ERROR:HDLParas:842 - "CPU_BRANCH_CTRL/branch_crtl.vhd" Line 3. The type of the element in aggregate does not correspond to any array type.	Number of errors : 0 ( 0 filtered)
ERROR:HDLParas:3312 - "CPU_BRANCH_CTRL/branch_crtl.vhd" Line 4. Undefined symbol 'and_logic_vector'.	Number of warnings : 1 ( 0 filtered)
ERROR:HDLParas:1209 - "CPU_BRANCH_CTRL/branch_crtl.vhd" Line 4. and_logic_vector: Undefined symbol (last report in this block)	Number of infos : 0 ( 0 filtered)
ERROR:HDLParas:3312 - "CPU_BRANCH_CTRL/branch_crtl.vhd" Line 4. Undefined symbol 'and_logic'.	*Use incremental -o branch_crtl to aim beh.exe -pri branch_crtl to pri-top branch_crtl to
ERROR:HDLParas:1209 - "CPU_BRANCH_CTRL/branch_crtl.vhd" Line 4. and_logic: Undefined symbol (last report in this block)	Number of CPUs detected in this system: 8
ERROR:HDLParas:3312 - "CPU_BRANCH_CTRL/branch_crtl.vhd" Line 4. Undefined symbol 'mux_vector'.	Turning on multi-threading, number of parallel sub-compilation jobs: 16
ERROR:HDLParas:1209 - "CPU_BRANCH_CTRL/branch_crtl.vhd" Line 4. mux_vector: Undefined symbol (last report in this block)	Determining compilation order of HDL files
ERROR:HDLParas:3312 - "CPU_BRANCH_CTRL/branch_crtl.vhd" Line 4. Undefined symbol 'PC_load_addr'.	Parsing VHDL file "muxent01.vhd" into library work
ERROR:HDLParas:1209 - "CPU_BRANCH_CTRL/branch_crtl.vhd" Line 4. PC_load_addr: Undefined symbol (last report in this block)	Parsing VHDL file "iff.vhd" into library work
ERROR:HDLParas:3312 - "CPU_BRANCH_CTRL/branch_crtl.vhd" Line 4. Undefined symbol 'nBRANCH'.	Parsing VHDL file "reg_file_functions.vhd" into library work
ERROR:HDLParas:808 - "CPU_BRANCH_CTRL/branch_crtl.vhd" Line 17. Undefined symbol 'N'.	Parsing VHDL file "muxdff.vhd" into library work
ERROR:HDLParas:1209 - "CPU_BRANCH_CTRL/branch_crtl.vhd" Line 17. not can not have such operands in this context.	Parsing VHDL file "cia_ap.vhd" into library work
ERROR:HDLParas:3312 - "CPU_BRANCH_CTRL/branch_crtl.vhd" Line 17. Undefined symbol 'CE'.	Parsing VHDL file "muxent01_bus.vhd" into library work
ERROR:HDLParas:1209 - "CPU_BRANCH_CTRL/branch_crtl.vhd" Line 18. Undefined symbol 'counter'.	Parsing VHDL file "counter.vhd" into library work
ERROR:HDLParas:3312 - "CPU_BRANCH_CTRL/branch_crtl.vhd" Line 18. Undefined symbol 'counter'.	Parsing VHDL file "cia_add_n_bit.vhd" into library work
ERROR:HDLParas:1209 - "CPU_BRANCH_CTRL/branch_crtl.vhd" Line 18. Undefined symbol 'clk'.	Parsing VHDL file "branch_crtl_functions.vhd" into library work
ERROR:HDLParas:3312 - "CPU_BRANCH_CTRL/branch_crtl.vhd" Line 18. Undefined symbol 'nRST'.	Parsing VHDL file "branch_crtl.vhd" into library work
ERROR:HDLParas:1209 - "CPU_BRANCH_CTRL/branch_crtl.vhd" Line 23. Undefined symbol 'nRST'.	Parsing VHDL file "branch_crtl_tb.vhd" into library work
ERROR:HDLParas:3312 - "CPU_BRANCH_CTRL/branch_crtl.vhd" Line 23. Undefined symbol 'nRST'.	Starting static elaboration
ERROR:HDLParas:1209 - "CPU_BRANCH_CTRL/branch_crtl.vhd" Line 23. CE: Undefined symbol (last report in this block)	Completed static elaboration
ERROR:HDLParas:3312 - "CPU_BRANCH_CTRL/branch_crtl.vhd" Line 23. Undefined symbol 'PC_sig'.	Compiling package standard



>set -fh branch ctrl.vst	>set -fh branch ctrl.vst
Release 14.7 - xst P 20131013 (n64)	Release 14.7 - xst P 20131013 (n64)
Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.	Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.
-> Parameter TMPDIR set to /xstprocdir/tmp	-> Parameter TMPDIR set to /xstprocdir/tmp
Total REAL time to Xst completion: 1.00 secs	Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.24 secs	Total CPU time to Xst completion: 0.24 secs
-> WARNING:Xst:3164 - Option "-debug" found multiple times in the command line. Only the first occurrence is considered.	-> WARNING:Xst:3164 - Option "-debug" found multiple times in the command line. Only the first occurrence is considered.
* HDL Compilation *	* HDL Compilation *
Compiling vhdl file "CPU_BRANCH_CTRL/muxonto1.vhd" in Library work.	Compiling vhdl file "CPU_BRANCH_CTRL/muxonto1.vhd" in Library work.
Entity <muxonto1> compiled.	Entity <muxonto1> compiled.
Entity <muxonto1? (Architecture <idea0>) compiled.	Entity <muxonto1? (Architecture <=) compiled.
Compiling vhdl file "CPU_BRANCH_CTRL/idd.vhd" in Library work.	Compiling vhdl file "CPU_BRANCH_CTRL/idd.vhd" in Library work.
Entity <idd> compiled.	Entity <idd> compiled.
Entity <idd? (Architecture <idea0>) compiled.	Entity <idd? (Architecture <=) compiled.
Compiling vhdl file "CPU_BRANCH_CTRL/ireq file functions.vhd" in Library work.	Compiling vhdl file "CPU_BRANCH_CTRL/ireq file functions.vhd" in Library work.
Package <ireq file functions> compiled.	Entity <cla_0p> compiled.
Package body <ireq file functions> compiled.	Entity <cla_0p> (Architecture <=) compiled.
Compiling vhdl file "CPU_BRANCH_CTRL/icia_0p.vhd" in Library work.	Compiling vhdl file "CPU_BRANCH_CTRL/ireq file functions.vhd" in Library work.
Entity <cla_0p> compiled.	Package <ireq file functions> compiled.
Entity <cla_0p> (Architecture <idea0>) compiled.	Package body <ireq file functions> compiled.
Compiling vhdl file "CPU_BRANCH_CTRL/muxdff.vhd" in Library work.	Compiling vhdl file "CPU_BRANCH_CTRL/muxdff.vhd" in Library work.
Entity <muxdff> compiled.	Entity <muxdff> compiled.
Entity <muxdff? (Architecture <idea0>) compiled.	Entity <muxdff? (Architecture <=) compiled.
Compiling vhdl file "CPU_BRANCH_CTRL/branch_ctrl functions.vhd" in Library work.	Compiling vhdl file "CPU_BRANCH_CTRL/branch_ctrl functions.vhd" in Library work.
Package <branch ctrl functions> compiled.	Package <branch ctrl functions> compiled.
Package body <branch ctrl functions> compiled.	Package body <branch ctrl functions> compiled.
Compiling vhdl file "CPU_BRANCH_CTRL/counter.vhd" in Library work.	Compiling vhdl file "CPU_BRANCH_CTRL/counter.vhd" in Library work.
Entity <counter> compiled.	Entity <counter> compiled.
Entity <counter? (Architecture <idea0>) compiled.	Entity <counter? (Architecture <=) compiled.
Compiling vhdl file "CPU_BRANCH_CTRL/icia_add_n_bit.vhd" in Library work.	Compiling vhdl file "CPU_BRANCH_CTRL/muxonto1_bus.vhd" in Library work.
Entity <icia_add_n_bit> compiled.	Entity <muxonto1_bus> compiled.
Entity <icia_add_n_bit? (Architecture <idea0>) compiled.	Entity <muxonto1_bus? (Architecture <=) compiled.
Compiling vhdl file "CPU_BRANCH_CTRL/muxonto1_bus.vhd" in Library work.	Compiling vhdl file "CPU_BRANCH_CTRL/icia_add_n_bit.vhd" in Library work.
Entity <muxonto1_bus> compiled.	Entity <icia_add_n_bit> compiled.
Entity <muxonto1_bus? (Architecture <idea0>) compiled.	Entity <icia_add_n_bit? (Architecture <=) compiled.
Compiling vhdl file "CPU_BRANCH_CTRL/branch_ctrl.vhd" in Library work.	Compiling vhdl file "CPU_BRANCH_CTRL/branch_ctrl.vhd" in Library work.
Entity <branch_ctrl> compiled.	Entity <branch_ctrl> compiled.
Entity <branch_ctrl? (Architecture <idea0>) compiled.	Entity <branch_ctrl? (Architecture <=) compiled.
Total REAL time to Xst completion: 3.00 secs	Total REAL time to Xst completion: 4.00 secs
Total CPU time to Xst completion: 2.66 secs	Total CPU time to Xst completion: 3.27 secs
->	->
Total memory usage is 4477132 kilobytes	Total memory usage is 4477120 kilobytes
Number of errors : 0 ( 0 filtered)	Number of errors : 0 ( 0 filtered)
Number of warnings : 1 ( 0 filtered)	Number of warnings : 1 ( 0 filtered)
Number of infos : 0 ( 0 filtered)	Number of infos : 0 ( 0 filtered)
*Use incremental -o branch_ctrl.tb aim beh exe -pri branch_ctrl.tb pri-top branch_ctrl.tb	*Use incremental -o branch_ctrl.tb aim beh exe -pri branch_ctrl.tb pri-top branch_ctrl.tb
(Sim P 20131013 signature 0x7708090)	(Sim P 20131013 signature 0x7708090)
Number of CPUs detected in this system: 8	Number of CPUs detected in this system: 8
Turning on multi-threading: number of parallel sub-compilation jobs: 16	Turning on multi-threading: number of parallel sub-compilation jobs: 16
Determining compilation order of HDL files	Determining compilation order of HDL files
Parsing VHDL file "muxonto1.vhd" into library work	Parsing VHDL file "muxonto1.vhd" into library work
Parsing VHDL file "idd.vhd" into library work	Parsing VHDL file "idd.vhd" into library work
Parsing VHDL file "ireq file functions.vhd" into library work	Parsing VHDL file "ireq file functions.vhd" into library work
Parsing VHDL file "muxdff.vhd" into library work	Parsing VHDL file "muxdff.vhd" into library work
Parsing VHDL file "icia_0p.vhd" into library work	Parsing VHDL file "icia_0p.vhd" into library work
Parsing VHDL file "muxonto1_bus.vhd" into library work	Parsing VHDL file "muxonto1_bus.vhd" into library work
Parsing VHDL file "counter.vhd" into library work	Parsing VHDL file "counter.vhd" into library work
Parsing VHDL file "icia_add_n_bit.vhd" into library work	Parsing VHDL file "icia_add_n_bit.vhd" into library work
Parsing VHDL file "branch_ctrl functions.vhd" into library work	Parsing VHDL file "branch_ctrl functions.vhd" into library work
Parsing VHDL file "branch_ctrl.vhd" into library work	Parsing VHDL file "branch_ctrl.vhd" into library work
Parsing VHDL file "branch_ctrl.tb.vhd" into library work	Parsing VHDL file "branch_ctrl.tb.vhd" into library work
Starting static elaboration	Starting static elaboration
Completed static elaboration	Completed static elaboration
Compiling package standard	Compiling package standard

>xst -fhn branch_ctrl.xst	>xst -fhn branch_ctrl.xst
Release 14.7 - xst P.20131013 (n64)	Release 14.7 - xst P.20131013 (n64)
Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.	Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.
-> Parameter TMPDIR set to /xstprojdir/tmp	-> Parameter TMPDIR set to /xstprojdir/tmp
Total REAL time to Xst completion: 0.00 secs	Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.28 secs	Total CPU time to Xst completion: 0.24 secs
-> WARNING:Xst:3164 - Option "-debug" found multiple times in the command line. Only the first occurrence is considered.	-> WARNING:Xst:3164 - Option "-debug" found multiple times in the command line. Only the first occurrence is considered.
HDL Compiler	HDL Compiler
Compiling vhdl file "CPU_BRANCH_CTRL/muxento1.vhd" in Library work.	Compiling vhdl file "CPU_BRANCH_CTRL/muxento1.vhd" in Library work.
Entity <muxento1> compiled.	Entity <muxento1> compiled.
Entity <muxento1> (Architecture <ideal>) compiled.	Entity <muxento1> (Architecture <=>) compiled.
Compiling vhdl file "CPU_BRANCH_CTRL/gff.vhd" in Library work.	Compiling vhdl file "CPU_BRANCH_CTRL/gff.vhd" in Library work.
Entity <gff> compiled.	Entity <gff> compiled.
Entity <gff> (Architecture <ideal>) compiled.	Entity <gff> (Architecture <=>) compiled.
Compiling vhdl file "CPU_BRANCH_CTRL/req_file_functions.vhd" in Library work.	Compiling vhdl file "CPU_BRANCH_CTRL/icla_gp.vhd" in Library work.
Package <req_file_functions> compiled.	Entity <icla_gp> compiled.
Package body <req_file_functions> compiled.	Entity <icla_gp> (Architecture <=>) compiled.
Compiling vhdl file "CPU_BRANCH_CTRL/icla_gp.vhd" in Library work.	Compiling vhdl file "CPU_BRANCH_CTRL/req_file_functions.vhd" in Library work.
Entity <icla_gp> compiled.	Package <req_file_functions> compiled.
Entity <icla_gp> (Architecture <ideal>) compiled.	Package body <req_file_functions> compiled.
Compiling vhdl file "CPU_BRANCH_CTRL/muxdff.vhd" in Library work.	Compiling vhdl file "CPU_BRANCH_CTRL/muxdff.vhd" in Library work.
Entity <muxdff> compiled.	Entity <muxdff> compiled.
Entity <muxdff> (Architecture <ideal>) compiled.	Entity <muxdff> (Architecture <=>) compiled.
Compiling vhdl file "CPU_BRANCH_CTRL/branch_ctrl_functions.vhd" in Library work.	Compiling vhdl file "CPU_BRANCH_CTRL/branch_ctrl_functions.vhd" in Library work.
Package <branch_ctrl_functions> compiled.	Package <branch_ctrl_functions> compiled.
Package body <branch_ctrl_functions> compiled.	Package body <branch_ctrl_functions> compiled.
Compiling vhdl file "CPU_BRANCH_CTRL/counter.vhd" in Library work.	Compiling vhdl file "CPU_BRANCH_CTRL/counter.vhd" in Library work.
Entity <counter> compiled.	Entity <counter> compiled.
Entity <counter> (Architecture <ideal>) compiled.	Entity <counter> (Architecture <=>) compiled.
Compiling vhdl file "CPU_BRANCH_CTRL/icla_add_n_bit.vhd" in Library work.	Compiling vhdl file "CPU_BRANCH_CTRL/muxento1_bus.vhd" in Library work.
Entity <icla_add_n_bit> compiled.	Entity <muxento1_bus> compiled.
Entity <icla_add_n_bit> (Architecture <ideal>) compiled.	Entity <muxento1_bus> (Architecture <=>) compiled.
Compiling vhdl file "CPU_BRANCH_CTRL/muxento1_bus.vhd" in Library work.	Compiling vhdl file "CPU_BRANCH_CTRL/icla_add_n_bit.vhd" in Library work.
Entity <muxento1_bus> compiled.	Entity <icla_add_n_bit> compiled.
Entity <muxento1_bus> (Architecture <ideal>) compiled.	Entity <icla_add_n_bit> (Architecture <=>) compiled.
Compiling vhdl file "CPU_BRANCH_CTRL/branch_ctrl.vhd" in Library work.	Compiling vhdl file "CPU_BRANCH_CTRL/branch_ctrl.vhd" in Library work.
Entity <branch_ctrl> compiled.	Entity <branch_ctrl> compiled.
Entity <branch_ctrl> (Architecture <ideal>) compiled.	Entity <branch_ctrl> (Architecture <=>) compiled.
Total REAL time to Xst completion: 0.60 secs	Total REAL time to Xst completion: 4.00 secs
Total CPU time to Xst completion: 0.46 secs	Total CPU time to Xst completion: 3.27 secs
->	->
Total memory usage is 4477128 kilobytes	Total memory usage is 4477120 kilobytes
Number of errors : 0 ( 0 filtered)	Number of errors : 0 ( 0 filtered)
Number of warnings : 1 ( 0 filtered)	Number of warnings : 1 ( 0 filtered)
Number of infos : 0 ( 0 filtered)	Number of infos : 0 ( 0 filtered)
*Use incremental -o branch_ctrl_tb isim beh.exe -pri branch_ctrl_tb.pri -top branch_ctrl_tb	*Use incremental -o branch_ctrl_tb isim beh.exe -pri branch_ctrl_tb.pri -top branch_ctrl_tb
(Sim P.20131013 (signature 0x7708090))	(Sim P.20131013 (signature 0x7708090))
Number of CPUs detected in this system: 8	Number of CPUs detected in this system: 8
Turning on multi-threading, number of parallel sub-compilation jobs: 16	Turning on multi-threading, number of parallel sub-compilation jobs: 16
Determining compilation order of HDL files	Determining compilation order of HDL files
Parsing VHDL file "muxento1.vhd" into library work	Parsing VHDL file "muxento1.vhd" into library work
Parsing VHDL file "gff.vhd" into library work	Parsing VHDL file "gff.vhd" into library work
Parsing VHDL file "req_file_functions.vhd" into library work	Parsing VHDL file "req_file_functions.vhd" into library work
Parsing VHDL file "muxdff.vhd" into library work	Parsing VHDL file "muxdff.vhd" into library work
Parsing VHDL file "icla_gp.vhd" into library work	Parsing VHDL file "icla_gp.vhd" into library work
Parsing VHDL file "muxento1_bus.vhd" into library work	Parsing VHDL file "muxento1_bus.vhd" into library work
Parsing VHDL file "counter.vhd" into library work	Parsing VHDL file "counter.vhd" into library work
Parsing VHDL file "icla_add_n_bit.vhd" into library work	Parsing VHDL file "icla_add_n_bit.vhd" into library work
Parsing VHDL file "branch_ctrl_functions.vhd" into library work	Parsing VHDL file "branch_ctrl_functions.vhd" into library work
Parsing VHDL file "branch_ctrl.vhd" into library work	Parsing VHDL file "branch_ctrl.vhd" into library work
Parsing VHDL file "branch_ctrl_tb.vhd" into library work	Parsing VHDL file "branch_ctrl_tb.vhd" into library work
Starting static elaboration	Starting static elaboration
Completed static elaboration	Completed static elaboration
Compiling package standard	Compiling package standard

```

>xst -ifn branch_ctrl.xst
Release 14.7 - xst P.20131013 (nt64)
Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.
--> Parameter TMPDIR set to ./xst/projnav.tmp
Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.24 secs

--> WARNING:Xst:3164 - Option "-debug" found multiple times in the command line. Only the first occurrence
*          HDL Compilation          *
Compiling vhdl file "CPU_BRANCH_CTRL//muxnto1.vhd" in Library work.
Entity <muxnto1> compiled.
Entity <muxnto1> (Architecture <>) compiled.
Compiling vhdl file "CPU_BRANCH_CTRL//dff.vhd" in Library work.
Entity <dff> compiled.
Entity <dff> (Architecture <>) compiled.
Compiling vhdl file "CPU_BRANCH_CTRL//cla_gp.vhd" in Library work.
Entity <cla_gp> compiled.
Entity <cla_gp> (Architecture <>) compiled.
Compiling vhdl file "CPU_BRANCH_CTRL//reg_file_functions.vhd" in Library work.
Package <reg_file_functions> compiled.
Package body <reg_file_functions> compiled.
Compiling vhdl file "CPU_BRANCH_CTRL//muxdff.vhd" in Library work.
Entity <muxdff> compiled.
Entity <muxdff> (Architecture <>) compiled.
Compiling vhdl file "CPU_BRANCH_CTRL//branch_ctrl_functions.vhd" in Library work.
Package <branch_ctrl_functions> compiled.
Package body <branch_ctrl_functions> compiled.
Compiling vhdl file "CPU_BRANCH_CTRL//counter.vhd" in Library work.
Entity <counter> compiled.
Entity <counter> (Architecture <>) compiled.
Compiling vhdl file "CPU_BRANCH_CTRL//muxnto1_bus.vhd" in Library work.
Entity <muxnto1_bus> compiled.
Entity <muxnto1_bus> (Architecture <>) compiled.
Compiling vhdl file "CPU_BRANCH_CTRL//cla_add_n_bit.vhd" in Library work.
Entity <cla_add_n_bit> compiled.
Entity <cla_add_n_bit> (Architecture <>) compiled.
Compiling vhdl file "CPU_BRANCH_CTRL//branch_ctrl.vhd" in Library work.
Entity <branch_ctrl> compiled.
Entity <branch_ctrl> (Architecture <>) compiled.
Total REAL time to Xst completion: 4.00 secs
Total CPU time to Xst completion: 3.27 secs

-->
Total memory usage is 4477120 kilobytes
Number of errors   : 0 ( 0 filtered)
Number of warnings : 1 ( 0 filtered)
Number of infos    : 0 ( 0 filtered)
>fuse -incremental -o branch_ctrl_tb_isim_beh.exe -prj branch_ctrl_tb.prj -top branch_ctrl_tb
ISim P.20131013 (signature 0x7708f090)
Number of CPUs detected in this system: 8
Turning on mult-threading, number of parallel sub-compilation jobs: 16
Determining compilation order of HDL files
Parsing VHDL file "muxnto1.vhd" into library work
Parsing VHDL file "dff.vhd" into library work
Parsing VHDL file "reg_file_functions.vhd" into library work
Parsing VHDL file "muxdff.vhd" into library work
Parsing VHDL file "cla_gp.vhd" into library work
Parsing VHDL file "muxnto1_bus.vhd" into library work

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Parsing VHDL file "counter.vhd" into library work
Parsing VHDL file "cla_add_n_bit.vhd" into library work
Parsing VHDL file "branch_ctrl_functions.vhd" into library work
Parsing VHDL file "branch_ctrl.vhd" into library work
Parsing VHDL file "branch_ctrl_tb.vhd" into library work
Starting static elaboration
Completed static elaboration
Compiling package standard
Compiling package std_logic_1164
Compiling package math_real
Compiling package reg_file_functions
Compiling package branch_ctrl_functions
Compiling package textio
Compiling package std_logic_textio
Compiling package numeric_std
Compiling architecture of entity muxnto1 [\muxnto1(1)\]
Compiling architecture of entity dff [dff_default]
Compiling architecture of entity muxdff [\muxdff(1)\]
Compiling architecture of entity counter [\counter(16)\]
Compiling architecture of entity muxnto1_bus [\muxnto1_bus(1,16)\]
Compiling architecture of entity cla_gp [cla_gp_default]
Compiling architecture of entity cla_add_n_bit [\cla_add_n_bit(16)\]
Compiling architecture of entity branch_ctrl [\branch_ctrl(16)\]
Compiling architecture ndv of entity branch_ctrl_tb
Time Resolution for simulation is 1ps.
Waiting for 1 sub-compilation(s) to finish...
Compiled 25 VHDL Units
Built simulation executable branch_ctrl_tb_isim_beh.exe
Fuse Memory Usage: 38108 KB
Fuse CPU Usage: 1155 ms
>branch_ctrl_tb_isim_beh.exe -tclbatch isim.tcl -wdb branch_ctrl_tb_isim_beh.wdb
ISim P.20131013 (signature 0x7708f090)
WARNING: A WEBPACK license was found.
WARNING: Please use Xilinx License Configuration Manager to check out a full ISim license.
WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for more information on t
This is a Lite version of ISim.
Time resolution is 1 ps
Simulator is doing circuit initialization process.
at 0 ps, Instance /branch_ctrl_tb/UUT/BRANCH_MUX\muxloop(0)\Ui/ : Warning: NUMERIC_STD.TO_
at 0 ps, Instance /branch_ctrl_tb/UUT/BRANCH_MUX\muxloop(1)\Ui/ : Warning: NUMERIC_STD.TO_
at 0 ps, Instance /branch_ctrl_tb/UUT/BRANCH_MUX\muxloop(2)\Ui/ : Warning: NUMERIC_STD.TO_
at 0 ps, Instance /branch_ctrl_tb/UUT/BRANCH_MUX\muxloop(3)\Ui/ : Warning: NUMERIC_STD.TO_
at 0 ps, Instance /branch_ctrl_tb/UUT/BRANCH_MUX\muxloop(4)\Ui/ : Warning: NUMERIC_STD.TO_
at 0 ps, Instance /branch_ctrl_tb/UUT/BRANCH_MUX\muxloop(5)\Ui/ : Warning: NUMERIC_STD.TO_
at 0 ps, Instance /branch_ctrl_tb/UUT/BRANCH_MUX\muxloop(6)\Ui/ : Warning: NUMERIC_STD.TO_
at 0 ps, Instance /branch_ctrl_tb/UUT/BRANCH_MUX\muxloop(7)\Ui/ : Warning: NUMERIC_STD.TO_
at 0 ps, Instance /branch_ctrl_tb/UUT/BRANCH_MUX\muxloop(8)\Ui/ : Warning: NUMERIC_STD.TO_
at 0 ps, Instance /branch_ctrl_tb/UUT/BRANCH_MUX\muxloop(9)\Ui/ : Warning: NUMERIC_STD.TO_
at 0 ps, Instance /branch_ctrl_tb/UUT/BRANCH_MUX\muxloop(10)\Ui/ : Warning: NUMERIC_STD.TC
at 0 ps, Instance /branch_ctrl_tb/UUT/BRANCH_MUX\muxloop(11)\Ui/ : Warning: NUMERIC_STD.TC
at 0 ps, Instance /branch_ctrl_tb/UUT/BRANCH_MUX\muxloop(12)\Ui/ : Warning: NUMERIC_STD.TC
at 0 ps, Instance /branch_ctrl_tb/UUT/BRANCH_MUX\muxloop(13)\Ui/ : Warning: NUMERIC_STD.TC
at 0 ps, Instance /branch_ctrl_tb/UUT/BRANCH_MUX\muxloop(14)\Ui/ : Warning: NUMERIC_STD.TC
at 0 ps, Instance /branch_ctrl_tb/UUT/BRANCH_MUX\muxloop(15)\Ui/ : Warning: NUMERIC_STD.TC
Finished circuit initialization process.
at 0 ps, Instance /branch_ctrl_tb/UUT/PC_ctr\I1(0)\Ui/U0/ : Warning: NUMERIC_STD.TO_INTEGER: i
at 0 ps, Instance /branch_ctrl_tb/UUT/PC_ctr\I1(1)\Ui/U0/ : Warning: NUMERIC_STD.TO_INTEGER: i
at 0 ps, Instance /branch_ctrl_tb/UUT/PC_ctr\I1(2)\Ui/U0/ : Warning: NUMERIC_STD.TO_INTEGER: i
at 0 ps, Instance /branch_ctrl_tb/UUT/PC_ctr\I1(3)\Ui/U0/ : Warning: NUMERIC_STD.TO_INTEGER: i

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at 0 ps, Instance /branch\_ctrl\_tb/UUT/PC\_ctr/I1(4)\Ui/U0/ : Warning: NUMERIC\_STD.TO\_INTEGER: I  
at 0 ps, Instance /branch\_ctrl\_tb/UUT/PC\_ctr/I1(5)\Ui/U0/ : Warning: NUMERIC\_STD.TO\_INTEGER: I  
at 0 ps, Instance /branch\_ctrl\_tb/UUT/PC\_ctr/I1(6)\Ui/U0/ : Warning: NUMERIC\_STD.TO\_INTEGER: I  
at 0 ps, Instance /branch\_ctrl\_tb/UUT/PC\_ctr/I1(7)\Ui/U0/ : Warning: NUMERIC\_STD.TO\_INTEGER: I  
at 0 ps, Instance /branch\_ctrl\_tb/UUT/PC\_ctr/I1(8)\Ui/U0/ : Warning: NUMERIC\_STD.TO\_INTEGER: I  
at 0 ps, Instance /branch\_ctrl\_tb/UUT/PC\_ctr/I1(9)\Ui/U0/ : Warning: NUMERIC\_STD.TO\_INTEGER: I  
at 0 ps, Instance /branch\_ctrl\_tb/UUT/PC\_ctr/I1(10)\Ui/U0/ : Warning: NUMERIC\_STD.TO\_INTEGER: I  
at 0 ps, Instance /branch\_ctrl\_tb/UUT/PC\_ctr/I1(11)\Ui/U0/ : Warning: NUMERIC\_STD.TO\_INTEGER: I  
at 0 ps, Instance /branch\_ctrl\_tb/UUT/PC\_ctr/I1(12)\Ui/U0/ : Warning: NUMERIC\_STD.TO\_INTEGER: I  
at 0 ps, Instance /branch\_ctrl\_tb/UUT/PC\_ctr/I1(13)\Ui/U0/ : Warning: NUMERIC\_STD.TO\_INTEGER: I  
at 0 ps, Instance /branch\_ctrl\_tb/UUT/PC\_ctr/I1(14)\Ui/U0/ : Warning: NUMERIC\_STD.TO\_INTEGER: I  
at 0 ps, Instance /branch\_ctrl\_tb/UUT/PC\_ctr/I1(15)\Ui/U0/ : Warning: NUMERIC\_STD.TO\_INTEGER: I

rence is considered.

the differences between the Lite and the Full version.

\_INTEGER: metavalue detected, returning 0  
\_INTEGER: metavalue detected, returning 0  
\_INTEGER: metavalue detected, returning 0  
\_INTEGER: metavalue detected, returning 0  
\_INTEGER: metavalue detected, returning 0  
\_INTEGER: metavalue detected, returning 0  
\_INTEGER: metavalue detected, returning 0  
\_INTEGER: metavalue detected, returning 0  
\_INTEGER: metavalue detected, returning 0  
)\_INTEGER: metavalue detected, returning 0  
)\_INTEGER: metavalue detected, returning 0  
)\_INTEGER: metavalue detected, returning 0  
)\_INTEGER: metavalue detected, returning 0  
)\_INTEGER: metavalue detected, returning 0  
)\_INTEGER: metavalue detected, returning 0

metavalue detected, returning 0  
metavalue detected, returning 0  
metavalue detected, returning 0  
metavalue detected, returning 0

[illegible]