

clk	ctrl	word	RW	DA	AA	BA	MB	MD	ALU_mode	ALU_function	N	C	V	Z	Const_in	Data_in	Address_out	Data_out	Comment				
1		0	U		0	0	0	U	U		0	0	0	0	1	11	0	0	RESET				
1		27	1	0	0	0	0	1		6	0	0	0	0	1	11	11	11	LOAD R(0) <= MEM(R(0))				
1		-32677	1	4	0	0	1	1		6	0	0	0	0	1	22	11	1	LOAD R(4) <= MEM(R(0))				
1		-24063	1	5	0	4	0	0		0	0	0	0	0	1	22	11	22	ADD R(5) <= R(0) + R(4)				
1		-12223	1	6	4	0	1	0		0	0	0	0	0	27	22	22	27	ADI R(6) <= R(4) + Const_in				
1		-4039	1	7	4	0	0	0		14	0	0	0	0	27	22	22	11	MOVE A R(7) <= R(4)				
1		25533	1	3	0	7	0	0		15	0	0	0	0	27	22	11	22	MOVE B R(3) <= R(7)				
1		3992	0	0	3	7	0	0		6	0	0	0	0	27	22	22	22	STORE B MEM(R(3)) <= R(7)				
1		4056	0	0	3	7	1	0		6	0	0	0	0	95	22	22	95	STORE CONST MEM(R(3)) <= Const_in				
1		1088	0	0	1	0	1	0		0	0	0	0	1	0	22	0	0	TEST R(1) using bus A: set NCVZ bits using ADD immediate Y=A + 0 alu command				
1		-11727	1	6	4	4	0	0		12	0	0	0	0	0	22	22	22	R(6) <= R(4) xor R(4)				
1		-15112	0	6	1	1	1	0		14	0	0	0	1	0	22	0	0	TEST R(1) using bus A: set NCVZ bits using Y=X alu command				
1		-51	1	7	7	7	1	0		3	0	1	0	0	95	22	21	95	R(7) <= R(7) - 1				
1		-9271	1	6	6	7	1	0		2	0	0	0	0	95	22	1	95	R(6) <= R(6) + 1				
1		-40	0	7	7	7	1	0		6	0	0	0	0	95	22	21	95	SET ALU NOP	DA=R(7)	AA=R(7)	BA=R(7)	NO WRITE

clk	ctrl	word	RW	DA	AA	BA	MB	MD	ALU_mode	ALU_function	N	C	V	Z	Const_in	Data_in	Address_out	Data_out	Comment				
1		0	U		0	0	0	U	U		0	0	0	0	1	11	0	0	RESET				
1		27	1	0	0	0	0	1		6	0	0	0	0	1	11	11	11	LOAD R(0) <= MEM(R(0))				
1		-32677	1	4	0	0	1	1		6	0	0	0	0	1	22	11	1	LOAD R(4) <= MEM(R(0))				
1		-24063	1	5	0	4	0	0		0	0	0	0	0	1	22	11	22	ADD R(5) <= R(0) + R(4)				
1		-12223	1	6	4	0	1	0		0	0	0	0	0	27	22	22	27	ADI R(6) <= R(4) + Const_in				
1		-4039	1	7	4	0	0	0		14	0	0	0	0	27	22	22	11	MOVE A R(7) <= R(4)				
1		25533	1	3	0	7	0	0		15	0	0	0	0	27	22	11	22	MOVE B R(3) <= R(7)				
1		3992	0	0	3	7	0	0		6	0	0	0	0	27	22	22	22	STORE B MEM(R(3)) <= R(7)				
1		4056	0	0	3	7	1	0		6	0	0	0	0	95	22	22	95	STORE CONST MEM(R(3)) <= Const_in				
1		1088	0	0	1	0	1	0		0	0	0	0	1	0	22	0	0	TEST R(1) using bus A: set NCVZ bits using ADD immediate Y=A + 0 alu command				
1		-11727	1	6	4	4	0	0		12	0	0	0	0	0	22	22	22	R(6) <= R(4) xor R(4)				
1		-15112	0	6	1	1	1	0		14	0	0	0	1	0	22	0	0	TEST R(1) using bus A: set NCVZ bits using Y=X alu command				
1		-51	1	7	7	7	1	0		3	0	1	0	0	95	22	21	95	R(7) <= R(7) - 1				
1		-9271	1	6	6	7	1	0		2	0	0	0	0	95	22	1	95	R(6) <= R(6) + 1				
1		-40	0	7	7	7	1	0		6	0	0	0	0	95	22	21	95	SET ALU NOP	DA=R(7)	AA=R(7)	BA=R(7)	NO WRITE

clk	ctrl	word	RW	DA	AA	BA	MB	MD	ALU_mode	ALU_function	N	C	V	Z	Const_in	Data_in	Address_out	Data_out	Comment				
1		0	U		0	0	0	U	U		0	0	0	0	1	11	0	0	RESET				
1		27	1	0	0	0	0	1		6	0	0	0	0	1	11	11	11	LOAD R(0) <= MEM(R(0))				
1		-32677	1	4	0	0	1	1		6	0	0	0	0	1	22	11	1	LOAD R(4) <= MEM(R(0))				
1		-24063	1	5	0	4	0	0		0	0	0	0	0	1	22	11	22	ADD R(5) <= R(0) + R(4)				
1		-12223	1	6	4	0	1	0		0	0	0	0	0	27	22	22	27	ADI R(6) <= R(4) + Const_in				
1		-4039	1	7	4	0	0	0		14	0	0	0	0	27	22	22	11	MOVE A R(7) <= R(4)				
1		25533	1	3	0	7	0	0		15	0	0	0	0	27	22	11	22	MOVE B R(3) <= R(7)				
1		3992	0	0	3	7	0	0		6	0	0	0	0	27	22	22	22	STORE B MEM(R(3)) <= R(7)				
1		4056	0	0	3	7	1	0		6	0	0	0	0	95	22	22	95	STORE CONST MEM(R(3)) <= Const_in				
1		1088	0	0	1	0	1	0		0	0	0	0	1	0	22	0	0	TEST R(1) using bus A: set NCVZ bits using ADD immediate Y=A + 0 alu command				
1		-11727	1	6	4	4	0	0		12	0	0	0	0	0	22	22	22	R(6) <= R(4) xor R(4)				
1		-15112	0	6	1	1	1	0		14	0	0	0	1	0	22	0	0	TEST R(1) using bus A: set NCVZ bits using Y=X alu command				
1		-51	1	7	7	7	1	0		3	0	1	0	0	95	22	21	95	R(7) <= R(7) - 1				
1		-9271	1	6	6	7	1	0		2	0	0	0	0	95	22	1	95	R(6) <= R(6) + 1				
1		-40	0	7	7	7	1	0		6	0	0	0	0	95	22	21	95	SET ALU NOP	DA=R(7)	AA=R(7)	BA=R(7)	NO WRITE

clk	ctrl	word	RW	DA	AA	BA	MB	MD	ALU_mode	ALU_function	N	C	V	Z	Const_in	Data_in	Address_out	Data_out	Comment				
1		0	U	0	0	0	U	U		0	0	0	0	0	1	11	0	0	RESET				
1		27	1	0	0	0	0	1		6	0	0	0	0	1	11	11	11	LOAD R(0) <= MEM(R(0))				
1		-32677	1	4	0	0	1	1		6	0	0	0	0	1	22	11	1	LOAD R(4) <= MEM(R(0))				
1		-24063	1	5	0	4	0	0		0	0	0	0	0	1	22	11	22	ADD R(5) <= R(0) + R(4)				
1		-12223	1	6	4	0	1	0		0	0	0	0	0	27	22	22	27	ADI R(6) <= R(4) + Const_in				
1		-4039	1	7	4	0	0	0		14	0	0	0	0	27	22	22	11	MOVE A R(7) <= R(4)				
1		25533	1	3	0	7	0	0		15	0	0	0	0	27	22	11	22	MOVE B R(3) <= R(7)				
1		3992	0	0	3	7	0	0		6	0	0	0	0	27	22	22	22	STORE B MEM(R(3)) <= R(7)				
1		4056	0	0	3	7	1	0		6	0	0	0	0	95	22	22	95	STORE CONST MEM(R(3)) <= Const_in				
1		1088	0	0	1	0	1	0		0	0	0	0	1	0	22	0	0	TEST R(1) using bus A: set NCVZ bits using ADD immediate Y=A + 0 alu command				
1		-11727	1	6	4	4	0	0		12	0	0	0	0	0	22	22	22	R(6) <= R(4) xor R(4)				
1		-15112	0	6	1	1	1	0		14	0	0	0	1	0	22	0	0	TEST R(1) using bus A: set NCVZ bits using Y=X alu command				
1		-51	1	7	7	7	1	0		3	0	1	0	0	95	22	21	95	R(7) <= R(7) - 1				
1		-9271	1	6	6	7	1	0		2	0	0	0	0	95	22	1	95	R(6) <= R(6) + 1				
1		-40	0	7	7	7	1	0		6	0	0	0	0	95	22	21	95	SET ALU NOP	DA=R(7)	AA=R(7)	BA=R(7)	NO WRITE

clk	ctrl	word	RW	DA	AA	BA	MB	MD	ALU_mode	ALU_function	N	C	V	Z	Const_in	Data_in	Address_out	Data_out	Comment				
1		0	U		0	0	0	U	U		0	0	0	0	1	11	0	0	RESET				
1		27	1	0	0	0	0	1		6	0	0	0	0	1	11	11	11	LOAD R(0) <= MEM(R(0))				
1		-32677	1	4	0	0	1	1		6	0	0	0	0	1	22	11	1	LOAD R(4) <= MEM(R(0))				
1		-24063	1	5	0	4	0	0		0	0	0	0	0	1	22	11	22	ADD R(5) <= R(0) + R(4)				
1		-12223	1	6	4	0	1	0		0	0	0	0	0	27	22	22	27	ADI R(6) <= R(4) + Const_in				
1		-4039	1	7	4	0	0	0		14	0	0	0	0	27	22	22	11	MOVE A R(7) <= R(4)				
1		25533	1	3	0	7	0	0		15	0	0	0	0	27	22	11	22	MOVE B R(3) <= R(7)				
1		3992	0	0	3	7	0	0		6	0	0	0	0	27	22	22	22	STORE B MEM(R(3)) <= R(7)				
1		4056	0	0	3	7	1	0		6	0	0	0	0	95	22	22	95	STORE CONST MEM(R(3)) <= Const_in				
1		1088	0	0	1	0	1	0		0	0	0	0	1	0	22	0	0	TEST R(1) using bus A: set NCVZ bits using ADD immediate Y=A + 0 alu command				
1		-11727	1	6	4	4	0	0		12	0	0	0	0	0	22	22	22	R(6) <= R(4) xor R(4)				
1		-15112	0	6	1	1	1	0		14	0	0	0	1	0	22	0	0	TEST R(1) using bus A: set NCVZ bits using Y=X alu command				
1		-51	1	7	7	7	1	0		3	0	1	0	0	95	22	21	95	R(7) <= R(7) - 1				
1		-9271	1	6	6	7	1	0		2	0	0	0	0	95	22	1	95	R(6) <= R(6) + 1				
1		-40	0	7	7	7	1	0		6	0	0	0	0	95	22	21	95	SET ALU NOP	DA=R(7)	AA=R(7)	BA=R(7)	NO WRITE

clk	ctrl	word	RW	DA	AA	BA	MB	MD	ALU_mode	ALU_function	N	C	V	Z	Const_in	Data_in	Address_out	Data_out	Comment				
1		0	U	0	0	0	U	U		0	0	0	0	0	1	11	0	0	RESET				
1		27	1	0	0	0	0	1		6	0	0	0	0	1	11	11	11	LOAD R(0) <= MEM(R(0))				
1		-32677	1	4	0	0	1	1		6	0	0	0	0	1	22	11	1	LOAD R(4) <= MEM(R(0))				
1		-24063	1	5	0	4	0	0		0	0	0	0	0	1	22	11	22	ADD R(5) <= R(0) + R(4)				
1		-12223	1	6	4	0	1	0		0	0	0	0	0	27	22	22	27	ADI R(6) <= R(4) + Const_in				
1		-4039	1	7	4	0	0	0		14	0	0	0	0	27	22	22	11	MOVE A R(7) <= R(4)				
1		25533	1	3	0	7	0	0		15	0	0	0	0	27	22	11	22	MOVE B R(3) <= R(7)				
1		3992	0	0	3	7	0	0		6	0	0	0	0	27	22	22	22	STORE B MEM(R(3)) <= R(7)				
1		4056	0	0	3	7	1	0		6	0	0	0	0	95	22	22	95	STORE CONST MEM(R(3)) <= Const_in				
1		1088	0	0	1	0	1	0		0	0	0	0	1	0	22	0	0	TEST R(1) using bus A: set NCVZ bits using ADD immediate Y=A + 0 alu command				
1		-11727	1	6	4	4	0	0		12	0	0	0	0	0	22	22	22	R(6) <= R(4) xor R(4)				
1		-15112	0	6	1	1	1	0		14	0	0	0	1	0	22	0	0	TEST R(1) using bus A: set NCVZ bits using Y=X alu command				
1		-51	1	7	7	7	1	0		3	0	1	0	0	95	22	21	95	R(7) <= R(7) - 1				
1		-9271	1	6	6	7	1	0		2	0	0	0	0	95	22	1	95	R(6) <= R(6) + 1				
1		-40	0	7	7	7	1	0		6	0	0	0	0	95	22	21	95	SET ALU NOP	DA=R(7)	AA=R(7)	BA=R(7)	NO WRITE

clk	ctrl	word	RW	DA	AA	BA	MB	MD	ALU_mode	ALU_function	N	C	V	Z	Const_in	Data_in	Address_out	Data_out	Comment				
1		0	U		0	0	0	U	U		0	0	0	0	1	11	0	0	RESET				
1		27	1	0	0	0	0	1		6	0	0	0	0	1	11	11	11	LOAD R(0) <= MEM(R(0))				
1		-32677	1	4	0	0	1	1		6	0	0	0	0	1	22	11	1	LOAD R(4) <= MEM(R(0))				
1		-24063	1	5	0	4	0	0		0	0	0	0	0	1	22	11	22	ADD R(5) <= R(0) + R(4)				
1		-12223	1	6	4	0	1	0		0	0	0	0	0	27	22	22	27	ADI R(6) <= R(4) + Const_in				
1		-4039	1	7	4	0	0	0		14	0	0	0	0	27	22	22	11	MOVE A R(7) <= R(4)				
1		25533	1	3	0	7	0	0		15	0	0	0	0	27	22	11	22	MOVE B R(3) <= R(7)				
1		3992	0	0	3	7	0	0		6	0	0	0	0	27	22	22	22	STORE B MEM(R(3)) <= R(7)				
1		4056	0	0	3	7	1	0		6	0	0	0	0	95	22	22	95	STORE CONST MEM(R(3)) <= Const_in				
1		1088	0	0	1	0	1	0		0	0	0	0	1	0	22	0	0	TEST R(1) using bus A: set NCVZ bits using ADD immediate Y=A + 0 alu command				
1		-11727	1	6	4	4	0	0		12	0	0	0	0	0	22	22	22	R(6) <= R(4) xor R(4)				
1		-15112	0	6	1	1	1	0		14	0	0	0	1	0	22	0	0	TEST R(1) using bus A: set NCVZ bits using Y=X alu command				
1		-51	1	7	7	7	1	0		3	0	1	0	0	95	22	21	95	R(7) <= R(7) - 1				
1		-9271	1	6	6	7	1	0		2	0	0	0	0	95	22	1	95	R(6) <= R(6) + 1				
1		-40	0	7	7	7	1	0		6	0	0	0	0	95	22	21	95	SET ALU NOP	DA=R(7)	AA=R(7)	BA=R(7)	NO WRITE

clk	ctrl	word	RW	DA	AA	BA	MB	MD	ALU_mode	ALU_function	N	C	V	Z	Const_in	Data_in	Address_out	Data_out	Comment				
1		0	U		0	0	0	U	U		0	0	0	0	1	11	0	0	RESET				
1		27	1	0	0	0	0	1		6	0	0	0	0	1	11	11	11	LOAD R(0) <= MEM(R(0))				
1		-32677	1	4	0	0	1	1		6	0	0	0	0	1	22	11	1	LOAD R(4) <= MEM(R(0))				
1		-24063	1	5	0	4	0	0		0	0	0	0	0	1	22	11	22	ADD R(5) <= R(0) + R(4)				
1		-12223	1	6	4	0	1	0		0	0	0	0	0	27	22	22	27	ADI R(6) <= R(4) + Const_in				
1		-4039	1	7	4	0	0	0		14	0	0	0	0	27	22	22	11	MOVE A R(7) <= R(4)				
1		25533	1	3	0	7	0	0		15	0	0	0	0	27	22	11	22	MOVE B R(3) <= R(7)				
1		3992	0	0	3	7	0	0		6	0	0	0	0	27	22	22	22	STORE B MEM(R(3)) <= R(7)				
1		4056	0	0	3	7	1	0		6	0	0	0	0	95	22	22	95	STORE CONST MEM(R(3)) <= Const_in				
1		1088	0	0	1	0	1	0		0	0	0	0	1	0	22	0	0	TEST R(1) using bus A: set NCVZ bits using ADD immediate Y=A + 0 alu command				
1		-11727	1	6	4	4	0	0		12	0	0	0	0	0	22	22	22	R(6) <= R(4) xor R(4)				
1		-15112	0	6	1	1	1	0		14	0	0	0	1	0	22	0	0	TEST R(1) using bus A: set NCVZ bits using Y=X alu command				
1		-51	1	7	7	7	1	0		3	0	1	0	0	95	22	21	95	R(7) <= R(7) - 1				
1		-9271	1	6	6	7	1	0		2	0	0	0	0	95	22	1	95	R(6) <= R(6) + 1				
1		-40	0	7	7	7	1	0		6	0	0	0	0	95	22	21	95	SET ALU NOP	DA=R(7)	AA=R(7)	BA=R(7)	NO WRITE

clk	ctrl	word	RW	DA	AA	BA	MB	MD	ALU_mode	ALU_function	N	C	V	Z	Const_in	Data_in	Address_out	Data_out	Comment				
1		0	U		0	0	0	U	U		0	0	0	0	1	11	0	0	RESET				
1		27	1	0	0	0	0	1		6	0	0	0	0	1	11	11	11	LOAD R(0) <= MEM(R(0))				
1		-32677	1	4	0	0	1	1		6	0	0	0	0	1	22	11	1	LOAD R(4) <= MEM(R(0))				
1		-24063	1	5	0	4	0	0		0	0	0	0	0	1	22	11	22	ADD R(5) <= R(0) + R(4)				
1		-12223	1	6	4	0	1	0		0	0	0	0	0	27	22	22	27	ADI R(6) <= R(4) + Const_in				
1		-4039	1	7	4	0	0	0		14	0	0	0	0	27	22	22	11	MOVE A R(7) <= R(4)				
1		25533	1	3	0	7	0	0		15	0	0	0	0	27	22	11	22	MOVE B R(3) <= R(7)				
1		3992	0	0	3	7	0	0		6	0	0	0	0	27	22	22	22	STORE B MEM(R(3)) <= R(7)				
1		4056	0	0	3	7	1	0		6	0	0	0	0	95	22	22	95	STORE CONST MEM(R(3)) <= Const_in				
1		1088	0	0	1	0	1	0		0	0	0	0	1	0	22	0	0	TEST R(1) using bus A: set NCVZ bits using ADD immediate Y=A + 0 alu command				
1		-11727	1	6	4	4	0	0		12	0	0	0	0	0	22	22	22	R(6) <= R(4) xor R(4)				
1		-15112	0	6	1	1	1	0		14	0	0	0	1	0	22	0	0	TEST R(1) using bus A: set NCVZ bits using Y=X alu command				
1		-51	1	7	7	7	1	0		3	0	1	0	0	95	22	21	95	R(7) <= R(7) - 1				
1		-9271	1	6	6	7	1	0		2	0	0	0	0	95	22	1	95	R(6) <= R(6) + 1				
1		-40	0	7	7	7	1	0		6	0	0	0	0	95	22	21	95	SET ALU NOP	DA=R(7)	AA=R(7)	BA=R(7)	NO WRITE

clk	ctrl	word	RW	DA	AA	BA	MB	MD	ALU_mode	ALU_function	N	C	V	Z	Const_in	Data_in	Address_out	Data_out	Comment				
1		0	U	0	0	0	U	U		0	0	0	0	0	1	11	0	0	RESET				
1		27	1	0	0	0	0	1		6	0	0	0	0	1	11	11	11	LOAD R(0) <= MEM(R(0))				
1		-32677	1	4	0	0	1	1		6	0	0	0	0	1	22	11	1	LOAD R(4) <= MEM(R(0))				
1		-24063	1	5	0	4	0	0		0	0	0	0	0	1	22	11	22	ADD R(5) <= R(0) + R(4)				
1		-12223	1	6	4	0	1	0		0	0	0	0	0	27	22	22	27	ADI R(6) <= R(4) + Const_in				
1		-4039	1	7	4	0	0	0		14	0	0	0	0	27	22	22	11	MOVE A R(7) <= R(4)				
1		25533	1	3	0	7	0	0		15	0	0	0	0	27	22	11	22	MOVE B R(3) <= R(7)				
1		3992	0	0	3	7	0	0		6	0	0	0	0	27	22	22	22	STORE B MEM(R(3)) <= R(7)				
1		4056	0	0	3	7	1	0		6	0	0	0	0	95	22	22	95	STORE CONST MEM(R(3)) <= Const_in				
1		1088	0	0	1	0	1	0		0	0	0	0	1	0	22	0	0	TEST R(1) using bus A: set NCVZ bits using ADD immediate Y=A + 0 alu command				
1		-11727	1	6	4	4	0	0		12	0	0	0	0	0	22	22	22	R(6) <= R(4) xor R(4)				
1		-15112	0	6	1	1	1	0		14	0	0	0	1	0	22	0	0	TEST R(1) using bus A: set NCVZ bits using Y=X alu command				
1		-51	1	7	7	7	1	0		3	0	1	0	0	95	22	21	95	R(7) <= R(7) - 1				
1		-9271	1	6	6	7	1	0		2	0	0	0	0	95	22	1	95	R(6) <= R(6) + 1				
1		-40	0	7	7	7	1	0		6	0	0	0	0	95	22	21	95	SET ALU NOP	DA=R(7)	AA=R(7)	BA=R(7)	NO WRITE

clk	ctrl	word	RW	DA	AA	BA	MB	MD	ALU_mode	ALU_function	N	C	V	Z	Const_in	Data_in	Address_out	Data_out	Comment				
1		0	U	0	0	0	U	U		0	0	0	0	0	1	11	0	0	RESET				
1		27	1	0	0	0	0	1		6	0	0	0	0	1	11	11	11	LOAD R(0) <= MEM(R(0))				
1		-32677	1	4	0	0	1	1		6	0	0	0	0	1	22	11	1	LOAD R(4) <= MEM(R(0))				
1		-24063	1	5	0	4	0	0		0	0	0	0	0	1	22	11	22	ADD R(5) <= R(0) + R(4)				
1		-12223	1	6	4	0	1	0		0	0	0	0	0	27	22	22	27	ADI R(6) <= R(4) + Const_in				
1		-4039	1	7	4	0	0	0		14	0	0	0	0	27	22	22	11	MOVE A R(7) <= R(4)				
1		25533	1	3	0	7	0	0		15	0	0	0	0	27	22	11	22	MOVE B R(3) <= R(7)				
1		3992	0	0	3	7	0	0		6	0	0	0	0	27	22	22	22	STORE B MEM(R(3)) <= R(7)				
1		4056	0	0	3	7	1	0		6	0	0	0	0	95	22	22	95	STORE CONST MEM(R(3)) <= Const_in				
1		1088	0	0	1	0	1	0		0	0	0	0	1	0	22	0	0	TEST R(1) using bus A: set NCVZ bits using ADD immediate Y=A + 0 alu command				
1		-11727	1	6	4	4	0	0		12	0	0	0	0	0	22	22	22	R(6) <= R(4) xor R(4)				
1		-15112	0	6	1	1	1	0		14	0	0	0	1	0	22	0	0	TEST R(1) using bus A: set NCVZ bits using Y=X alu command				
1		-51	1	7	7	7	1	0		3	0	1	0	0	95	22	21	95	R(7) <= R(7) - 1				
1		-9271	1	6	6	7	1	0		2	0	0	0	0	95	22	1	95	R(6) <= R(6) + 1				
1		-40	0	7	7	7	1	0		6	0	0	0	0	95	22	21	95	SET ALU NOP	DA=R(7)	AA=R(7)	BA=R(7)	NO WRITE

clk	ctrl	word	RW	DA	AA	BA	MB	MD	ALU_mode	ALU_function	N	C	V	Z	Const_in	Data_in	Address_out	Data_out	Comment				
1		0	U		0	0	0	U	U		0	0	0	0	1	11	0	0	RESET				
1		27	1	0	0	0	0	1		6	0	0	0	0	1	11	11	11	LOAD R(0) <= MEM(R(0))				
1		-32677	1	4	0	0	1	1		6	0	0	0	0	1	22	11	1	LOAD R(4) <= MEM(R(0))				
1		-24063	1	5	0	4	0	0		0	0	0	0	0	1	22	11	22	ADD R(5) <= R(0) + R(4)				
1		-12223	1	6	4	0	1	0		0	0	0	0	0	27	22	22	27	ADI R(6) <= R(4) + Const_in				
1		-4039	1	7	4	0	0	0		14	0	0	0	0	27	22	22	11	MOVE A R(7) <= R(4)				
1		25533	1	3	0	7	0	0		15	0	0	0	0	27	22	11	22	MOVE B R(3) <= R(7)				
1		3992	0	0	3	7	0	0		6	0	0	0	0	27	22	22	22	STORE B MEM(R(3)) <= R(7)				
1		4056	0	0	3	7	1	0		6	0	0	0	0	95	22	22	95	STORE CONST MEM(R(3)) <= Const_in				
1		1088	0	0	1	0	1	0		0	0	0	0	1	0	22	0	0	TEST R(1) using bus A: set NCVZ bits using ADD immediate Y=A + 0 alu command				
1		-11727	1	6	4	4	0	0		12	0	0	0	0	0	22	22	22	R(6) <= R(4) xor R(4)				
1		-15112	0	6	1	1	1	0		14	0	0	0	1	0	22	0	0	TEST R(1) using bus A: set NCVZ bits using Y=X alu command				
1		-51	1	7	7	7	1	0		3	0	1	0	0	95	22	21	95	R(7) <= R(7) - 1				
1		-9271	1	6	6	7	1	0		2	0	0	0	0	95	22	1	95	R(6) <= R(6) + 1				
1		-40	0	7	7	7	1	0		6	0	0	0	0	95	22	21	95	SET ALU NOP	DA=R(7)	AA=R(7)	BA=R(7)	NO WRITE

clk	ctrl	word	RW	DA	AA	BA	MB	MD	ALU_mode	ALU_function	N	C	V	Z	Const_in	Data_in	Address_out	Data_out	Comment				
1		0	U		0	0	0	U	U		0	0	0	0	1	11	0	0	RESET				
1		27	1	0	0	0	0	1		6	0	0	0	0	1	11	11	11	LOAD R(0) <= MEM(R(0))				
1		-32677	1	4	0	0	1	1		6	0	0	0	0	1	22	11	1	LOAD R(4) <= MEM(R(0))				
1		-24063	1	5	0	4	0	0		0	0	0	0	0	1	22	11	22	ADD R(5) <= R(0) + R(4)				
1		-12223	1	6	4	0	1	0		0	0	0	0	0	27	22	22	27	ADI R(6) <= R(4) + Const_in				
1		-4039	1	7	4	0	0	0		14	0	0	0	0	27	22	22	11	MOVE A R(7) <= R(4)				
1		25533	1	3	0	7	0	0		15	0	0	0	0	27	22	11	22	MOVE B R(3) <= R(7)				
1		3992	0	0	3	7	0	0		6	0	0	0	0	27	22	22	22	STORE B MEM(R(3)) <= R(7)				
1		4056	0	0	3	7	1	0		6	0	0	0	0	95	22	22	95	STORE CONST MEM(R(3)) <= Const_in				
1		1088	0	0	1	0	1	0		0	0	0	0	1	0	22	0	0	TEST R(1) using bus A: set NCVZ bits using ADD immediate Y=A + 0 alu command				
1		-11727	1	6	4	4	0	0		12	0	0	0	0	0	22	22	22	R(6) <= R(4) xor R(4)				
1		-15112	0	6	1	1	1	0		14	0	0	0	1	0	22	0	0	TEST R(1) using bus A: set NCVZ bits using Y=X alu command				
1		-51	1	7	7	7	1	0		3	0	1	0	0	95	22	21	95	R(7) <= R(7) - 1				
1		-9271	1	6	6	7	1	0		2	0	0	0	0	95	22	1	95	R(6) <= R(6) + 1				
1		-40	0	7	7	7	1	0		6	0	0	0	0	95	22	21	95	SET ALU NOP	DA=R(7)	AA=R(7)	BA=R(7)	NO WRITE

IDEAL

ctrl	word	RW	DA	AA	BA	MB	MD	ALU mode	ALU function	N	C	V	Z	Const in	Data in	Address out	Data out	Comment				
1	0	U	0	0	0	U	U		0	0	0	0		1	11		0	0 RESET				
1	27	1	0	0	0	0	1		6	0	0	0		1	11		11	11 LOAD R(0) <= MEM(R(0))				
1	-32677	1	4	0	0	1	1		6	0	0	0		1	22		11	1 LOAD R(4) <= MEM(R(0))				
1	-24063	1	5	0	4	0	0		0	0	0	0		1	22		11	22 ADD R(5) <= R(0) + R(4)				
1	-12223	1	6	4	0	1	0		0	0	0	0		27	22		22	27 ADI R(6) <= R(4) + Const in				
1	-4039	1	7	4	0	0	0		14	0	0	0		27	22		22	11 MOVE A R(7) <= R(4)				
1	25533	1	3	0	7	0	0		15	0	0	0		27	22		11	22 MOVE B R(3) <= R(7)				
1	3992	0	0	3	7	0	0		6	0	0	0		27	22		22	22 STORE B MEM(R(3)) <= R(7)				
1	4056	0	0	3	7	1	0		6	0	0	0		95	22		22	95 STORE CONST MEM(R(3)) <= Const in				
1	1088	0	0	1	0	1	0		0	0	0	1		0	22		0	0 TEST R(1) using bus A: set NCVZ bits using ADD immediate Y=A + 0 alu command				
1	-11727	1	6	4	4	0	0		12	0	0	0		0	22		22	22 R(6) <= R(4) xor R(4)				
1	-15112	0	6	1	1	1	0		14	0	0	1		0	22		0	0 TEST R(1) using bus A: set NCVZ bits using Y=X alu command				
1	-51	1	7	7	7	1	0		3	0	1	0		95	22		21	95 R(7) <= R(7) - 1				
1	-9271	1	6	6	7	1	0		2	0	0	0		95	22		1	95 R(6) <= R(6) + 1				
1	-40	0	7	7	7	1	0		6	0	0	0		95	22		21	95 SET ALU NOP	DA=R(7)	AA=R(7)	BA=R(7)	NO WRITE