

ERROR:HDLParasers:850 - "64200100/cpu.vhd" Line 132. Formal port DataIn does not exist in Compon
ERROR:HDLParasers:850 - "64200100/cpu.vhd" Line 133. Formal port AddressOut does not exist in Coi
ERROR:HDLParasers:850 - "64200100/cpu.vhd" Line 134. Formal port DataOut does not exist in Comp
ERROR:HDLParasers:1418 - "64200112/cpu.vhd" Line 83. Formal generic ctrl_width does not exist in br
ERROR:HDLParasers:843 - "64200112/cpu.vhd" Line 117. Formal Data_in of cpu_datapath is used twic

ient 'cpu_datapath'.
mponent 'cpu_datapath'.
onent 'cpu_datapath'.
anch_ctrl.
e.

>xst -fh cpu.xst	>xst -fh cpu.xst
Release 14.7 - xst P.20131013 (m64)	Release 14.7 - xst P.20131013 (m64)
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--> Parameter TMPDIR set to ./xstprojdir/tmp	--> Parameter TMPDIR set to ./xstprojdir/tmp
Total REAL time to Xst completion: 0.00 secs	Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.31 secs	Total CPU time to Xst completion: 0.24 secs
--> WARNING:Xst-3164 - Option "-debug" found multiple times in the command line. Only the first occurrence is considered.	--> WARNING:Xst-3164 - Option "-debug" found multiple times in the command line. Only the first occurrence is considered.
* HDL Compilation *	* HDL Compilation *
Compiling vhdl file "muxent01.vhd" in Library work.	Compiling vhdl file "muxent01.vhd" in Library work.
Entity <muxent01> compiled.	Entity <muxent01> compiled.
Entity <muxent01> (Architecture <ideal>) compiled.	Entity <muxent01> (Architecture <=>) compiled.
Compiling vhdl file "dff.vhd" in Library work.	Compiling vhdl file "dff.vhd" in Library work.
Entity <dff> compiled.	Entity <dff> compiled.
Entity <dff> (Architecture <ideal>) compiled.	Entity <dff> (Architecture <=>) compiled.
Compiling vhdl file "cda_gp.vhd" in Library work.	Compiling vhdl file "cda_gp.vhd" in Library work.
Entity <cda_gp> compiled.	Entity <cda_gp> compiled.
Entity <cda_gp> (Architecture <ideal>) compiled.	Entity <cda_gp> (Architecture <=>) compiled.
Compiling vhdl file "muxdff.vhd" in Library work.	Compiling vhdl file "muxdff.vhd" in Library work.
Entity <muxdff> compiled.	Entity <muxdff> compiled.
Entity <muxdff> (Architecture <ideal>) compiled.	Entity <muxdff> (Architecture <=>) compiled.
Compiling vhdl file "req_file_functions.vhd" in Library work.	Compiling vhdl file "req_file_functions.vhd" in Library work.
Package <req_file_functions> compiled.	Package <req_file_functions> compiled.
Package body <req_file_functions> compiled.	Package body <req_file_functions> compiled.
Compiling vhdl file "cda_add_n_bit.vhd" in Library work.	Compiling vhdl file "cda_add_n_bit.vhd" in Library work.
Entity <cda_add_n_bit> compiled.	Entity <cda_add_n_bit> compiled.
Entity <cda_add_n_bit> (Architecture <ideal>) compiled.	Entity <cda_add_n_bit> (Architecture <=>) compiled.
Compiling vhdl file "dmuxent01.vhd" in Library work.	Compiling vhdl file "dmuxent01.vhd" in Library work.
Entity <dmuxent01> compiled.	Entity <dmuxent01> compiled.
Entity <dmuxent01> (Architecture <ideal>) compiled.	Entity <dmuxent01> (Architecture <=>) compiled.
Compiling vhdl file "muxent01_bus.vhd" in Library work.	Compiling vhdl file "muxent01_bus.vhd" in Library work.
Entity <muxent01_bus> compiled.	Entity <muxent01_bus> compiled.
Entity <muxent01_bus> (Architecture <ideal>) compiled.	Entity <muxent01_bus> (Architecture <=>) compiled.
Compiling vhdl file "shift_req.vhd" in Library work.	Compiling vhdl file "shift_req.vhd" in Library work.
Entity <shift_req> compiled.	Entity <shift_req> compiled.
Entity <shift_req> (Architecture <ideal>) compiled.	Entity <shift_req> (Architecture <=>) compiled.
Compiling vhdl file "rcpu_datapath_functions.vhd" in Library work.	Compiling vhdl file "branch_ctrl_functions.vhd" in Library work.
Package <cpu_datapath_functions> compiled.	Package <branch_ctrl_functions> compiled.
Compiling vhdl file "req_file.vhd" in Library work.	Package body <branch_ctrl_functions> compiled.
Entity <req_file> compiled.	Compiling vhdl file "counter.vhd" in Library work.
Entity <req_file> (Architecture <ideal>) compiled.	Entity <counter> compiled.
Compiling vhdl file "rnda_alu_cda.vhd" in Library work.	Entity <counter> (Architecture <=>) compiled.
Entity <rnda_alu> compiled.	Compiling vhdl file "rcpu_datapath_functions.vhd" in Library work.
Entity <rnda_alu> (Architecture <ideal>) compiled.	Package <cpu_datapath_functions> compiled.
Compiling vhdl file "branch_ctrl_functions.vhd" in Library work.	Compiling vhdl file "req_file.vhd" in Library work.
Package <branch_ctrl_functions> compiled.	Entity <req_file> compiled.
Package body <branch_ctrl_functions> compiled.	Entity <req_file> (Architecture <=>) compiled.
Compiling vhdl file "counter.vhd" in Library work.	Compiling vhdl file "rnda_alu_cda.vhd" in Library work.
Entity <counter> compiled.	Entity <rnda_alu> compiled.
Entity <counter> (Architecture <ideal>) compiled.	Entity <rnda_alu> (Architecture <=>) compiled.
Compiling vhdl file "rcpu_functions.vhd" in Library work.	Compiling vhdl file "rcpu_functions.vhd" in Library work.
Package <cpu_functions> compiled.	Package <cpu_functions> compiled.
Compiling vhdl file "branch_ctrl.vhd" in Library work.	Compiling vhdl file "rcpu_datapath.vhd" in Library work.
Entity <branch_ctrl> compiled.	Entity <cpu_datapath> compiled.
Entity <branch_ctrl> (Architecture <ideal>) compiled.	Entity <cpu_datapath> (Architecture <=>) compiled.
Compiling vhdl file "rcpu_datapath.vhd" in Library work.	Compiling vhdl file "branch_ctrl.vhd" in Library work.
Entity <cpu_datapath> compiled.	Entity <branch_ctrl> compiled.
Entity <cpu_datapath> (Architecture <ideal>) compiled.	Entity <branch_ctrl> (Architecture <=>) compiled.
Compiling vhdl file "rcpu.vhd" in Library work.	Compiling vhdl file "rcpu.vhd" in Library work.
Entity <rcpu> compiled.	Entity <rcpu> compiled.
Entity <rcpu> (Architecture <ideal>) compiled.	Entity <rcpu> (Architecture <=>) compiled.
Compiling vhdl file "rom.vhd" in Library work.	Compiling vhdl file "rom.vhd" in Library work.
Entity <rom> compiled.	Entity <rom> compiled.
Entity <rom> (Architecture <ideal>) compiled.	Entity <rom> (Architecture <=>) compiled.
Compiling vhdl file "sram.vhd" in Library work.	Compiling vhdl file "sram.vhd" in Library work.
Entity <sram> compiled.	Entity <sram> compiled.

>xst -ifn cpu.xst	>xst -ifn cpu.xst
Release 14.7 - xst P 20131013 (n164)	Release 14.7 - xst P 20131013 (n164)
Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.	Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.
--> Parameter TMPDIR set to ./xst/projnav/tmp	--> Parameter TMPDIR set to ./xst/projnav/tmp
Total REAL time to Xst completion: 1.00 secs	Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.25 secs	Total CPU time to Xst completion: 0.24 secs
--> WARNING:Xst:3164 - Option "-debug" found multiple times in the command line. Only the first occurrence is considered.	--> WARNING:Xst:3164 - Option "-debug" found multiple times in the command line. Only the first occurrence is considered.
* HDL Compilation *	* HDL Compilation *
Compiling vhd file "muxnto1.vhd" in Library work.	Compiling vhd file "muxnto1.vhd" in Library work.
Entity <muxnto1> compiled.	Entity <muxnto1> compiled.
Entity <muxnto1> (Architecture <ideal>) compiled.	Entity <muxnto1> (Architecture <=>) compiled.
Compiling vhd file "dff.vhd" in Library work.	Compiling vhd file "dff.vhd" in Library work.
Entity <dff> compiled.	Entity <dff> compiled.
Entity <dff> (Architecture <ideal>) compiled.	Entity <dff> (Architecture <=>) compiled.
Compiling vhd file "cda_gp.vhd" in Library work.	Compiling vhd file "cda_gp.vhd" in Library work.
Entity <cda_gp> compiled.	Entity <cda_gp> compiled.
Entity <cda_gp> (Architecture <ideal>) compiled.	Entity <cda_gp> (Architecture <=>) compiled.
Compiling vhd file "muxdff.vhd" in Library work.	Compiling vhd file "muxdff.vhd" in Library work.
Entity <muxdff> compiled.	Entity <muxdff> compiled.
Entity <muxdff> (Architecture <ideal>) compiled.	Entity <muxdff> (Architecture <=>) compiled.
Compiling vhd file "reg_file_functions.vhd" in Library work.	Compiling vhd file "reg_file_functions.vhd" in Library work.
Package <reg_file_functions> compiled.	Package <reg_file_functions> compiled.
Package body <reg_file_functions> compiled.	Package body <reg_file_functions> compiled.
Compiling vhd file "cda_add_n_bit.vhd" in Library work.	Compiling vhd file "cda_add_n_bit.vhd" in Library work.
Entity <cda_add_n_bit> compiled.	Entity <cda_add_n_bit> compiled.
Entity <cda_add_n_bit> (Architecture <ideal>) compiled.	Entity <cda_add_n_bit> (Architecture <=>) compiled.
Compiling vhd file "dmuxnto1.vhd" in Library work.	Compiling vhd file "dmuxnto1.vhd" in Library work.
Entity <dmuxnto1> compiled.	Entity <dmuxnto1> compiled.
Entity <dmuxnto1> (Architecture <ideal>) compiled.	Entity <dmuxnto1> (Architecture <=>) compiled.
Compiling vhd file "muxnto1_bus.vhd" in Library work.	Compiling vhd file "muxnto1_bus.vhd" in Library work.
Entity <muxnto1_bus> compiled.	Entity <muxnto1_bus> compiled.
Entity <muxnto1_bus> (Architecture <ideal>) compiled.	Entity <muxnto1_bus> (Architecture <=>) compiled.
Compiling vhd file "shift_req.vhd" in Library work.	Compiling vhd file "shift_req.vhd" in Library work.
Entity <shift_req> compiled.	Entity <shift_req> compiled.
Entity <shift_req> (Architecture <ideal>) compiled.	Entity <shift_req> (Architecture <=>) compiled.
Compiling vhd file "cpu_datapath_functions.vhd" in Library work.	Compiling vhd file "branch_ctrl_functions.vhd" in Library work.
Package <cpu_datapath_functions> compiled.	Package <branch_ctrl_functions> compiled.
Compiling vhd file "reg_file.vhd" in Library work.	Package body <branch_ctrl_functions> compiled.
Entity <reg_file> compiled.	Compiling vhd file "counter.vhd" in Library work.
Entity <reg_file> (Architecture <ideal>) compiled.	Entity <counter> compiled.
Compiling vhd file "ndn_alu.vhd" in Library work.	Entity <counter> (Architecture <=>) compiled.
Entity <ndn_alu> compiled.	Compiling vhd file "cpu_datapath_functions.vhd" in Library work.
Entity <ndn_alu> (Architecture <ideal>) compiled.	Package <cpu_datapath_functions> compiled.
Compiling vhd file "branch_ctrl_functions.vhd" in Library work.	Compiling vhd file "reg_file.vhd" in Library work.
Package <branch_ctrl_functions> compiled.	Entity <reg_file> compiled.
Package body <branch_ctrl_functions> compiled.	Entity <reg_file> (Architecture <=>) compiled.
Compiling vhd file "counter.vhd" in Library work.	Compiling vhd file "ndn_alu_cda.vhd" in Library work.
Entity <counter> compiled.	Entity <ndn_alu> compiled.
Entity <counter> (Architecture <ideal>) compiled.	Entity <ndn_alu> (Architecture <=>) compiled.
Compiling vhd file "cpu_functions.vhd" in Library work.	Compiling vhd file "cpu_functions.vhd" in Library work.
Package <cpu_functions> compiled.	Package <cpu_functions> compiled.
Compiling vhd file "branch_ctrl.vhd" in Library work.	Compiling vhd file "cpu_datapath.vhd" in Library work.
Entity <branch_ctrl> compiled.	Entity <cpu_datapath> compiled.
Entity <branch_ctrl> (Architecture <ideal>) compiled.	Entity <cpu_datapath> (Architecture <=>) compiled.
Compiling vhd file "cpu_datapath.vhd" in Library work.	Compiling vhd file "branch_ctrl.vhd" in Library work.
Entity <cpu_datapath> compiled.	Entity <branch_ctrl> compiled.
Entity <cpu_datapath> (Architecture <ideal>) compiled.	Entity <branch_ctrl> (Architecture <=>) compiled.
Compiling vhd file "cpu.vhd" in Library work.	Compiling vhd file "cpu.vhd" in Library work.
Entity <cpu> compiled.	Entity <cpu> compiled.
ERROR:HDLParas:850 - "cpu.vhd" Line 132. Formal port DataIn does not exist in Component 'cpu_datapath'.	Entity <cpu> (Architecture <=>) compiled.
ERROR:HDLParas:850 - "cpu.vhd" Line 133. Formal port AddressOut does not exist in Component 'cpu_datapath'.	Compiling vhd file "rom.vhd" in Library work.
ERROR:HDLParas:850 - "cpu.vhd" Line 134. Formal port DataOut does not exist in Component 'cpu_datapath'.	Entity <rom> compiled.
Total REAL time to Xst completion: 4.00 secs	Entity <rom> (Architecture <ndv>) compiled.
Total CPU time to Xst completion: 3.16 secs	Compiling vhd file "sram.vhd" in Library work.
	Entity <sram> compiled.

>xst -fIn cpu.xst	>xst -fIn cpu.xst
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--> Parameter TMPDIR set to ./xst/projnav.tmp	--> Parameter TMPDIR set to ./xst/projnav.tmp
Total REAL time to Xst completion: 0.00 secs	Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.23 secs	Total CPU time to Xst completion: 0.24 secs
--> WARNING:Xst:3164 - Option "-debug" found multiple times in the command line. Only the first occurrence is considered.	--> WARNING:Xst:3164 - Option "-debug" found multiple times in the command line. Only the first occurrence is considered.
* HDL Compilation *	* HDL Compilation *
Compiling vhdl file "muxnto1.vhd" in Library work.	Compiling vhdl file "muxnto1.vhd" in Library work.
Entity <muxnto1> compiled.	Entity <muxnto1> compiled.
Entity <muxnto1> (Architecture <ideal>) compiled.	Entity <muxnto1> (Architecture <=>) compiled.
Compiling vhdl file "dff.vhd" in Library work.	Compiling vhdl file "dff.vhd" in Library work.
Entity <dff> compiled.	Entity <dff> compiled.
Entity <dff> (Architecture <ideal>) compiled.	Entity <dff> (Architecture <=>) compiled.
Compiling vhdl file "ccla_gp.vhd" in Library work.	Compiling vhdl file "ccla_gp.vhd" in Library work.
Entity <ccla_gp> compiled.	Entity <ccla_gp> compiled.
Entity <ccla_gp> (Architecture <ideal>) compiled.	Entity <ccla_gp> (Architecture <=>) compiled.
Compiling vhdl file "muxdff.vhd" in Library work.	Compiling vhdl file "muxdff.vhd" in Library work.
Entity <muxdff> compiled.	Entity <muxdff> compiled.
Entity <muxdff> (Architecture <ideal>) compiled.	Entity <muxdff> (Architecture <=>) compiled.
Compiling vhdl file "reg_file_functions.vhd" in Library work.	Compiling vhdl file "reg_file_functions.vhd" in Library work.
Package <reg_file_functions> compiled.	Package <reg_file_functions> compiled.
Package body <reg_file_functions> compiled.	Package body <reg_file_functions> compiled.
Compiling vhdl file "ccla_add_n_bit.vhd" in Library work.	Compiling vhdl file "ccla_add_n_bit.vhd" in Library work.
Entity <ccla_add_n_bit> compiled.	Entity <ccla_add_n_bit> compiled.
Entity <ccla_add_n_bit> (Architecture <ideal>) compiled.	Entity <ccla_add_n_bit> (Architecture <=>) compiled.
Compiling vhdl file "dmuxnto1.vhd" in Library work.	Compiling vhdl file "dmuxnto1.vhd" in Library work.
Entity <dmuxnto1> compiled.	Entity <dmuxnto1> compiled.
Entity <dmuxnto1> (Architecture <ideal>) compiled.	Entity <dmuxnto1> (Architecture <=>) compiled.
Compiling vhdl file "muxnto1_bus.vhd" in Library work.	Compiling vhdl file "muxnto1_bus.vhd" in Library work.
Entity <muxnto1_bus> compiled.	Entity <muxnto1_bus> compiled.
Entity <muxnto1_bus> (Architecture <ideal>) compiled.	Entity <muxnto1_bus> (Architecture <=>) compiled.
Compiling vhdl file "shift_reg.vhd" in Library work.	Compiling vhdl file "shift_reg.vhd" in Library work.
Entity <shift_reg> compiled.	Entity <shift_reg> compiled.
Entity <shift_reg> (Architecture <ideal>) compiled.	Entity <shift_reg> (Architecture <=>) compiled.
Compiling vhdl file "cpu_datapath_functions.vhd" in Library work.	Compiling vhdl file "branch_ctrl_functions.vhd" in Library work.
Package <cpu_datapath_functions> compiled.	Package <branch_ctrl_functions> compiled.
Compiling vhdl file "reg_file.vhd" in Library work.	Package body <branch_ctrl_functions> compiled.
Entity <reg_file> compiled.	Compiling vhdl file "counter.vhd" in Library work.
Entity <reg_file> (Architecture <ideal>) compiled.	Entity <counter> compiled.
Compiling vhdl file "ndn_alu.vhd" in Library work.	Entity <counter> (Architecture <=>) compiled.
Entity <ndn_alu> compiled.	Compiling vhdl file "cpu_datapath_functions.vhd" in Library work.
Entity <ndn_alu> (Architecture <ideal>) compiled.	Package <cpu_datapath_functions> compiled.
Compiling vhdl file "branch_ctrl_functions.vhd" in Library work.	Compiling vhdl file "reg_file.vhd" in Library work.
Package <branch_ctrl_functions> compiled.	Entity <reg_file> compiled.
Package body <branch_ctrl_functions> compiled.	Entity <reg_file> (Architecture <=>) compiled.
Compiling vhdl file "counter.vhd" in Library work.	Compiling vhdl file "ndn_alu_cia.vhd" in Library work.
Entity <counter> compiled.	Entity <ndn_alu> compiled.
Entity <counter> (Architecture <ideal>) compiled.	Entity <ndn_alu> (Architecture <=>) compiled.
Compiling vhdl file "cpu_functions.vhd" in Library work.	Compiling vhdl file "cpu_functions.vhd" in Library work.
Package <cpu_functions> compiled.	Package <cpu_functions> compiled.
Compiling vhdl file "branch_ctrl.vhd" in Library work.	Compiling vhdl file "cpu_datapath.vhd" in Library work.
Entity <branch_ctrl> compiled.	Entity <cpu_datapath> compiled.
Entity <branch_ctrl> (Architecture <ideal>) compiled.	Entity <cpu_datapath> (Architecture <=>) compiled.
Compiling vhdl file "cpu_datapath.vhd" in Library work.	Compiling vhdl file "branch_ctrl.vhd" in Library work.
Entity <cpu_datapath> compiled.	Entity <branch_ctrl> compiled.
Entity <cpu_datapath> (Architecture <ideal>) compiled.	Entity <branch_ctrl> (Architecture <=>) compiled.
Compiling vhdl file "cpu.vhd" in Library work.	Compiling vhdl file "cpu.vhd" in Library work.
Entity <cpu> compiled.	Entity <cpu> compiled.
ERROR:HDLParas:1418 - "cpu.vhd" Line 83. Formal generic ctrl_width does not exist in branch_ctrl.	Entity <cpu> (Architecture <=>) compiled.
ERROR:HDLParas:843 - "cpu.vhd" Line 117. Formal Data in of cpu_datapath is used twice.	Compiling vhdl file "rom.vhd" in Library work.
Total REAL time to Xst completion: 3.00 secs	Entity <rom> compiled.
Total CPU time to Xst completion: 2.86 secs	Entity <rom> (Architecture <ndv>) compiled.
-->	Compiling vhdl file "sram.vhd" in Library work.
	Entity <sram> compiled.

>xst -fh cpu.xst	>xst -fh cpu.xst
Release 14.7 - xst P 20131013 (m64)	Release 14.7 - xst P 20131013 (m64)
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--> Parameter TMPDIR set to /xstprocnv/tmp	--> Parameter TMPDIR set to /xstprocnv/tmp
Total REAL time to Xst completion: 1.09 secs	Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.33 secs	Total CPU time to Xst completion: 0.24 secs
--> WARNING:Xst-3164 - Option "-debug" found multiple times in the command line. Only the first occurrence is considered.	--> WARNING:Xst-3164 - Option "-debug" found multiple times in the command line. Only the first occurrence is considered.
* HDL Compilation *	* HDL Compilation *
Compiling vhdl file "muxent01.vhd" in Library work.	Compiling vhdl file "muxent01.vhd" in Library work.
Entity <muxent01> compiled.	Entity <muxent01> compiled.
Entity <muxent01> (Architecture <ideab1>) compiled.	Entity <muxent01> (Architecture <=>) compiled.
Compiling vhdl file "dff.vhd" in Library work.	Compiling vhdl file "dff.vhd" in Library work.
Entity <dff> compiled.	Entity <dff> compiled.
Entity <dff> (Architecture <ideab1>) compiled.	Entity <dff> (Architecture <=>) compiled.
Compiling vhdl file "cila_ap.vhd" in Library work.	Compiling vhdl file "cila_ap.vhd" in Library work.
Entity <cila_ap> compiled.	Entity <cila_ap> compiled.
Entity <cila_ap> (Architecture <ideab1>) compiled.	Entity <cila_ap> (Architecture <=>) compiled.
Compiling vhdl file "muxdff.vhd" in Library work.	Compiling vhdl file "muxdff.vhd" in Library work.
Entity <muxdff> compiled.	Entity <muxdff> compiled.
Entity <muxdff> (Architecture <ideab1>) compiled.	Entity <muxdff> (Architecture <=>) compiled.
Compiling vhdl file "req_file_functions.vhd" in Library work.	Compiling vhdl file "req_file_functions.vhd" in Library work.
Package <req_file_functions> compiled.	Package <req_file_functions> compiled.
Package body <req_file_functions> compiled.	Package body <req_file_functions> compiled.
Compiling vhdl file "cila_add_n_bit.vhd" in Library work.	Compiling vhdl file "cila_add_n_bit.vhd" in Library work.
Entity <cila_add_n_bit> compiled.	Entity <cila_add_n_bit> compiled.
Entity <cila_add_n_bit> (Architecture <ideab1>) compiled.	Entity <cila_add_n_bit> (Architecture <=>) compiled.
Compiling vhdl file "dmuxent01.vhd" in Library work.	Compiling vhdl file "dmuxent01.vhd" in Library work.
Entity <dmuxent01> compiled.	Entity <dmuxent01> compiled.
Entity <dmuxent01> (Architecture <ideab1>) compiled.	Entity <dmuxent01> (Architecture <=>) compiled.
Compiling vhdl file "muxent01_bus.vhd" in Library work.	Compiling vhdl file "muxent01_bus.vhd" in Library work.
Entity <muxent01_bus> compiled.	Entity <muxent01_bus> compiled.
Entity <muxent01_bus> (Architecture <ideab2>) compiled.	Entity <muxent01_bus> (Architecture <=>) compiled.
Compiling vhdl file "shift_req.vhd" in Library work.	Compiling vhdl file "shift_req.vhd" in Library work.
Entity <shift_req> compiled.	Entity <shift_req> compiled.
Entity <shift_req> (Architecture <ideab1>) compiled.	Entity <shift_req> (Architecture <=>) compiled.
Compiling vhdl file "icpu_datapath_functions.vhd" in Library work.	Compiling vhdl file "branch_ctrl_functions.vhd" in Library work.
Package <cpu_datapath_functions> compiled.	Package <branch_ctrl_functions> compiled.
Compiling vhdl file "req_file.vhd" in Library work.	Package body <branch_ctrl_functions> compiled.
Entity <req_file> compiled.	Compiling vhdl file "counter.vhd" in Library work.
Entity <req_file> (Architecture <ideab1>) compiled.	Entity <counter> compiled.
Compiling vhdl file "rnda_alu_cila.vhd" in Library work.	Entity <counter> (Architecture <=>) compiled.
Entity <rnda_alu_cila> compiled.	Compiling vhdl file "icpu_datapath_functions.vhd" in Library work.
Entity <rnda_alu_cila> (Architecture <ideab1>) compiled.	Package <cpu_datapath_functions> compiled.
Compiling vhdl file "branch_ctrl_functions.vhd" in Library work.	Compiling vhdl file "req_file.vhd" in Library work.
Package <branch_ctrl_functions> compiled.	Entity <rnda_alu_cila> compiled.
Package body <branch_ctrl_functions> compiled.	Entity <rnda_alu_cila> (Architecture <=>) compiled.
Compiling vhdl file "counter.vhd" in Library work.	Compiling vhdl file "icpu_functions.vhd" in Library work.
Entity <counter> compiled.	Package <cpu_functions> compiled.
Entity <counter> (Architecture <ideab1>) compiled.	Compiling vhdl file "icpu_datapath.vhd" in Library work.
Compiling vhdl file "icpu_functions.vhd" in Library work.	Entity <cpu_datapath> compiled.
Package <cpu_functions> compiled.	Entity <cpu_datapath> (Architecture <=>) compiled.
Compiling vhdl file "branch_ctrl.vhd" in Library work.	Compiling vhdl file "branch_ctrl.vhd" in Library work.
Entity <branch_ctrl> compiled.	Entity <branch_ctrl> compiled.
Entity <branch_ctrl> (Architecture <ideab1>) compiled.	Entity <branch_ctrl> (Architecture <=>) compiled.
Compiling vhdl file "icpu_datapath.vhd" in Library work.	Entity <cpu_datapath> compiled.
Entity <cpu_datapath> compiled.	Entity <cpu_datapath> (Architecture <ideab1>) compiled.
Entity <cpu_datapath> (Architecture <ideab1>) compiled.	Compiling vhdl file "icpu.vhd" in Library work.
Compiling vhdl file "icpu.vhd" in Library work.	Entity <icpu> compiled.
Entity <icpu> compiled.	Entity <icpu> (Architecture <ideab1>) compiled.
Entity <icpu> (Architecture <ideab1>) compiled.	Compiling vhdl file "rom.vhd" in Library work.
Compiling vhdl file "rom.vhd" in Library work.	Entity <rom> compiled.
Entity <rom> compiled.	Entity <rom> (Architecture <ndp>) compiled.
Entity <rom> (Architecture <ndp>) compiled.	Entity <rom> (Architecture <ndp>) compiled.
Compiling vhdl file "ram.vhd" in Library work.	Compiling vhdl file "ram.vhd" in Library work.
Entity <ram> compiled.	Entity <ram> compiled.

>xst -fh cpu.xst	>xst -fh cpu.xst
Release 14.7 - xst P.20131013 (n64)	Release 14.7 - xst P.20131013 (n64)
Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.	Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.
-> Parameter TMPDIR set to /xstprojdir/tmp	-> Parameter TMPDIR set to /xstprojdir/tmp
Total REAL time to Xst completion: 0.00 secs	Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.23 secs	Total CPU time to Xst completion: 0.24 secs
-> WARNING:Xst:3164 - Option "-debug" found multiple times in the command line. Only the first occurrence is considered.	-> WARNING:Xst:3164 - Option "-debug" found multiple times in the command line. Only the first occurrence is considered.
* HDL Compilation *	* HDL Compilation *
Compiling vhdl file "muxnto1.vhd" in Library work.	Compiling vhdl file "muxnto1.vhd" in Library work.
Entity <muxnto1> compiled.	Entity <muxnto1> compiled.
Entity <muxnto1? (Architecture <ideal>) compiled.	Entity <muxnto1? (Architecture <=>) compiled.
Compiling vhdl file "dff.vhd" in Library work.	Compiling vhdl file "dff.vhd" in Library work.
Entity <dff> compiled.	Entity <dff> compiled.
Entity <dff? (Architecture <ideal>) compiled.	Entity <dff? (Architecture <=>) compiled.
Compiling vhdl file "icla_gp.vhd" in Library work.	Compiling vhdl file "icla_gp.vhd" in Library work.
Entity <icla_gp> compiled.	Entity <icla_gp> compiled.
Entity <icla_gp? (Architecture <ideal>) compiled.	Entity <icla_gp? (Architecture <=>) compiled.
Compiling vhdl file "muxdff.vhd" in Library work.	Compiling vhdl file "muxdff.vhd" in Library work.
Entity <muxdff> compiled.	Entity <muxdff> compiled.
Entity <muxdff? (Architecture <ideal>) compiled.	Entity <muxdff? (Architecture <=>) compiled.
Compiling vhdl file "req. file functions.vhd" in Library work.	Compiling vhdl file "req. file functions.vhd" in Library work.
Package <req. file functions> compiled.	Package <req. file functions> compiled.
Package body req. file functions compiled.	Package body req. file functions compiled.
Compiling vhdl file "icla_add_n_bit.vhd" in Library work.	Compiling vhdl file "icla_add_n_bit.vhd" in Library work.
Entity <icla_add_n_bit> compiled.	Entity <icla_add_n_bit> compiled.
Entity <icla_add_n_bit? (Architecture <ideal>) compiled.	Entity <icla_add_n_bit? (Architecture <=>) compiled.
Compiling vhdl file "dmuxnto1.vhd" in Library work.	Compiling vhdl file "dmuxnto1.vhd" in Library work.
Entity <dmuxnto1> compiled.	Entity <dmuxnto1> compiled.
Entity <dmuxnto1? (Architecture <ideal>) compiled.	Entity <dmuxnto1? (Architecture <=>) compiled.
Compiling vhdl file "muxnto1_bus.vhd" in Library work.	Compiling vhdl file "muxnto1_bus.vhd" in Library work.
Entity <muxnto1_bus> compiled.	Entity <muxnto1_bus> compiled.
Entity <muxnto1_bus? (Architecture <ideal>) compiled.	Entity <muxnto1_bus? (Architecture <=>) compiled.
Compiling vhdl file "shift_req.vhd" in Library work.	Compiling vhdl file "shift_req.vhd" in Library work.
Entity <shift_req> compiled.	Entity <shift_req> compiled.
Entity <shift_req? (Architecture <ideal>) compiled.	Entity <shift_req? (Architecture <=>) compiled.
Compiling vhdl file "icpu_datapath_functions.vhd" in Library work.	Compiling vhdl file "branch_ctrl_functions.vhd" in Library work.
Package <cpu_datapath_functions> compiled.	Package <branch_ctrl_functions> compiled.
Compiling vhdl file "req. file.vhd" in Library work.	Package body <branch_ctrl_functions> compiled.
Entity <req. file> compiled.	Compiling vhdl file "counter.vhd" in Library work.
Entity <req. file? (Architecture <ideal>) compiled.	Entity <counter> compiled.
Compiling vhdl file "rnda_alu_cia.vhd" in Library work.	Entity <counter? (Architecture <=>) compiled.
Entity <rnda_alu> compiled.	Compiling vhdl file "icpu_datapath_functions.vhd" in Library work.
Entity <rnda_alu? (Architecture <ideal>) compiled.	Package <cpu_datapath_functions> compiled.
Compiling vhdl file "branch_ctrl_functions.vhd" in Library work.	Compiling vhdl file "req. file.vhd" in Library work.
Package <branch_ctrl_functions> compiled.	Entity <req. file> compiled.
Package body <branch_ctrl_functions> compiled.	Entity <req. file? (Architecture <=>) compiled.
Compiling vhdl file "req. file.vhd" in Library work.	Compiling vhdl file "rnda_alu_cia.vhd" in Library work.
Entity <rnda_alu> compiled.	Entity <rnda_alu> compiled.
Entity <rnda_alu? (Architecture <ideal>) compiled.	Entity <rnda_alu? (Architecture <=>) compiled.
Compiling vhdl file "icpu_functions.vhd" in Library work.	Compiling vhdl file "icpu_functions.vhd" in Library work.
Package <cpu_functions> compiled.	Package <cpu_functions> compiled.
Compiling vhdl file "branch_ctrl.vhd" in Library work.	Compiling vhdl file "icpu_datapath.vhd" in Library work.
Entity <branch_ctrl> compiled.	Entity <cpu_datapath> compiled.
Entity <branch_ctrl? (Architecture <ideal>) compiled.	Entity <cpu_datapath? (Architecture <=>) compiled.
Compiling vhdl file "icpu_datapath.vhd" in Library work.	Compiling vhdl file "branch_ctrl.vhd" in Library work.
Entity <cpu_datapath> compiled.	Entity <branch_ctrl> compiled.
Entity <cpu_datapath? (Architecture <ideal>) compiled.	Entity <branch_ctrl? (Architecture <=>) compiled.
Compiling vhdl file "icpu.vhd" in Library work.	Compiling vhdl file "icpu.vhd" in Library work.
Entity <cpu> compiled.	Entity <cpu> compiled.
Entity <cpu? (Architecture <ideal>) compiled.	Entity <cpu> (Architecture <=>) compiled.
Compiling vhdl file "rom.vhd" in Library work.	Compiling vhdl file "rom.vhd" in Library work.
Entity <rom> compiled.	Entity <rom> compiled.
Entity <rom? (Architecture <ndp>) compiled.	Entity <rom> (Architecture <ndp>) compiled.
Compiling vhdl file "ram.vhd" in Library work.	Compiling vhdl file "ram.vhd" in Library work.
Entity <ram> compiled.	Entity <ram> compiled.

> xst -fh cpu.xst	> xst -fh cpu.xst
Release 14.7 - xst P 20131013 (m64)	Release 14.7 - xst P 20131013 (m64)
Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.	Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.
-> Parameter TMPDIR set to /xstprojdir/tmp	-> Parameter TMPDIR set to /xstprojdir/tmp
Total REAL time to Xst completion: 0.00 secs	Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.23 secs	Total CPU time to Xst completion: 0.23 secs
-> WARNING:Xst-3164 - Option "-debug" found multiple times in the command line. Only the first occurrence is considered.	-> WARNING:Xst-3164 - Option "-debug" found multiple times in the command line. Only the first occurrence is considered.
* HDL Compilation	* HDL Compilation
Compiling vhdl file "muxent01.vhd" in Library work.	Compiling vhdl file "muxent01.vhd" in Library work.
Entity <muxent01> compiled.	Entity <muxent01> compiled.
Entity <muxent01> (Architecture <ideab1>) compiled.	Entity <muxent01> (Architecture <=>) compiled.
Compiling vhdl file "dff.vhd" in Library work.	Compiling vhdl file "dff.vhd" in Library work.
Entity <dff> compiled.	Entity <dff> compiled.
Entity <dff> (Architecture <ideab1>) compiled.	Entity <dff> (Architecture <=>) compiled.
Compiling vhdl file "cila_gp.vhd" in Library work.	Compiling vhdl file "cila_gp.vhd" in Library work.
Entity <cila_gp> compiled.	Entity <cila_gp> compiled.
Entity <cila_gp> (Architecture <ideab1>) compiled.	Entity <cila_gp> (Architecture <=>) compiled.
Compiling vhdl file "muxdff.vhd" in Library work.	Compiling vhdl file "muxdff.vhd" in Library work.
Entity <muxdff> compiled.	Entity <muxdff> compiled.
Entity <muxdff> (Architecture <ideab1>) compiled.	Entity <muxdff> (Architecture <=>) compiled.
Compiling vhdl file "req_file_functions.vhd" in Library work.	Compiling vhdl file "req_file_functions.vhd" in Library work.
Package <req_file_functions> compiled.	Package <req_file_functions> compiled.
Package body <req_file_functions> compiled.	Package body <req_file_functions> compiled.
Compiling vhdl file "cila_add_n_bit.vhd" in Library work.	Compiling vhdl file "cila_add_n_bit.vhd" in Library work.
Entity <cila_add_n_bit> compiled.	Entity <cila_add_n_bit> compiled.
Entity <cila_add_n_bit> (Architecture <ideab1>) compiled.	Entity <cila_add_n_bit> (Architecture <=>) compiled.
Compiling vhdl file "dmuxent01.vhd" in Library work.	Compiling vhdl file "dmuxent01.vhd" in Library work.
Entity <dmuxent01> compiled.	Entity <dmuxent01> compiled.
Entity <dmuxent01> (Architecture <ideab1>) compiled.	Entity <dmuxent01> (Architecture <=>) compiled.
Compiling vhdl file "muxent01_bus.vhd" in Library work.	Compiling vhdl file "muxent01_bus.vhd" in Library work.
Entity <muxent01_bus> compiled.	Entity <muxent01_bus> compiled.
Entity <muxent01_bus> (Architecture <ideab1>) compiled.	Entity <muxent01_bus> (Architecture <=>) compiled.
Compiling vhdl file "shift_req.vhd" in Library work.	Compiling vhdl file "shift_req.vhd" in Library work.
Entity <shift_req> compiled.	Entity <shift_req> compiled.
Entity <shift_req> (Architecture <ideab1>) compiled.	Entity <shift_req> (Architecture <=>) compiled.
Compiling vhdl file "icpu_datapath_functions.vhd" in Library work.	Compiling vhdl file "branch_ctrl_functions.vhd" in Library work.
Package <cpu_datapath_functions> compiled.	Package <branch_ctrl_functions> compiled.
Compiling vhdl file "req_file.vhd" in Library work.	Package body <branch_ctrl_functions> compiled.
Entity <req_file> compiled.	Compiling vhdl file "counter.vhd" in Library work.
Entity <req_file> (Architecture <ideab1>) compiled.	Entity <counter> compiled.
Compiling vhdl file "rdrn_alu_cila.vhd" in Library work.	Entity <counter> (Architecture <=>) compiled.
Entity <rdrn_alu> compiled.	Compiling vhdl file "icpu_datapath_functions.vhd" in Library work.
Entity <rdrn_alu> (Architecture <ideab1>) compiled.	Package <cpu_datapath_functions> compiled.
Compiling vhdl file "branch_ctrl_functions.vhd" in Library work.	Compiling vhdl file "req_file.vhd" in Library work.
Package <branch_ctrl_functions> compiled.	Entity <req_file> compiled.
Package body <branch_ctrl_functions> compiled.	Entity <req_file> (Architecture <=>) compiled.
Compiling vhdl file "counter.vhd" in Library work.	Compiling vhdl file "rdrn_alu_cila.vhd" in Library work.
Entity <counter> compiled.	Entity <rdrn_alu> compiled.
Entity <counter> (Architecture <ideab1>) compiled.	Entity <rdrn_alu> (Architecture <=>) compiled.
Compiling vhdl file "icpu_functions.vhd" in Library work.	Compiling vhdl file "icpu_functions.vhd" in Library work.
Package <cpu_functions> compiled.	Package <cpu_functions> compiled.
Compiling vhdl file "branch_ctrl.vhd" in Library work.	Compiling vhdl file "icpu_datapath.vhd" in Library work.
Entity <branch_ctrl> compiled.	Entity <cpu_datapath> compiled.
Entity <branch_ctrl> (Architecture <ideab1>) compiled.	Entity <cpu_datapath> (Architecture <=>) compiled.
Compiling vhdl file "icpu_datapath.vhd" in Library work.	Compiling vhdl file "branch_ctrl.vhd" in Library work.
Entity <cpu_datapath> compiled.	Entity <branch_ctrl> compiled.
Entity <cpu_datapath> (Architecture <ideab1>) compiled.	Entity <branch_ctrl> (Architecture <=>) compiled.
Compiling vhdl file "icpu.vhd" in Library work.	Compiling vhdl file "icpu.vhd" in Library work.
Entity <cpu> compiled.	Entity <cpu> compiled.
Entity <cpu> (Architecture <ideab1>) compiled.	Entity <cpu> (Architecture <=>) compiled.
Compiling vhdl file "rom.vhd" in Library work.	Compiling vhdl file "rom.vhd" in Library work.
Entity <rom> compiled.	Entity <rom> compiled.
Entity <rom> (Architecture <ndp>) compiled.	Entity <rom> (Architecture <ndp>) compiled.
Compiling vhdl file "iram.vhd" in Library work.	Compiling vhdl file "iram.vhd" in Library work.
Entity <iram> compiled.	Entity <iram> compiled.

>xst -fh cpu_xst	>xst -fh cpu_xst
Release 14.7 - xst P 20131013 (m64)	Release 14.7 - xst P 20131013 (m64)
Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.	Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.
--> Parameter TMPDIR set to /xstprograw/tmp	--> Parameter TMPDIR set to /xstprograw/tmp
Total REAL time to Xst completion: 0.00 secs	Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.23 secs	Total CPU time to Xst completion: 0.24 secs
--> WARNING:Xst-3164 - Option "-debug" found multiple times in the command line. Only the first occurrence is considered.	--> WARNING:Xst-3164 - Option "-debug" found multiple times in the command line. Only the first occurrence is considered.
* HDL Compilation *	* HDL Compilation *
Compiling vhdl file "muxent01.vhd" in Library work.	Compiling vhdl file "muxent01.vhd" in Library work.
Entity <muxent01> compiled.	Entity <muxent01> compiled.
Entity <muxent01> (Architecture <ideab1>) compiled.	Entity <muxent01> (Architecture <=>) compiled.
Compiling vhdl file "dff.vhd" in Library work.	Compiling vhdl file "dff.vhd" in Library work.
Entity <dff> compiled.	Entity <dff> compiled.
Entity <dff> (Architecture <ideab1>) compiled.	Entity <dff> (Architecture <=>) compiled.
Compiling vhdl file "cda_ap.vhd" in Library work.	Compiling vhdl file "cda_ap.vhd" in Library work.
Entity <cda_ap> compiled.	Entity <cda_ap> compiled.
Entity <cda_ap> (Architecture <ideab1>) compiled.	Entity <cda_ap> (Architecture <=>) compiled.
Compiling vhdl file "muxdff.vhd" in Library work.	Compiling vhdl file "muxdff.vhd" in Library work.
Entity <muxdff> compiled.	Entity <muxdff> compiled.
Entity <muxdff> (Architecture <ideab1>) compiled.	Entity <muxdff> (Architecture <=>) compiled.
Compiling vhdl file "req_file_functions.vhd" in Library work.	Compiling vhdl file "req_file_functions.vhd" in Library work.
Package <req_file_functions> compiled.	Package <req_file_functions> compiled.
Package body <req_file_functions> compiled.	Package body <req_file_functions> compiled.
Compiling vhdl file "cda_add_n_bit.vhd" in Library work.	Compiling vhdl file "cda_add_n_bit.vhd" in Library work.
Entity <cda_add_n_bit> compiled.	Entity <cda_add_n_bit> compiled.
Entity <cda_add_n_bit> (Architecture <ideab1>) compiled.	Entity <cda_add_n_bit> (Architecture <=>) compiled.
Compiling vhdl file "dmuxent01.vhd" in Library work.	Compiling vhdl file "dmuxent01.vhd" in Library work.
Entity <dmuxent01> compiled.	Entity <dmuxent01> compiled.
Entity <dmuxent01> (Architecture <ideab1>) compiled.	Entity <dmuxent01> (Architecture <=>) compiled.
Compiling vhdl file "muxent01_bus.vhd" in Library work.	Compiling vhdl file "muxent01_bus.vhd" in Library work.
Entity <muxent01_bus> compiled.	Entity <muxent01_bus> compiled.
Entity <muxent01_bus> (Architecture <ideab1>) compiled.	Entity <muxent01_bus> (Architecture <=>) compiled.
Compiling vhdl file "shift_req.vhd" in Library work.	Compiling vhdl file "shift_req.vhd" in Library work.
Entity <shift_req> compiled.	Entity <shift_req> compiled.
Entity <shift_req> (Architecture <ideab1>) compiled.	Entity <shift_req> (Architecture <=>) compiled.
Compiling vhdl file "rcpu_datapath_functions.vhd" in Library work.	Compiling vhdl file "branch_ctrl_functions.vhd" in Library work.
Package <cpu_datapath_functions> compiled.	Package <branch_ctrl_functions> compiled.
Compiling vhdl file "req_file.vhd" in Library work.	Package body <branch_ctrl_functions> compiled.
Entity <req_file> compiled.	Compiling vhdl file "counter.vhd" in Library work.
Entity <req_file> (Architecture <ideab1>) compiled.	Entity <counter> compiled.
Compiling vhdl file "rnda_alu_cda.vhd" in Library work.	Entity <counter> (Architecture <=>) compiled.
Entity <rnda_alu_cda> compiled.	Compiling vhdl file "rcpu_datapath_functions.vhd" in Library work.
Entity <rnda_alu_cda> (Architecture <ideab1>) compiled.	Package <cpu_datapath_functions> compiled.
Compiling vhdl file "branch_ctrl_functions.vhd" in Library work.	Compiling vhdl file "req_file.vhd" in Library work.
Package <branch_ctrl_functions> compiled.	Entity <req_file> compiled.
Package body <branch_ctrl_functions> compiled.	Entity <req_file> (Architecture <=>) compiled.
Compiling vhdl file "counter.vhd" in Library work.	Compiling vhdl file "rnda_alu_cda.vhd" in Library work.
Entity <counter> compiled.	Entity <rnda_alu_cda> compiled.
Entity <counter> (Architecture <ideab1>) compiled.	Entity <rnda_alu_cda> (Architecture <=>) compiled.
Compiling vhdl file "rcpu_functions.vhd" in Library work.	Compiling vhdl file "rcpu_functions.vhd" in Library work.
Package <cpu_functions> compiled.	Package <cpu_functions> compiled.
Compiling vhdl file "branch_ctrl.vhd" in Library work.	Compiling vhdl file "rcpu_datapath.vhd" in Library work.
Entity <branch_ctrl> compiled.	Entity <rcpu_datapath> compiled.
Entity <branch_ctrl> (Architecture <ideab1>) compiled.	Entity <rcpu_datapath> (Architecture <=>) compiled.
Compiling vhdl file "rcpu_datapath.vhd" in Library work.	Compiling vhdl file "branch_ctrl.vhd" in Library work.
Entity <rcpu_datapath> compiled.	Entity <branch_ctrl> compiled.
Entity <rcpu_datapath> (Architecture <ideab1>) compiled.	Entity <branch_ctrl> (Architecture <=>) compiled.
Compiling vhdl file "rcpu.vhd" in Library work.	Compiling vhdl file "rcpu.vhd" in Library work.
Entity <rcpu> compiled.	Entity <rcpu> compiled.
Entity <rcpu> (Architecture <ideab1>) compiled.	Entity <rcpu> (Architecture <=>) compiled.
Compiling vhdl file "rom.vhd" in Library work.	Compiling vhdl file "rom.vhd" in Library work.
Entity <rom> compiled.	Entity <rom> compiled.
Entity <rom> (Architecture <ndp>) compiled.	Entity <rom> (Architecture <ndp>) compiled.
Compiling vhdl file "ram.vhd" in Library work.	Compiling vhdl file "ram.vhd" in Library work.
Entity <ram> compiled.	Entity <ram> compiled.

> xst -th cpu.xst	> xst -th cpu.xst
Release 14.7 - xst P.20131013 (n64)	Release 14.7 - xst P.20131013 (n64)
Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.	Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.
-> Parameter TMPDIR set to /xst/procnav.tmp	-> Parameter TMPDIR set to /xst/procnav.tmp
Total REAL time to Xst completion: 0.00 secs	Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.23 secs	Total CPU time to Xst completion: 0.24 secs
-> WARNING:Xst:3164 - Option "-debug" found multiple times in the command line. Only the first occurrence is considered.	-> WARNING:Xst:3164 - Option "-debug" found multiple times in the command line. Only the first occurrence is considered.
* HDL Compilation *	* HDL Compilation *
Compiling vhdl file "muxent01.vhd" in Library work.	Compiling vhdl file "muxent01.vhd" in Library work.
Entity <muxent01> compiled.	Entity <muxent01> compiled.
Entity <muxent01> (Architecture <ideal>) compiled.	Entity <muxent01> (Architecture <=>) compiled.
Compiling vhdl file "dff.vhd" in Library work.	Compiling vhdl file "dff.vhd" in Library work.
Entity <dff> compiled.	Entity <dff> compiled.
Entity <dff> (Architecture <ideal>) compiled.	Entity <dff> (Architecture <=>) compiled.
Compiling vhdl file "cda_gp.vhd" in Library work.	Compiling vhdl file "cda_gp.vhd" in Library work.
Entity <cda_gp> compiled.	Entity <cda_gp> compiled.
Entity <cda_gp> (Architecture <ideal>) compiled.	Entity <cda_gp> (Architecture <=>) compiled.
Compiling vhdl file "muxdff.vhd" in Library work.	Compiling vhdl file "muxdff.vhd" in Library work.
Entity <muxdff> compiled.	Entity <muxdff> compiled.
Entity <muxdff> (Architecture <ideal>) compiled.	Entity <muxdff> (Architecture <=>) compiled.
Compiling vhdl file "req. file functions.vhd" in Library work.	Compiling vhdl file "req. file functions.vhd" in Library work.
Package <req. file functions> compiled.	Package <req. file functions> compiled.
Package body <req. file functions> compiled.	Package body <req. file functions> compiled.
Compiling vhdl file "cda_add_n_bit.vhd" in Library work.	Compiling vhdl file "cda_add_n_bit.vhd" in Library work.
Entity <cda_add_n_bit> compiled.	Entity <cda_add_n_bit> compiled.
Entity <cda_add_n_bit> (Architecture <ideal>) compiled.	Entity <cda_add_n_bit> (Architecture <=>) compiled.
Compiling vhdl file "dmuxent01.vhd" in Library work.	Compiling vhdl file "dmuxent01.vhd" in Library work.
Entity <dmuxent01> compiled.	Entity <dmuxent01> compiled.
Entity <dmuxent01> (Architecture <ideal>) compiled.	Entity <dmuxent01> (Architecture <=>) compiled.
Compiling vhdl file "muxent01_bus.vhd" in Library work.	Compiling vhdl file "muxent01_bus.vhd" in Library work.
Entity <muxent01_bus> compiled.	Entity <muxent01_bus> compiled.
Entity <muxent01_bus> (Architecture <ideal>) compiled.	Entity <muxent01_bus> (Architecture <=>) compiled.
Compiling vhdl file "shift_req.vhd" in Library work.	Compiling vhdl file "shift_req.vhd" in Library work.
Entity <shift_req> compiled.	Entity <shift_req> compiled.
Entity <shift_req> (Architecture <ideal>) compiled.	Entity <shift_req> (Architecture <=>) compiled.
Compiling vhdl file "rcpu_datapath_functions.vhd" in Library work.	Compiling vhdl file "branch_ctrl_functions.vhd" in Library work.
Package <cpu_datapath_functions> compiled.	Package <branch_ctrl_functions> compiled.
Compiling vhdl file "req. file.vhd" in Library work.	Package body <branch_ctrl_functions> compiled.
Entity <req. file> compiled.	Compiling vhdl file "counter.vhd" in Library work.
Entity <req. file> (Architecture <ideal>) compiled.	Entity <counter> compiled.
Compiling vhdl file "rnda_alu_cda.vhd" in Library work.	Entity <counter> (Architecture <=>) compiled.
Entity <rnda_alu> compiled.	Compiling vhdl file "rcpu_datapath_functions.vhd" in Library work.
Entity <rnda_alu> (Architecture <ideal>) compiled.	Package <cpu_datapath_functions> compiled.
Compiling vhdl file "branch_ctrl_functions.vhd" in Library work.	Compiling vhdl file "req. file.vhd" in Library work.
Package <branch_ctrl_functions> compiled.	Entity <req. file> compiled.
Package body <branch_ctrl_functions> compiled.	Entity <req. file> (Architecture <=>) compiled.
Compiling vhdl file "rcpu_functions.vhd" in Library work.	Compiling vhdl file "rnda_alu_cda.vhd" in Library work.
Entity <rcpu_functions> compiled.	Entity <rnda_alu_cda> compiled.
Entity <rcpu_functions> (Architecture <ideal>) compiled.	Entity <rnda_alu_cda> (Architecture <=>) compiled.
Compiling vhdl file "branch_ctrl.vhd" in Library work.	Compiling vhdl file "rcpu_functions.vhd" in Library work.
Entity <branch_ctrl> compiled.	Package <cpu_functions> compiled.
Entity <branch_ctrl> (Architecture <ideal>) compiled.	Compiling vhdl file "rcpu_datapath.vhd" in Library work.
Compiling vhdl file "rcpu_datapath.vhd" in Library work.	Entity <rcpu_datapath> compiled.
Entity <cpu_datapath> compiled.	Entity <rcpu_datapath> (Architecture <=>) compiled.
Entity <cpu_datapath> (Architecture <ideal>) compiled.	Compiling vhdl file "branch_ctrl.vhd" in Library work.
Compiling vhdl file "rcpu.vhd" in Library work.	Entity <branch_ctrl> compiled.
Entity <rcpu> compiled.	Entity <branch_ctrl> (Architecture <=>) compiled.
Entity <rcpu> (Architecture <ideal>) compiled.	Compiling vhdl file "rcpu.vhd" in Library work.
Compiling vhdl file "rom.vhd" in Library work.	Entity <rcpu> compiled.
Entity <rom> compiled.	Entity <rcpu> (Architecture <=>) compiled.
Entity <rom> (Architecture <ndyn>) compiled.	Compiling vhdl file "rom.vhd" in Library work.
Compiling vhdl file "ram.vhd" in Library work.	Entity <rom> compiled.
Entity <ram> compiled.	Entity <rom> (Architecture <ndyn>) compiled.
	Compiling vhdl file "ram.vhd" in Library work.
	Entity <ram> compiled.

>set -fH cpu.xst	>set -fH cpu.xst
Release 14.7 - xst P.20131013 (n64)	Release 14.7 - xst P.20131013 (n64)
Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.	Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.
-> Parameter TMPDIR set to /xstprojdir/tmp	-> Parameter TMPDIR set to /xstprojdir/tmp
Total REAL time to Xst completion: 0.00 secs	Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.22 secs	Total CPU time to Xst completion: 0.24 secs
-> WARNING:Xst:3164 - Option "-debug" found multiple times in the command line. Only the first occurrence is considered.	-> WARNING:Xst:3164 - Option "-debug" found multiple times in the command line. Only the first occurrence is considered.
* HDL Compilation *	* HDL Compilation *
Compiling vhdl file "muxnto1.vhd" in Library work.	Compiling vhdl file "muxnto1.vhd" in Library work.
Entity <muxnto1> compiled.	Entity <muxnto1> compiled.
Entity <muxnto1> (Architecture <ideab>) compiled.	Entity <muxnto1> (Architecture <=>) compiled.
Compiling vhdl file "dff.vhd" in Library work.	Compiling vhdl file "dff.vhd" in Library work.
Entity <dff> compiled.	Entity <dff> compiled.
Entity <dff> (Architecture <ideab>) compiled.	Entity <dff> (Architecture <=>) compiled.
Compiling vhdl file "cda_gp.vhd" in Library work.	Compiling vhdl file "cda_gp.vhd" in Library work.
Entity <cda_gp> compiled.	Entity <cda_gp> compiled.
Entity <cda_gp> (Architecture <ideab>) compiled.	Entity <cda_gp> (Architecture <=>) compiled.
Compiling vhdl file "muxdff.vhd" in Library work.	Compiling vhdl file "muxdff.vhd" in Library work.
Entity <muxdff> compiled.	Entity <muxdff> compiled.
Entity <muxdff> (Architecture <ideab>) compiled.	Entity <muxdff> (Architecture <=>) compiled.
Compiling vhdl file "reg_file_functions.vhd" in Library work.	Compiling vhdl file "reg_file_functions.vhd" in Library work.
Package <reg_file_functions> compiled.	Package <reg_file_functions> compiled.
Package body <reg_file_functions> compiled.	Package body <reg_file_functions> compiled.
Compiling vhdl file "cda_add_n_bit.vhd" in Library work.	Compiling vhdl file "cda_add_n_bit.vhd" in Library work.
Entity <cda_add_n_bit> compiled.	Entity <cda_add_n_bit> compiled.
Entity <cda_add_n_bit> (Architecture <ideab>) compiled.	Entity <cda_add_n_bit> (Architecture <=>) compiled.
Compiling vhdl file "dmuxnto1.vhd" in Library work.	Compiling vhdl file "dmuxnto1.vhd" in Library work.
Entity <dmuxnto1> compiled.	Entity <dmuxnto1> compiled.
Entity <dmuxnto1> (Architecture <ideab>) compiled.	Entity <dmuxnto1> (Architecture <=>) compiled.
Compiling vhdl file "muxnto1_bus.vhd" in Library work.	Compiling vhdl file "muxnto1_bus.vhd" in Library work.
Entity <muxnto1_bus> compiled.	Entity <muxnto1_bus> compiled.
Entity <muxnto1_bus> (Architecture <ideab>) compiled.	Entity <muxnto1_bus> (Architecture <=>) compiled.
Compiling vhdl file "shift_reg.vhd" in Library work.	Compiling vhdl file "shift_reg.vhd" in Library work.
Entity <shift_reg> compiled.	Entity <shift_reg> compiled.
Entity <shift_reg> (Architecture <ideab>) compiled.	Entity <shift_reg> (Architecture <=>) compiled.
Compiling vhdl file "branch_ctrl_functions.vhd" in Library work.	Compiling vhdl file "branch_ctrl_functions.vhd" in Library work.
Package <branch_ctrl_functions> compiled.	Package <branch_ctrl_functions> compiled.
Package body <branch_ctrl_functions> compiled.	Package body <branch_ctrl_functions> compiled.
Compiling vhdl file "counter.vhd" in Library work.	Compiling vhdl file "counter.vhd" in Library work.
Entity <counter> compiled.	Entity <counter> compiled.
Entity <counter> (Architecture <ideab>) compiled.	Entity <counter> (Architecture <=>) compiled.
Compiling vhdl file "cpu_datapath_functions.vhd" in Library work.	Compiling vhdl file "cpu_datapath_functions.vhd" in Library work.
Package <cpu_datapath_functions> compiled.	Package <cpu_datapath_functions> compiled.
Compiling vhdl file "reg_file.vhd" in Library work.	Compiling vhdl file "reg_file.vhd" in Library work.
Entity <reg_file> compiled.	Entity <reg_file> compiled.
Entity <reg_file> (Architecture <ideab>) compiled.	Entity <reg_file> (Architecture <=>) compiled.
Compiling vhdl file "ndn_alu_cda.vhd" in Library work.	Compiling vhdl file "ndn_alu_cda.vhd" in Library work.
Entity <ndn_alu_cda> compiled.	Entity <ndn_alu_cda> compiled.
Entity <ndn_alu_cda> (Architecture <ideab>) compiled.	Entity <ndn_alu_cda> (Architecture <=>) compiled.
Compiling vhdl file "cpu_functions.vhd" in Library work.	Compiling vhdl file "cpu_functions.vhd" in Library work.
Package <cpu_functions> compiled.	Package <cpu_functions> compiled.
Compiling vhdl file "cpu_datapath.vhd" in Library work.	Compiling vhdl file "cpu_datapath.vhd" in Library work.
Entity <cpu_datapath> compiled.	Entity <cpu_datapath> compiled.
Entity <cpu_datapath> (Architecture <ideab>) compiled.	Entity <cpu_datapath> (Architecture <=>) compiled.
Compiling vhdl file "branch_ctrl.vhd" in Library work.	Compiling vhdl file "branch_ctrl.vhd" in Library work.
Entity <branch_ctrl> compiled.	Entity <branch_ctrl> compiled.
Entity <branch_ctrl> (Architecture <ideab>) compiled.	Entity <branch_ctrl> (Architecture <=>) compiled.
Compiling vhdl file "cpu.vhd" in Library work.	Compiling vhdl file "cpu.vhd" in Library work.
Entity <cpu> compiled.	Entity <cpu> compiled.
Entity <cpu> (Architecture <ideab>) compiled.	Entity <cpu> (Architecture <=>) compiled.
Compiling vhdl file "rom.vhd" in Library work.	Compiling vhdl file "rom.vhd" in Library work.
Entity <rom> compiled.	Entity <rom> compiled.
Entity <rom> (Architecture <ndp>) compiled.	Entity <rom> (Architecture <ndp>) compiled.
Compiling vhdl file "ram.vhd" in Library work.	Compiling vhdl file "ram.vhd" in Library work.
Entity <ram> compiled.	Entity <ram> compiled.

>xst -fh cpu.xst	>xst -fh cpu.xst
Release 14.7 - xst P 20131013 (m64)	Release 14.7 - xst P 20131013 (m64)
Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.	Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.
-> Parameter TMPDIR set to ./xstpropav.tmp	-> Parameter TMPDIR set to ./xstpropav.tmp
Total REAL time to Xst completion: 0.00 secs	Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.23 secs	Total CPU time to Xst completion: 0.24 secs
-> WARNING:Xst-3164 - Option "-debug" found multiple times in the command line. Only the first occurrence is considered.	-> WARNING:Xst-3164 - Option "-debug" found multiple times in the command line. Only the first occurrence is considered.
* HDL Compilation *	* HDL Compilation *
Compiling vhdl file "muxnto1.vhd" in Library work.	Compiling vhdl file "muxnto1.vhd" in Library work.
Entity <muxnto1> compiled.	Entity <muxnto1> compiled.
Entity <muxnto1> (Architecture <ideal>) compiled.	Entity <muxnto1> (Architecture <= >) compiled.
Compiling vhdl file "dff.vhd" in Library work.	Compiling vhdl file "dff.vhd" in Library work.
Entity <dff> compiled.	Entity <dff> compiled.
Entity <dff> (Architecture <ideal>) compiled.	Entity <dff> (Architecture <= >) compiled.
Compiling vhdl file "cila_gp.vhd" in Library work.	Compiling vhdl file "cila_gp.vhd" in Library work.
Entity <cila_gp> compiled.	Entity <cila_gp> compiled.
Entity <cila_gp> (Architecture <ideal>) compiled.	Entity <cila_gp> (Architecture <= >) compiled.
Compiling vhdl file "muxdff.vhd" in Library work.	Compiling vhdl file "muxdff.vhd" in Library work.
Entity <muxdff> compiled.	Entity <muxdff> compiled.
Entity <muxdff> (Architecture <ideal>) compiled.	Entity <muxdff> (Architecture <= >) compiled.
Compiling vhdl file "req_file_functions.vhd" in Library work.	Compiling vhdl file "req_file_functions.vhd" in Library work.
Package <req_file_functions> compiled.	Package <req_file_functions> compiled.
Package body <req_file_functions> compiled.	Package body <req_file_functions> compiled.
Compiling vhdl file "cila_add_n_bit.vhd" in Library work.	Compiling vhdl file "cila_add_n_bit.vhd" in Library work.
Entity <cila_add_n_bit> compiled.	Entity <cila_add_n_bit> compiled.
Entity <cila_add_n_bit> (Architecture <ideal>) compiled.	Entity <cila_add_n_bit> (Architecture <= >) compiled.
Compiling vhdl file "dmuxnto1.vhd" in Library work.	Compiling vhdl file "dmuxnto1.vhd" in Library work.
Entity <dmuxnto1> compiled.	Entity <dmuxnto1> compiled.
Entity <dmuxnto1> (Architecture <ideal>) compiled.	Entity <dmuxnto1> (Architecture <= >) compiled.
Compiling vhdl file "muxnto1_bus.vhd" in Library work.	Compiling vhdl file "muxnto1_bus.vhd" in Library work.
Entity <muxnto1_bus> compiled.	Entity <muxnto1_bus> compiled.
Entity <muxnto1_bus> (Architecture <ideal>) compiled.	Entity <muxnto1_bus> (Architecture <= >) compiled.
Compiling vhdl file "shift_req.vhd" in Library work.	Compiling vhdl file "shift_req.vhd" in Library work.
Entity <shift_req> compiled.	Entity <shift_req> compiled.
Entity <shift_req> (Architecture <ideal>) compiled.	Entity <shift_req> (Architecture <= >) compiled.
Compiling vhdl file "rcpu_datapath_functions.vhd" in Library work.	Compiling vhdl file "branch_ctrl_functions.vhd" in Library work.
Package <cpu_datapath_functions> compiled.	Package <branch_ctrl_functions> compiled.
Compiling vhdl file "req_file.vhd" in Library work.	Package body <branch_ctrl_functions> compiled.
Entity <req_file> compiled.	Compiling vhdl file "counter.vhd" in Library work.
Entity <req_file> (Architecture <ideal>) compiled.	Entity <counter> compiled.
Compiling vhdl file "rnda_alu_cila.vhd" in Library work.	Entity <counter> (Architecture <= >) compiled.
Entity <rnda_alu> compiled.	Compiling vhdl file "rcpu_datapath_functions.vhd" in Library work.
Entity <rnda_alu> (Architecture <ideal>) compiled.	Package <cpu_datapath_functions> compiled.
Compiling vhdl file "branch_ctrl_functions.vhd" in Library work.	Compiling vhdl file "req_file.vhd" in Library work.
Package <branch_ctrl_functions> compiled.	Entity <req_file> compiled.
Package body <branch_ctrl_functions> compiled.	Entity <req_file> (Architecture <= >) compiled.
Compiling vhdl file "counter.vhd" in Library work.	Compiling vhdl file "rnda_alu_cila.vhd" in Library work.
Entity <counter> compiled.	Entity <rnda_alu> compiled.
Entity <counter> (Architecture <ideal>) compiled.	Entity <rnda_alu> (Architecture <= >) compiled.
Compiling vhdl file "rcpu_functions.vhd" in Library work.	Compiling vhdl file "rcpu_functions.vhd" in Library work.
Package <cpu_functions> compiled.	Package <cpu_functions> compiled.
Compiling vhdl file "branch_ctrl.vhd" in Library work.	Compiling vhdl file "rcpu_datapath.vhd" in Library work.
Entity <branch_ctrl> compiled.	Entity <cpu_datapath> compiled.
Entity <branch_ctrl> (Architecture <ideal>) compiled.	Entity <cpu_datapath> (Architecture <= >) compiled.
Compiling vhdl file "rcpu_datapath.vhd" in Library work.	Compiling vhdl file "branch_ctrl.vhd" in Library work.
Entity <cpu_datapath> compiled.	Entity <branch_ctrl> compiled.
Entity <cpu_datapath> (Architecture <ideal>) compiled.	Entity <branch_ctrl> (Architecture <= >) compiled.
Compiling vhdl file "rcpu.vhd" in Library work.	Compiling vhdl file "rcpu.vhd" in Library work.
Entity <rcpu> compiled.	Entity <rcpu> compiled.
Entity <rcpu> (Architecture <ideal>) compiled.	Entity <rcpu> (Architecture <= >) compiled.
Compiling vhdl file "rom.vhd" in Library work.	Compiling vhdl file "rom.vhd" in Library work.
Entity <rom> compiled.	Entity <rom> compiled.
Entity <rom> (Architecture <ideal>) compiled.	Entity <rom> (Architecture <= >) compiled.
Compiling vhdl file "sram.vhd" in Library work.	Compiling vhdl file "sram.vhd" in Library work.
Entity <sram> compiled.	Entity <sram> compiled.

>xst -fh cpu.xst	>xst -fh cpu.xst
Release 14.7 - xst P.20131013 (m64)	Release 14.7 - xst P.20131013 (m64)
Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.	Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.
-> Parameter TMPDIR set to ./xstprojdir/tmp	-> Parameter TMPDIR set to ./xstprojdir/tmp
Total REAL time to Xst completion: 0.00 secs	Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.23 secs	Total CPU time to Xst completion: 0.24 secs
-> WARNING:Xst-3164 - Option "-debug" found multiple times in the command line. Only the first occurrence is considered.	-> WARNING:Xst-3164 - Option "-debug" found multiple times in the command line. Only the first occurrence is considered.
* HDL Compilation	* HDL Compilation
Compiling vhdl file "muxent01.vhd" in Library work.	Compiling vhdl file "muxent01.vhd" in Library work.
Entity <muxent01> compiled.	Entity <muxent01> compiled.
Entity <muxent01> (Architecture <ideal>) compiled.	Entity <muxent01> (Architecture <=) compiled.
Compiling vhdl file "dff.vhd" in Library work.	Compiling vhdl file "dff.vhd" in Library work.
Entity <dff> compiled.	Entity <dff> compiled.
Entity <dff> (Architecture <ideal>) compiled.	Entity <dff> (Architecture <=) compiled.
Compiling vhdl file "cda_gp.vhd" in Library work.	Compiling vhdl file "cda_gp.vhd" in Library work.
Entity <cda_gp> compiled.	Entity <cda_gp> compiled.
Entity <cda_gp> (Architecture <ideal>) compiled.	Entity <cda_gp> (Architecture <=) compiled.
Compiling vhdl file "muxdff.vhd" in Library work.	Compiling vhdl file "muxdff.vhd" in Library work.
Entity <muxdff> compiled.	Entity <muxdff> compiled.
Entity <muxdff> (Architecture <ideal>) compiled.	Entity <muxdff> (Architecture <=) compiled.
Compiling vhdl file "req_file_functions.vhd" in Library work.	Compiling vhdl file "req_file_functions.vhd" in Library work.
Package <req_file_functions> compiled.	Package <req_file_functions> compiled.
Package body <req_file_functions> compiled.	Package body <req_file_functions> compiled.
Compiling vhdl file "cda_add_n_bit.vhd" in Library work.	Compiling vhdl file "cda_add_n_bit.vhd" in Library work.
Entity <cda_add_n_bit> compiled.	Entity <cda_add_n_bit> compiled.
Entity <cda_add_n_bit> (Architecture <ideal>) compiled.	Entity <cda_add_n_bit> (Architecture <=) compiled.
Compiling vhdl file "dmuxent01.vhd" in Library work.	Compiling vhdl file "dmuxent01.vhd" in Library work.
Entity <dmuxent01> compiled.	Entity <dmuxent01> compiled.
Entity <dmuxent01> (Architecture <ideal>) compiled.	Entity <dmuxent01> (Architecture <=) compiled.
Compiling vhdl file "muxent01_bus.vhd" in Library work.	Compiling vhdl file "muxent01_bus.vhd" in Library work.
Entity <muxent01_bus> compiled.	Entity <muxent01_bus> compiled.
Entity <muxent01_bus> (Architecture <ideal>) compiled.	Entity <muxent01_bus> (Architecture <=) compiled.
Compiling vhdl file "shift_req.vhd" in Library work.	Compiling vhdl file "shift_req.vhd" in Library work.
Entity <shift_req> compiled.	Entity <shift_req> compiled.
Entity <shift_req> (Architecture <ideal>) compiled.	Entity <shift_req> (Architecture <=) compiled.
Compiling vhdl file "cpu_datapath_functions.vhd" in Library work.	Compiling vhdl file "branch_ctrl_functions.vhd" in Library work.
Package <cpu_datapath_functions> compiled.	Package <branch_ctrl_functions> compiled.
Compiling vhdl file "req_file.vhd" in Library work.	Package body <branch_ctrl_functions> compiled.
Entity <req_file> compiled.	Compiling vhdl file "counter.vhd" in Library work.
Entity <req_file> (Architecture <ideal>) compiled.	Entity <counter> compiled.
Compiling vhdl file "rnda_alu_cda.vhd" in Library work.	Entity <counter> (Architecture <=) compiled.
Entity <rnda_alu_cda> compiled.	Compiling vhdl file "cpu_datapath_functions.vhd" in Library work.
Entity <rnda_alu_cda> (Architecture <ideal>) compiled.	Package <cpu_datapath_functions> compiled.
Compiling vhdl file "branch_ctrl_functions.vhd" in Library work.	Compiling vhdl file "req_file.vhd" in Library work.
Package <branch_ctrl_functions> compiled.	Entity <req_file> compiled.
Package body <branch_ctrl_functions> compiled.	Entity <req_file> (Architecture <=) compiled.
Compiling vhdl file "counter.vhd" in Library work.	Compiling vhdl file "rnda_alu_cda.vhd" in Library work.
Entity <counter> compiled.	Entity <rnda_alu_cda> compiled.
Entity <counter> (Architecture <ideal>) compiled.	Entity <rnda_alu_cda> (Architecture <=) compiled.
Compiling vhdl file "cpu_functions.vhd" in Library work.	Compiling vhdl file "cpu_functions.vhd" in Library work.
Package <cpu_functions> compiled.	Package <cpu_functions> compiled.
Compiling vhdl file "branch_ctrl.vhd" in Library work.	Compiling vhdl file "cpu_datapath.vhd" in Library work.
Entity <branch_ctrl> compiled.	Entity <cpu_datapath> compiled.
Entity <branch_ctrl> (Architecture <ideal>) compiled.	Entity <cpu_datapath> (Architecture <=) compiled.
Compiling vhdl file "cpu_datapath.vhd" in Library work.	Compiling vhdl file "branch_ctrl.vhd" in Library work.
Entity <cpu_datapath> compiled.	Entity <branch_ctrl> compiled.
Entity <cpu_datapath> (Architecture <ideal>) compiled.	Entity <branch_ctrl> (Architecture <=) compiled.
Compiling vhdl file "cpu.vhd" in Library work.	Compiling vhdl file "cpu.vhd" in Library work.
Entity <cpu> compiled.	Entity <cpu> compiled.
Entity <cpu> (Architecture <ideal>) compiled.	Entity <cpu> (Architecture <=) compiled.
Compiling vhdl file "rom.vhd" in Library work.	Compiling vhdl file "rom.vhd" in Library work.
Entity <rom> compiled.	Entity <rom> compiled.
Entity <rom> (Architecture <ideal>) compiled.	Entity <rom> (Architecture <=) compiled.
Compiling vhdl file "ram.vhd" in Library work.	Compiling vhdl file "ram.vhd" in Library work.
Entity <ram> compiled.	Entity <ram> compiled.

>xst -fh cpu.xst	>xst -fh cpu.xst
Release 14.7 - xst P 20131013 (m64)	Release 14.7 - xst P 20131013 (m64)
Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.	Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.
--> Parameter TMPDIR set to ./xstprojdir/tmp	--> Parameter TMPDIR set to ./xstprojdir/tmp
Total REAL time to Xst completion: 0.00 secs	Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.23 secs	Total CPU time to Xst completion: 0.24 secs
--> WARNING:Xst-3164 - Option "-debug" found multiple times in the command line. Only the first occurrence is considered.	--> WARNING:Xst-3164 - Option "-debug" found multiple times in the command line. Only the first occurrence is considered.
* HDL Compilation	* HDL Compilation
Compiling vhdl file "muxent01.vhd" in Library work.	Compiling vhdl file "muxent01.vhd" in Library work.
Entity <muxent01> compiled.	Entity <muxent01> compiled.
Entity <muxent01> (Architecture <ideal>) compiled.	Entity <muxent01> (Architecture <=) compiled.
Compiling vhdl file "dff.vhd" in Library work.	Compiling vhdl file "dff.vhd" in Library work.
Entity <dff> compiled.	Entity <dff> compiled.
Entity <dff> (Architecture <ideal>) compiled.	Entity <dff> (Architecture <=) compiled.
Compiling vhdl file "cda_gp.vhd" in Library work.	Compiling vhdl file "cda_gp.vhd" in Library work.
Entity <cda_gp> compiled.	Entity <cda_gp> compiled.
Entity <cda_gp> (Architecture <ideal>) compiled.	Entity <cda_gp> (Architecture <=) compiled.
Compiling vhdl file "muxdff.vhd" in Library work.	Compiling vhdl file "muxdff.vhd" in Library work.
Entity <muxdff> compiled.	Entity <muxdff> compiled.
Entity <muxdff> (Architecture <ideal>) compiled.	Entity <muxdff> (Architecture <=) compiled.
Compiling vhdl file "req_file_functions.vhd" in Library work.	Compiling vhdl file "req_file_functions.vhd" in Library work.
Package <req_file_functions> compiled.	Package <req_file_functions> compiled.
Package body <req_file_functions> compiled.	Package body <req_file_functions> compiled.
Compiling vhdl file "cda_add_n_bit.vhd" in Library work.	Compiling vhdl file "cda_add_n_bit.vhd" in Library work.
Entity <cda_add_n_bit> compiled.	Entity <cda_add_n_bit> compiled.
Entity <cda_add_n_bit> (Architecture <ideal>) compiled.	Entity <cda_add_n_bit> (Architecture <=) compiled.
Compiling vhdl file "dmuxent01.vhd" in Library work.	Compiling vhdl file "dmuxent01.vhd" in Library work.
Entity <dmuxent01> compiled.	Entity <dmuxent01> compiled.
Entity <dmuxent01> (Architecture <ideal>) compiled.	Entity <dmuxent01> (Architecture <=) compiled.
Compiling vhdl file "muxent01_bus.vhd" in Library work.	Compiling vhdl file "muxent01_bus.vhd" in Library work.
Entity <muxent01_bus> compiled.	Entity <muxent01_bus> compiled.
Entity <muxent01_bus> (Architecture <ideal>) compiled.	Entity <muxent01_bus> (Architecture <=) compiled.
Compiling vhdl file "shift_req.vhd" in Library work.	Compiling vhdl file "shift_req.vhd" in Library work.
Entity <shift_req> compiled.	Entity <shift_req> compiled.
Entity <shift_req> (Architecture <ideal>) compiled.	Entity <shift_req> (Architecture <=) compiled.
Compiling vhdl file "cpu_datapath_functions.vhd" in Library work.	Compiling vhdl file "branch_ctrl_functions.vhd" in Library work.
Package <cpu_datapath_functions> compiled.	Package <branch_ctrl_functions> compiled.
Compiling vhdl file "req_file.vhd" in Library work.	Package body <branch_ctrl_functions> compiled.
Entity <req_file> compiled.	Compiling vhdl file "counter.vhd" in Library work.
Entity <req_file> (Architecture <ideal>) compiled.	Entity <counter> compiled.
Compiling vhdl file "rnda_alu_cda.vhd" in Library work.	Entity <counter> (Architecture <=) compiled.
Entity <rnda_alu_cda> compiled.	Compiling vhdl file "cpu_datapath_functions.vhd" in Library work.
Entity <rnda_alu_cda> (Architecture <ideal>) compiled.	Package <cpu_datapath_functions> compiled.
Compiling vhdl file "branch_ctrl_functions.vhd" in Library work.	Compiling vhdl file "req_file.vhd" in Library work.
Package <branch_ctrl_functions> compiled.	Entity <req_file> compiled.
Package body <branch_ctrl_functions> compiled.	Entity <req_file> (Architecture <=) compiled.
Compiling vhdl file "counter.vhd" in Library work.	Compiling vhdl file "rnda_alu_cda.vhd" in Library work.
Entity <counter> compiled.	Entity <rnda_alu_cda> compiled.
Entity <counter> (Architecture <ideal>) compiled.	Entity <rnda_alu_cda> (Architecture <=) compiled.
Compiling vhdl file "cpu_functions.vhd" in Library work.	Compiling vhdl file "cpu_functions.vhd" in Library work.
Package <cpu_functions> compiled.	Package <cpu_functions> compiled.
Compiling vhdl file "branch_ctrl.vhd" in Library work.	Compiling vhdl file "cpu_datapath.vhd" in Library work.
Entity <branch_ctrl> compiled.	Entity <cpu_datapath> compiled.
Entity <branch_ctrl> (Architecture <ideal>) compiled.	Entity <cpu_datapath> (Architecture <=) compiled.
Compiling vhdl file "cpu_datapath.vhd" in Library work.	Compiling vhdl file "branch_ctrl.vhd" in Library work.
Entity <cpu_datapath> compiled.	Entity <branch_ctrl> compiled.
Entity <cpu_datapath> (Architecture <ideal>) compiled.	Entity <branch_ctrl> (Architecture <=) compiled.
Compiling vhdl file "cpu.vhd" in Library work.	Compiling vhdl file "cpu.vhd" in Library work.
Entity <cpu> compiled.	Entity <cpu> compiled.
Entity <cpu> (Architecture <ideal>) compiled.	Entity <cpu> (Architecture <=) compiled.
Compiling vhdl file "rom.vhd" in Library work.	Compiling vhdl file "rom.vhd" in Library work.
Entity <rom> compiled.	Entity <rom> compiled.
Entity <rom> (Architecture <ideal>) compiled.	Entity <rom> (Architecture <=) compiled.
Compiling vhdl file "sram.vhd" in Library work.	Compiling vhdl file "sram.vhd" in Library work.
Entity <sram> compiled.	Entity <sram> compiled.

>xst -fh cpu.xst	>xst -fh cpu.xst
Release 14.7 - xst P.20131013 (n64)	Release 14.7 - xst P.20131013 (n64)
Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.	Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.
-> Parameter TMPDIR set to /xst/propag.tmp	-> Parameter TMPDIR set to /xst/propag.tmp
Total REAL time to Xst completion: 0.00 secs	Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.23 secs	Total CPU time to Xst completion: 0.24 secs
-> WARNING:Xst:3164 - Option "-debug" found multiple times in the command line. Only the first occurrence is considered.	-> WARNING:Xst:3164 - Option "-debug" found multiple times in the command line. Only the first occurrence is considered.
* HDL Compilation *	* HDL Compilation *
Compiling vhdl file "muxent01.vhd" in Library work.	Compiling vhdl file "muxent01.vhd" in Library work.
Entity <muxent01> compiled.	Entity <muxent01> compiled.
Entity <muxent01> (Architecture <ideal>) compiled.	Entity <muxent01> (Architecture <=>) compiled.
Compiling vhdl file "dff.vhd" in Library work.	Compiling vhdl file "dff.vhd" in Library work.
Entity <dff> compiled.	Entity <dff> compiled.
Entity <dff> (Architecture <ideal>) compiled.	Entity <dff> (Architecture <=>) compiled.
Compiling vhdl file "cda_gp.vhd" in Library work.	Compiling vhdl file "cda_gp.vhd" in Library work.
Entity <cda_gp> compiled.	Entity <cda_gp> compiled.
Entity <cda_gp> (Architecture <ideal>) compiled.	Entity <cda_gp> (Architecture <=>) compiled.
Compiling vhdl file "muxdff.vhd" in Library work.	Compiling vhdl file "muxdff.vhd" in Library work.
Entity <muxdff> compiled.	Entity <muxdff> compiled.
Entity <muxdff> (Architecture <ideal>) compiled.	Entity <muxdff> (Architecture <=>) compiled.
Compiling vhdl file "reg_file_functions.vhd" in Library work.	Compiling vhdl file "reg_file_functions.vhd" in Library work.
Package <reg_file_functions> compiled.	Package <reg_file_functions> compiled.
Package body <reg_file_functions> compiled.	Package body <reg_file_functions> compiled.
Compiling vhdl file "cda_add_n_bit.vhd" in Library work.	Compiling vhdl file "cda_add_n_bit.vhd" in Library work.
Entity <cda_add_n_bit> compiled.	Entity <cda_add_n_bit> compiled.
Entity <cda_add_n_bit> (Architecture <ideal>) compiled.	Entity <cda_add_n_bit> (Architecture <=>) compiled.
Compiling vhdl file "dmuxent01.vhd" in Library work.	Compiling vhdl file "dmuxent01.vhd" in Library work.
Entity <dmuxent01> compiled.	Entity <dmuxent01> compiled.
Entity <dmuxent01> (Architecture <ideal>) compiled.	Entity <dmuxent01> (Architecture <=>) compiled.
Compiling vhdl file "muxent01_bus.vhd" in Library work.	Compiling vhdl file "muxent01_bus.vhd" in Library work.
Entity <muxent01_bus> compiled.	Entity <muxent01_bus> compiled.
Entity <muxent01_bus> (Architecture <ideal>) compiled.	Entity <muxent01_bus> (Architecture <=>) compiled.
Compiling vhdl file "shift_reg.vhd" in Library work.	Compiling vhdl file "shift_reg.vhd" in Library work.
Entity <shift_reg> compiled.	Entity <shift_reg> compiled.
Entity <shift_reg> (Architecture <ideal>) compiled.	Entity <shift_reg> (Architecture <=>) compiled.
Compiling vhdl file "icpu_datapath_functions.vhd" in Library work.	Compiling vhdl file "branch_ctrl_functions.vhd" in Library work.
Package <cpu_datapath_functions> compiled.	Package <branch_ctrl_functions> compiled.
Compiling vhdl file "reg_file.vhd" in Library work.	Package body <branch_ctrl_functions> compiled.
Entity <reg_file> compiled.	Compiling vhdl file "counter.vhd" in Library work.
Entity <reg_file> (Architecture <ideal>) compiled.	Entity <counter> compiled.
Compiling vhdl file "ndn_alu_cda.vhd" in Library work.	Entity <counter> (Architecture <=>) compiled.
Entity <ndn_alu> compiled.	Compiling vhdl file "icpu_datapath_functions.vhd" in Library work.
Entity <ndn_alu> (Architecture <ideal>) compiled.	Package <cpu_datapath_functions> compiled.
Compiling vhdl file "branch_ctrl_functions.vhd" in Library work.	Compiling vhdl file "reg_file.vhd" in Library work.
Package <branch_ctrl_functions> compiled.	Entity <reg_file> compiled.
Package body <branch_ctrl_functions> compiled.	Entity <reg_file> (Architecture <=>) compiled.
Compiling vhdl file "counter.vhd" in Library work.	Compiling vhdl file "ndn_alu_cda.vhd" in Library work.
Entity <counter> compiled.	Entity <ndn_alu> compiled.
Entity <counter> (Architecture <ideal>) compiled.	Entity <ndn_alu> (Architecture <=>) compiled.
Compiling vhdl file "icpu.vhd" in Library work.	Compiling vhdl file "icpu_functions.vhd" in Library work.
Entity <cpu> compiled.	Package <cpu_functions> compiled.
Entity <cpu> (Architecture <Behavioral>) compiled.	Compiling vhdl file "icpu_datapath.vhd" in Library work.
Compiling vhdl file "from.vhd" in Library work.	Entity <cpu_datapath> compiled.
Entity <from> compiled.	Entity <cpu_datapath> (Architecture <=>) compiled.
Entity <from> (Architecture <ndv>) compiled.	Compiling vhdl file "branch_ctrl.vhd" in Library work.
Compiling vhdl file "sram.vhd" in Library work.	Entity <branch_ctrl> compiled.
Entity <sram> compiled.	Entity <branch_ctrl> (Architecture <=>) compiled.
Entity <sram> (Architecture <ndv>) compiled.	Compiling vhdl file "icpu.vhd" in Library work.
Compiling vhdl file "branch_ctrl.vhd" in Library work.	Entity <cpu> compiled.
Entity <branch_ctrl> compiled.	Entity <cpu> (Architecture <=>) compiled.
Entity <branch_ctrl> (Architecture <ideal>) compiled.	Compiling vhdl file "from.vhd" in Library work.
Compiling vhdl file "icpu_datapath.vhd" in Library work.	Entity <from> compiled.
Entity <cpu_datapath> compiled.	Entity <from> (Architecture <ndv>) compiled.
Entity <cpu_datapath> (Architecture <ideal>) compiled.	Compiling vhdl file "sram.vhd" in Library work.
Compiling vhdl file "icpu_functions.vhd" in Library work.	Entity <sram> compiled.

>xst -fh cpu.xst	>xst -fh cpu.xst
Release 14.7 - xst P.20131013 (m64)	Release 14.7 - xst P.20131013 (m64)
Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.	Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.
-> Parameter TMPDIR set to ./xstpropav.tmp	-> Parameter TMPDIR set to ./xstpropav.tmp
Total REAL time to Xst completion: 0.00 secs	Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.22 secs	Total CPU time to Xst completion: 0.24 secs
-> WARNING:Xst-3164 - Option "-debug" found multiple times in the command line. Only the first occurrence is considered.	-> WARNING:Xst-3164 - Option "-debug" found multiple times in the command line. Only the first occurrence is considered.
* HDL Compilation *	* HDL Compilation *
Compiling vhdl file "muxnto1.vhd" in Library work.	Compiling vhdl file "muxnto1.vhd" in Library work.
Entity <muxnto1> compiled.	Entity <muxnto1> compiled.
Entity <muxnto1> (Architecture <ideal>) compiled.	Entity <muxnto1> (Architecture <= >) compiled.
Compiling vhdl file "dff.vhd" in Library work.	Compiling vhdl file "dff.vhd" in Library work.
Entity <dff> compiled.	Entity <dff> compiled.
Entity <dff> (Architecture <ideal>) compiled.	Entity <dff> (Architecture <= >) compiled.
Compiling vhdl file "cila_gp.vhd" in Library work.	Compiling vhdl file "cila_gp.vhd" in Library work.
Entity <cila_gp> compiled.	Entity <cila_gp> compiled.
Entity <cila_gp> (Architecture <ideal>) compiled.	Entity <cila_gp> (Architecture <= >) compiled.
Compiling vhdl file "muxdff.vhd" in Library work.	Compiling vhdl file "muxdff.vhd" in Library work.
Entity <muxdff> compiled.	Entity <muxdff> compiled.
Entity <muxdff> (Architecture <ideal>) compiled.	Entity <muxdff> (Architecture <= >) compiled.
Compiling vhdl file "req_file_functions.vhd" in Library work.	Compiling vhdl file "req_file_functions.vhd" in Library work.
Package <req_file_functions> compiled.	Package <req_file_functions> compiled.
Package body <req_file_functions> compiled.	Package body <req_file_functions> compiled.
Compiling vhdl file "cila_add_n_bit.vhd" in Library work.	Compiling vhdl file "cila_add_n_bit.vhd" in Library work.
Entity <cila_add_n_bit> compiled.	Entity <cila_add_n_bit> compiled.
Entity <cila_add_n_bit> (Architecture <ideal>) compiled.	Entity <cila_add_n_bit> (Architecture <= >) compiled.
Compiling vhdl file "dmuxnto1.vhd" in Library work.	Compiling vhdl file "dmuxnto1.vhd" in Library work.
Entity <dmuxnto1> compiled.	Entity <dmuxnto1> compiled.
Entity <dmuxnto1> (Architecture <ideal>) compiled.	Entity <dmuxnto1> (Architecture <= >) compiled.
Compiling vhdl file "muxnto1_bus.vhd" in Library work.	Compiling vhdl file "muxnto1_bus.vhd" in Library work.
Entity <muxnto1_bus> compiled.	Entity <muxnto1_bus> compiled.
Entity <muxnto1_bus> (Architecture <ideal>) compiled.	Entity <muxnto1_bus> (Architecture <= >) compiled.
Compiling vhdl file "shift_req.vhd" in Library work.	Compiling vhdl file "shift_req.vhd" in Library work.
Entity <shift_req> compiled.	Entity <shift_req> compiled.
Entity <shift_req> (Architecture <ideal>) compiled.	Entity <shift_req> (Architecture <= >) compiled.
Compiling vhdl file "rcpu_datapath_functions.vhd" in Library work.	Compiling vhdl file "branch_ctrl_functions.vhd" in Library work.
Package <cpu_datapath_functions> compiled.	Package <branch_ctrl_functions> compiled.
Compiling vhdl file "req_file.vhd" in Library work.	Package body <branch_ctrl_functions> compiled.
Entity <req_file> compiled.	Compiling vhdl file "counter.vhd" in Library work.
Entity <req_file> (Architecture <ideal>) compiled.	Entity <counter> compiled.
Compiling vhdl file "rnda_alu_cila.vhd" in Library work.	Entity <counter> (Architecture <= >) compiled.
Entity <rnda_alu> compiled.	Compiling vhdl file "rcpu_datapath_functions.vhd" in Library work.
Entity <rnda_alu> (Architecture <ideal>) compiled.	Package <cpu_datapath_functions> compiled.
Compiling vhdl file "branch_ctrl_functions.vhd" in Library work.	Compiling vhdl file "req_file.vhd" in Library work.
Package <branch_ctrl_functions> compiled.	Entity <req_file> compiled.
Package body <branch_ctrl_functions> compiled.	Entity <req_file> (Architecture <= >) compiled.
Compiling vhdl file "counter.vhd" in Library work.	Compiling vhdl file "rnda_alu_cila.vhd" in Library work.
Entity <counter> compiled.	Entity <rnda_alu> compiled.
Entity <counter> (Architecture <ideal>) compiled.	Entity <rnda_alu> (Architecture <= >) compiled.
Compiling vhdl file "rcpu_functions.vhd" in Library work.	Compiling vhdl file "rcpu_functions.vhd" in Library work.
Package <cpu_functions> compiled.	Package <cpu_functions> compiled.
Compiling vhdl file "branch_ctrl.vhd" in Library work.	Compiling vhdl file "rcpu_datapath.vhd" in Library work.
Entity <branch_ctrl> compiled.	Entity <cpu_datapath> compiled.
Entity <branch_ctrl> (Architecture <ideal>) compiled.	Entity <cpu_datapath> (Architecture <= >) compiled.
Compiling vhdl file "rcpu_datapath.vhd" in Library work.	Compiling vhdl file "branch_ctrl.vhd" in Library work.
Entity <cpu_datapath> compiled.	Entity <branch_ctrl> compiled.
Entity <cpu_datapath> (Architecture <ideal>) compiled.	Entity <branch_ctrl> (Architecture <= >) compiled.
Compiling vhdl file "rcpu.vhd" in Library work.	Compiling vhdl file "rcpu.vhd" in Library work.
Entity <rcpu> compiled.	Entity <rcpu> compiled.
Entity <rcpu> (Architecture <ideal>) compiled.	Entity <rcpu> (Architecture <= >) compiled.
Compiling vhdl file "rom.vhd" in Library work.	Compiling vhdl file "rom.vhd" in Library work.
Entity <rom> compiled.	Entity <rom> compiled.
Entity <rom> (Architecture <ideal>) compiled.	Entity <rom> (Architecture <= >) compiled.
Compiling vhdl file "sram.vhd" in Library work.	Compiling vhdl file "sram.vhd" in Library work.
Entity <sram> compiled.	Entity <sram> compiled.

>xst -fh cpu.xst	>xst -fh cpu.xst
Release 14.7 - xst P 20131013 (m64)	Release 14.7 - xst P 20131013 (m64)
Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.	Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.
-> Parameter TMPDIR set to /xstprograw/tmp	-> Parameter TMPDIR set to /xstprograw/tmp
Total REAL time to Xst completion: 0.00 secs	Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.24 secs	Total CPU time to Xst completion: 0.24 secs
-> WARNING:Xst-3164 - Option "-debug" found multiple times in the command line. Only the first occurrence is considered.	-> WARNING:Xst-3164 - Option "-debug" found multiple times in the command line. Only the first occurrence is considered.
* HDL Compilation *	* HDL Compilation *
Compiling vhdl file "muxentof1.vhd" in Library work.	Compiling vhdl file "muxentof1.vhd" in Library work.
Entity <muxentof1> compiled.	Entity <muxentof1> compiled.
Entity <muxentof1> (Architecture <idealb1>) compiled.	Entity <muxentof1> (Architecture <=>) compiled.
Compiling vhdl file "dff.vhd" in Library work.	Compiling vhdl file "dff.vhd" in Library work.
Entity <dff> compiled.	Entity <dff> compiled.
Entity <dff> (Architecture <idealb1>) compiled.	Entity <dff> (Architecture <=>) compiled.
Compiling vhdl file "cila_gp.vhd" in Library work.	Compiling vhdl file "cila_gp.vhd" in Library work.
Entity <cila_gp> compiled.	Entity <cila_gp> compiled.
Entity <cila_gp> (Architecture <idealb1>) compiled.	Entity <cila_gp> (Architecture <=>) compiled.
Compiling vhdl file "muxdff.vhd" in Library work.	Compiling vhdl file "muxdff.vhd" in Library work.
Entity <muxdff> compiled.	Entity <muxdff> compiled.
Entity <muxdff> (Architecture <idealb1>) compiled.	Entity <muxdff> (Architecture <=>) compiled.
Compiling vhdl file "req_file_functions.vhd" in Library work.	Compiling vhdl file "req_file_functions.vhd" in Library work.
Package <req_file_functions> compiled.	Package <req_file_functions> compiled.
Package body <req_file_functions> compiled.	Package body <req_file_functions> compiled.
Compiling vhdl file "cila_add_n_bit.vhd" in Library work.	Compiling vhdl file "cila_add_n_bit.vhd" in Library work.
Entity <cila_add_n_bit> compiled.	Entity <cila_add_n_bit> compiled.
Entity <cila_add_n_bit> (Architecture <idealb1>) compiled.	Entity <cila_add_n_bit> (Architecture <=>) compiled.
Compiling vhdl file "dmuxentof1.vhd" in Library work.	Compiling vhdl file "dmuxentof1.vhd" in Library work.
Entity <dmuxentof1> compiled.	Entity <dmuxentof1> compiled.
Entity <dmuxentof1> (Architecture <idealb1>) compiled.	Entity <dmuxentof1> (Architecture <=>) compiled.
Compiling vhdl file "muxentof1_bus.vhd" in Library work.	Compiling vhdl file "muxentof1_bus.vhd" in Library work.
Entity <muxentof1_bus> compiled.	Entity <muxentof1_bus> compiled.
Entity <muxentof1_bus> (Architecture <idealb1>) compiled.	Entity <muxentof1_bus> (Architecture <=>) compiled.
Compiling vhdl file "shiftr_req.vhd" in Library work.	Compiling vhdl file "shiftr_req.vhd" in Library work.
Entity <shiftr_req> compiled.	Entity <shiftr_req> compiled.
Entity <shiftr_req> (Architecture <idealb1>) compiled.	Entity <shiftr_req> (Architecture <=>) compiled.
Compiling vhdl file "icpu_datapath_functions.vhd" in Library work.	Compiling vhdl file "branch_ctrl_functions.vhd" in Library work.
Package <cpu_datapath_functions> compiled.	Package <branch_ctrl_functions> compiled.
Compiling vhdl file "req_file.vhd" in Library work.	Package body <branch_ctrl_functions> compiled.
Entity <req_file> compiled.	Compiling vhdl file "counter.vhd" in Library work.
Entity <req_file> (Architecture <idealb1>) compiled.	Entity <counter> compiled.
Compiling vhdl file "rnda_alu_cila.vhd" in Library work.	Entity <counter> (Architecture <=>) compiled.
Entity <rnda_alu> compiled.	Compiling vhdl file "icpu_datapath_functions.vhd" in Library work.
Entity <rnda_alu> (Architecture <idealb1>) compiled.	Package <cpu_datapath_functions> compiled.
Compiling vhdl file "branch_ctrl_functions.vhd" in Library work.	Compiling vhdl file "req_file.vhd" in Library work.
Package <branch_ctrl_functions> compiled.	Entity <rnda_alu> compiled.
Package body <branch_ctrl_functions> compiled.	Entity <rnda_alu> (Architecture <=>) compiled.
Compiling vhdl file "icpu_functions.vhd" in Library work.	Compiling vhdl file "icpu_functions.vhd" in Library work.
Package <cpu_functions> compiled.	Package <cpu_functions> compiled.
Compiling vhdl file "branch_ctrl.vhd" in Library work.	Compiling vhdl file "icpu_datapath.vhd" in Library work.
Entity <branch_ctrl> compiled.	Entity <cpu_datapath> compiled.
Entity <branch_ctrl> (Architecture <idealb1>) compiled.	Entity <cpu_datapath> (Architecture <=>) compiled.
Compiling vhdl file "icpu_datapath.vhd" in Library work.	Compiling vhdl file "branch_ctrl.vhd" in Library work.
Entity <cpu_datapath> compiled.	Entity <branch_ctrl> compiled.
Entity <cpu_datapath> (Architecture <idealb1>) compiled.	Entity <branch_ctrl> (Architecture <=>) compiled.
Compiling vhdl file "icpu.vhd" in Library work.	Compiling vhdl file "icpu.vhd" in Library work.
Entity <icpu> compiled.	Entity <icpu> compiled.
Entity <icpu> (Architecture <idealb1>) compiled.	Entity <icpu> (Architecture <=>) compiled.
Compiling vhdl file "rom.vhd" in Library work.	Compiling vhdl file "rom.vhd" in Library work.
Entity <rom> compiled.	Entity <rom> compiled.
Entity <rom> (Architecture <ndtp>) compiled.	Entity <rom> (Architecture <ndtp>) compiled.
Compiling vhdl file "ram.vhd" in Library work.	Compiling vhdl file "ram.vhd" in Library work.
Entity <ram> compiled.	Entity <ram> compiled.

```

>xst -ifn cpu.xst
Release 14.7 - xst P.20131013 (nt64)
Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.
--> Parameter TMPDIR set to ./xst/projnav.tmp
Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.24 secs

--> WARNING:Xst:3164 - Option "-debug" found multiple times in the command line. Only the first occurrence
*          HDL Compilation          *
Compiling vhdl file "/muxnto1.vhd" in Library work.
Entity <muxnto1> compiled.
Entity <muxnto1> (Architecture <>) compiled.
Compiling vhdl file "/dff.vhd" in Library work.
Entity <dff> compiled.
Entity <dff> (Architecture <>) compiled.
Compiling vhdl file "/cla_gp.vhd" in Library work.
Entity <cla_gp> compiled.
Entity <cla_gp> (Architecture <>) compiled.
Compiling vhdl file "/muxdff.vhd" in Library work.
Entity <muxdff> compiled.
Entity <muxdff> (Architecture <>) compiled.
Compiling vhdl file "/reg_file_functions.vhd" in Library work.
Package <reg_file_functions> compiled.
Package body <reg_file_functions> compiled.
Compiling vhdl file "/cla_add_n_bit.vhd" in Library work.
Entity <cla_add_n_bit> compiled.
Entity <cla_add_n_bit> (Architecture <>) compiled.
Compiling vhdl file "/dmuxnto1.vhd" in Library work.
Entity <dmuxnto1> compiled.
Entity <dmuxnto1> (Architecture <>) compiled.
Compiling vhdl file "/muxnto1_bus.vhd" in Library work.
Entity <muxnto1_bus> compiled.
Entity <muxnto1_bus> (Architecture <>) compiled.
Compiling vhdl file "/shift_reg.vhd" in Library work.
Entity <shift_reg> compiled.
Entity <shift_reg> (Architecture <>) compiled.
Compiling vhdl file "/branch_ctrl_functions.vhd" in Library work.
Package <branch_ctrl_functions> compiled.
Package body <branch_ctrl_functions> compiled.
Compiling vhdl file "/counter.vhd" in Library work.
Entity <counter> compiled.
Entity <counter> (Architecture <>) compiled.
Compiling vhdl file "/cpu_datapath_functions.vhd" in Library work.
Package <cpu_datapath_functions> compiled.
Compiling vhdl file "/reg_file.vhd" in Library work.
Entity <reg_file> compiled.
Entity <reg_file> (Architecture <>) compiled.
Compiling vhdl file "/ndn_alu_cla.vhd" in Library work.
Entity <ndn_alu> compiled.
Entity <ndn_alu> (Architecture <>) compiled.
Compiling vhdl file "/cpu_functions.vhd" in Library work.
Package <cpu_functions> compiled.
Compiling vhdl file "/cpu_datapath.vhd" in Library work.
Entity <cpu_datapath> compiled.
Entity <cpu_datapath> (Architecture <>) compiled.
Compiling vhdl file "/branch_ctrl.vhd" in Library work.
Entity <branch_ctrl> compiled.
Entity <branch_ctrl> (Architecture <>) compiled.

```

Compiling vhdI file "/cpu.vhd" in Library work.
Entity <cpu> compiled.
Entity <cpu> (Architecture <>) compiled.
Compiling vhdI file "/rom.vhd" in Library work.
Entity <rom> compiled.
Entity <rom> (Architecture <ndv>) compiled.
Compiling vhdI file "/sram.vhd" in Library work.
Entity <sram> compiled.
Entity <sram> (Architecture <ndv>) compiled.
Total REAL time to Xst completion: 1.00 secs
Total CPU time to Xst completion: 0.66 secs

-->

Total memory usage is 4477168 kilobytes
Number of errors : 0 (0 filtered)
Number of warnings : 1 (0 filtered)
Number of infos : 0 (0 filtered)
>fuse -incremental -o cpu_tb_isim_beh.exe -prj cpu_tb.prj -top cpu_tb
ISim P.20131013 (signature 0x7708f090)
Number of CPUs detected in this system: 8
Turning on mult-threading, number of parallel sub-compilation jobs: 16
Determining compilation order of HDL files
Parsing VHDL file "muxnto1.vhd" into library work
Parsing VHDL file "dff.vhd" into library work
Parsing VHDL file "reg_file_functions.vhd" into library work
Parsing VHDL file "muxdff.vhd" into library work
Parsing VHDL file "cla_gp.vhd" into library work
Parsing VHDL file "shift_reg.vhd" into library work
Parsing VHDL file "muxnto1_bus.vhd" into library work
Parsing VHDL file "dmuxnto1.vhd" into library work
Parsing VHDL file "cla_add_n_bit.vhd" into library work
Parsing VHDL file "reg_file.vhd" into library work
Parsing VHDL file "ndn_alu_cla.vhd" into library work
Parsing VHDL file "cpu_datapath_functions.vhd" into library work
Parsing VHDL file "counter.vhd" into library work
Parsing VHDL file "branch_ctrl_functions.vhd" into library work
Parsing VHDL file "cpu_functions.vhd" into library work
Parsing VHDL file "cpu_datapath.vhd" into library work
Parsing VHDL file "branch_ctrl.vhd" into library work
Parsing VHDL file "sram.vhd" into library work
Parsing VHDL file "rom.vhd" into library work
Parsing VHDL file "cpu.vhd" into library work
Parsing VHDL file "cpu_tb.vhd" into library work
Starting static elaboration
Completed static elaboration
Compiling package standard
Compiling package std_logic_1164
Compiling package numeric_std
Compiling package math_real
Compiling package reg_file_functions
Compiling package cpu_datapath_functions
Compiling package cpu_functions
Compiling package textio
Compiling package std_logic_textio
Compiling package std_logic_arith
Compiling package std_logic_unsigned
Compiling package branch_ctrl_functions
Compiling architecture of entity dmuxnto1 [dmuxnto1(3)]
Compiling architecture of entity muxnto1 [muxnto1(3)]

Compiling architecture of entity muxnto1_bus [\muxnto1_bus(3,16)]
Compiling architecture of entity muxnto1 [\muxnto1(2)]
Compiling architecture of entity dff [dff_default]
Compiling architecture of entity muxdff [\muxdff(2)]
Compiling architecture of entity shift_reg [\shift_reg(16)]
Compiling architecture of entity reg_file [\reg_file(8,16)]
Compiling architecture of entity muxnto1 [\muxnto1(1)]
Compiling architecture of entity muxnto1_bus [\muxnto1_bus(1,16)]
Compiling architecture of entity cla_gp [cla_gp_default]
Compiling architecture of entity cla_add_n_bit [\cla_add_n_bit(16)]
Compiling architecture of entity ndn_alu [\ndn_alu(16)]
Compiling architecture of entity cpu_datapath [\cpu_datapath(8,16)]
Compiling architecture of entity muxdff [\muxdff(1)]
Compiling architecture of entity counter [\counter(16)]
Compiling architecture of entity branch_ctrl [\branch_ctrl(16)]
Compiling architecture of entity cpu [\cpu(8,16,4,4)]
Compiling architecture ndv of entity rom [\rom(4,16)]
Compiling architecture ndv of entity sram [\sram(4,16)]
Compiling architecture ndv of entity cpu_tb
Time Resolution for simulation is 1ps.
Waiting for 13 sub-compilation(s) to finish...
Compiled 53 VHDL Units
Built simulation executable cpu_tb_isim_beh.exe
Fuse Memory Usage: 40968 KB
Fuse CPU Usage: 1546 ms
>fuse -incremental -o cpu_logging_tb_isim_beh.exe -prj cpu_logging_tb.prj -top cpu_tb
ISim P.20131013 (signature 0x7708f090)
Number of CPUs detected in this system: 8
Turning on mult-threading, number of parallel sub-compilation jobs: 16
Determining compilation order of HDL files
Parsing VHDL file "muxnto1.vhd" into library work
Parsing VHDL file "dff.vhd" into library work
Parsing VHDL file "reg_file_functions.vhd" into library work
Parsing VHDL file "muxdff.vhd" into library work
Parsing VHDL file "cla_gp.vhd" into library work
Parsing VHDL file "shift_reg.vhd" into library work
Parsing VHDL file "muxnto1_bus.vhd" into library work
Parsing VHDL file "dmuxnto1.vhd" into library work
Parsing VHDL file "cla_add_n_bit.vhd" into library work
Parsing VHDL file "reg_file__logging.vhd" into library work
Parsing VHDL file "ndn_alu_cla.vhd" into library work
Parsing VHDL file "cpu_datapath_functions.vhd" into library work
Parsing VHDL file "counter.vhd" into library work
Parsing VHDL file "branch_ctrl_functions.vhd" into library work
Parsing VHDL file "cpu_functions.vhd" into library work
Parsing VHDL file "cpu_datapath__logging.vhd" into library work
Parsing VHDL file "branch_ctrl__logging.vhd" into library work
Parsing VHDL file "sram__logging.vhd" into library work
Parsing VHDL file "rom__logging.vhd" into library work
Parsing VHDL file "cpu.vhd" into library work
Parsing VHDL file "cpu_tb.vhd" into library work
Starting static elaboration
Completed static elaboration
Compiling package standard
Compiling package std_logic_1164
Compiling package numeric_std
Compiling package math_real
Compiling package reg_file_functions
Compiling package cpu_datapath_functions

Compiling package cpu_functions
 Compiling package textio
 Compiling package std_logic_textio
 Compiling package std_logic_arith
 Compiling package std_logic_unsigned
 Compiling package branch_ctrl_functions
 Compiling architecture of entity dmuxnto1 [dmuxnto1(3)]
 Compiling architecture of entity muxnto1 [muxnto1(3)]
 Compiling architecture of entity muxnto1_bus [muxnto1_bus(3,16)]
 Compiling architecture of entity muxnto1 [muxnto1(2)]
 Compiling architecture of entity dff [dff_default]
 Compiling architecture of entity muxdff [muxdff(2)]
 Compiling architecture of entity shift_reg [shift_reg(16)]
 Compiling architecture of entity reg_file [reg_file(8,16)]
 Compiling architecture of entity muxnto1 [muxnto1(1)]
 Compiling architecture of entity muxnto1_bus [muxnto1_bus(1,16)]
 Compiling architecture of entity cla_gp [cla_gp_default]
 Compiling architecture of entity cla_add_n_bit [cla_add_n_bit(16)]
 Compiling architecture of entity ndn_alu [ndn_alu(16)]
 Compiling architecture of entity cpu_datapath [cpu_datapath(8,16)]
 Compiling architecture of entity muxdff [muxdff(1)]
 Compiling architecture of entity counter [counter(16)]
 Compiling architecture of entity branch_ctrl [branch_ctrl(16)]
 Compiling architecture of entity cpu [cpu(8,16,4,4)]
 Compiling architecture ndv of entity rom [rom(4,16)]
 Compiling architecture ndv of entity sram [sram(4,16)]
 Compiling architecture ndv of entity cpu_tb
 Time Resolution for simulation is 1ps.
 Waiting for 5 sub-compilation(s) to finish...
 Compiled 53 VHDL Units
 Built simulation executable cpu_logging_tb_isim_beh.exe
 Fuse Memory Usage: 41188 KB
 Fuse CPU Usage: 1437 ms
 >cpu_tb_isim_beh.exe -tclbatch isim.tcl -wdb cpu_tb_isim_beh.wdb
 ISim P.20131013 (signature 0x7708f090)
 WARNING: A WEBPACK license was found.
 WARNING: Please use Xilinx License Configuration Manager to check out a full ISim license.
 WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for more information on t
 This is a Lite version of ISim.
 Time resolution is 1 ps
 Simulator is doing circuit initialization process.
 at 0 ps, Instance /cpu_tb/UUT/DATAPATH/REG_FILE1/REG_DMUX/ : Warning: NUMERIC_STD.TO_I
 at 0 ps, Instance /cpu_tb/UUT/DATAPATH/REG_FILE1/A_BUS_MUX/muxloop(0)VUI/ : Warning: NUM
 at 0 ps, Instance /cpu_tb/UUT/DATAPATH/REG_FILE1/A_BUS_MUX/muxloop(1)VUI/ : Warning: NUM
 at 0 ps, Instance /cpu_tb/UUT/DATAPATH/REG_FILE1/A_BUS_MUX/muxloop(2)VUI/ : Warning: NUM
 at 0 ps, Instance /cpu_tb/UUT/DATAPATH/REG_FILE1/A_BUS_MUX/muxloop(3)VUI/ : Warning: NUM
 at 0 ps, Instance /cpu_tb/UUT/DATAPATH/REG_FILE1/A_BUS_MUX/muxloop(4)VUI/ : Warning: NUM
 at 0 ps, Instance /cpu_tb/UUT/DATAPATH/REG_FILE1/A_BUS_MUX/muxloop(5)VUI/ : Warning: NUM
 at 0 ps, Instance /cpu_tb/UUT/DATAPATH/REG_FILE1/A_BUS_MUX/muxloop(6)VUI/ : Warning: NUM
 at 0 ps, Instance /cpu_tb/UUT/DATAPATH/REG_FILE1/A_BUS_MUX/muxloop(7)VUI/ : Warning: NUM
 at 0 ps, Instance /cpu_tb/UUT/DATAPATH/REG_FILE1/A_BUS_MUX/muxloop(8)VUI/ : Warning: NUM
 at 0 ps, Instance /cpu_tb/UUT/DATAPATH/REG_FILE1/A_BUS_MUX/muxloop(9)VUI/ : Warning: NUM
 at 0 ps, Instance /cpu_tb/UUT/DATAPATH/REG_FILE1/A_BUS_MUX/muxloop(10)VUI/ : Warning: NUI
 at 0 ps, Instance /cpu_tb/UUT/DATAPATH/REG_FILE1/A_BUS_MUX/muxloop(11)VUI/ : Warning: NUI
 at 0 ps, Instance /cpu_tb/UUT/DATAPATH/REG_FILE1/A_BUS_MUX/muxloop(12)VUI/ : Warning: NUI
 at 0 ps, Instance /cpu_tb/UUT/DATAPATH/REG_FILE1/A_BUS_MUX/muxloop(13)VUI/ : Warning: NUI
 at 0 ps, Instance /cpu_tb/UUT/DATAPATH/REG_FILE1/A_BUS_MUX/muxloop(14)VUI/ : Warning: NUI
 at 0 ps, Instance /cpu_tb/UUT/DATAPATH/REG_FILE1/A_BUS_MUX/muxloop(15)VUI/ : Warning: NUI
 at 0 ps, Instance /cpu_tb/UUT/DATAPATH/REG_FILE1/B_BUS_MUX/muxloop(0)VUI/ : Warning: NUM

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at 0 ps, Instance /cpu_tb/UUT/DATAPATH/REG_FILE1/regloop(1)\Regi/I1(15)\U0/U0/ : Warning: NU
at 0 ps, Instance /cpu_tb/UUT/DATAPATH/REG_FILE1/regloop(0)\Regi/I1(0)\U0/U0/ : Warning: NUM
at 0 ps, Instance /cpu_tb/UUT/DATAPATH/REG_FILE1/regloop(0)\Regi/I1(1)\U0/U0/ : Warning: NUM
at 0 ps, Instance /cpu_tb/UUT/DATAPATH/REG_FILE1/regloop(0)\Regi/I1(2)\U0/U0/ : Warning: NUM
at 0 ps, Instance /cpu_tb/UUT/DATAPATH/REG_FILE1/regloop(0)\Regi/I1(3)\U0/U0/ : Warning: NUM
at 0 ps, Instance /cpu_tb/UUT/DATAPATH/REG_FILE1/regloop(0)\Regi/I1(4)\U0/U0/ : Warning: NUM
at 0 ps, Instance /cpu_tb/UUT/DATAPATH/REG_FILE1/regloop(0)\Regi/I1(5)\U0/U0/ : Warning: NUM
at 0 ps, Instance /cpu_tb/UUT/DATAPATH/REG_FILE1/regloop(0)\Regi/I1(6)\U0/U0/ : Warning: NUM
at 0 ps, Instance /cpu_tb/UUT/DATAPATH/REG_FILE1/regloop(0)\Regi/I1(7)\U0/U0/ : Warning: NUM
at 0 ps, Instance /cpu_tb/UUT/DATAPATH/REG_FILE1/regloop(0)\Regi/I1(8)\U0/U0/ : Warning: NUM
at 0 ps, Instance /cpu_tb/UUT/DATAPATH/REG_FILE1/regloop(0)\Regi/I1(9)\U0/U0/ : Warning: NUM
at 0 ps, Instance /cpu_tb/UUT/DATAPATH/REG_FILE1/regloop(0)\Regi/I1(10)\U0/U0/ : Warning: NU
at 0 ps, Instance /cpu_tb/UUT/DATAPATH/REG_FILE1/regloop(0)\Regi/I1(11)\U0/U0/ : Warning: NU
at 0 ps, Instance /cpu_tb/UUT/DATAPATH/REG_FILE1/regloop(0)\Regi/I1(12)\U0/U0/ : Warning: NU
at 0 ps, Instance /cpu_tb/UUT/DATAPATH/REG_FILE1/regloop(0)\Regi/I1(13)\U0/U0/ : Warning: NU
at 0 ps, Instance /cpu_tb/UUT/DATAPATH/REG_FILE1/regloop(0)\Regi/I1(14)\U0/U0/ : Warning: NU
at 0 ps, Instance /cpu_tb/UUT/DATAPATH/REG_FILE1/regloop(0)\Regi/I1(15)\U0/U0/ : Warning: NU
at 0 ps, Instance /cpu_tb/UUT/JB_CTRL/PC_ctr/I1(0)\Ui/U0/ : Warning: NUMERIC_STD.TO_INTEGEI
at 0 ps, Instance /cpu_tb/UUT/JB_CTRL/PC_ctr/I1(1)\Ui/U0/ : Warning: NUMERIC_STD.TO_INTEGEI
at 0 ps, Instance /cpu_tb/UUT/JB_CTRL/PC_ctr/I1(2)\Ui/U0/ : Warning: NUMERIC_STD.TO_INTEGEI
at 0 ps, Instance /cpu_tb/UUT/JB_CTRL/PC_ctr/I1(3)\Ui/U0/ : Warning: NUMERIC_STD.TO_INTEGEI
at 0 ps, Instance /cpu_tb/UUT/JB_CTRL/PC_ctr/I1(4)\Ui/U0/ : Warning: NUMERIC_STD.TO_INTEGEI
at 0 ps, Instance /cpu_tb/UUT/JB_CTRL/PC_ctr/I1(5)\Ui/U0/ : Warning: NUMERIC_STD.TO_INTEGEI
at 0 ps, Instance /cpu_tb/UUT/JB_CTRL/PC_ctr/I1(6)\Ui/U0/ : Warning: NUMERIC_STD.TO_INTEGEI
at 0 ps, Instance /cpu_tb/UUT/JB_CTRL/PC_ctr/I1(7)\Ui/U0/ : Warning: NUMERIC_STD.TO_INTEGEI
at 0 ps, Instance /cpu_tb/UUT/JB_CTRL/PC_ctr/I1(8)\Ui/U0/ : Warning: NUMERIC_STD.TO_INTEGEI
at 0 ps, Instance /cpu_tb/UUT/JB_CTRL/PC_ctr/I1(9)\Ui/U0/ : Warning: NUMERIC_STD.TO_INTEGEI
at 0 ps, Instance /cpu_tb/UUT/JB_CTRL/PC_ctr/I1(10)\Ui/U0/ : Warning: NUMERIC_STD.TO_INTEGEI
at 0 ps, Instance /cpu_tb/UUT/JB_CTRL/PC_ctr/I1(11)\Ui/U0/ : Warning: NUMERIC_STD.TO_INTEGEI
at 0 ps, Instance /cpu_tb/UUT/JB_CTRL/PC_ctr/I1(12)\Ui/U0/ : Warning: NUMERIC_STD.TO_INTEGEI
at 0 ps, Instance /cpu_tb/UUT/JB_CTRL/PC_ctr/I1(13)\Ui/U0/ : Warning: NUMERIC_STD.TO_INTEGEI
at 0 ps, Instance /cpu_tb/UUT/JB_CTRL/PC_ctr/I1(14)\Ui/U0/ : Warning: NUMERIC_STD.TO_INTEGEI
at 0 ps, Instance /cpu_tb/UUT/JB_CTRL/PC_ctr/I1(15)\Ui/U0/ : Warning: NUMERIC_STD.TO_INTEGEI
at 0 ps, Instance /cpu_tb/DATAMEM/ : Warning: NUMERIC_STD.TO_INTEGER: metavalue detected, I
>cpu_logging_tb_isim_beh.exe -tclbatch isim.tcl -wdb cpu_logging_tb_isim_beh.wdb
ISim P.20131013 (signature 0x7708f090)
WARNING: A WEBPACK license was found.
WARNING: Please use Xilinx License Configuration Manager to check out a full ISim license.
WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for more information on t
This is a Lite version of ISim.
Time resolution is 1 ps
Simulator is doing circuit initialization process.
at 0 ps, Instance /cpu_tb/UUT/DATAPATH/REG_FILE1/REG_DMUX/ : Warning: NUMERIC_STD.TO_I
at 0 ps, Instance /cpu_tb/UUT/DATAPATH/REG_FILE1/A_BUS_MUX/muxloop(0)\Ui/ : Warning: NUM
at 0 ps, Instance /cpu_tb/UUT/DATAPATH/REG_FILE1/A_BUS_MUX/muxloop(1)\Ui/ : Warning: NUM
at 0 ps, Instance /cpu_tb/UUT/DATAPATH/REG_FILE1/A_BUS_MUX/muxloop(2)\Ui/ : Warning: NUM
at 0 ps, Instance /cpu_tb/UUT/DATAPATH/REG_FILE1/A_BUS_MUX/muxloop(3)\Ui/ : Warning: NUM
at 0 ps, Instance /cpu_tb/UUT/DATAPATH/REG_FILE1/A_BUS_MUX/muxloop(4)\Ui/ : Warning: NUM
at 0 ps, Instance /cpu_tb/UUT/DATAPATH/REG_FILE1/A_BUS_MUX/muxloop(5)\Ui/ : Warning: NUM
at 0 ps, Instance /cpu_tb/UUT/DATAPATH/REG_FILE1/A_BUS_MUX/muxloop(6)\Ui/ : Warning: NUM
at 0 ps, Instance /cpu_tb/UUT/DATAPATH/REG_FILE1/A_BUS_MUX/muxloop(7)\Ui/ : Warning: NUM
at 0 ps, Instance /cpu_tb/UUT/DATAPATH/REG_FILE1/A_BUS_MUX/muxloop(8)\Ui/ : Warning: NUM
at 0 ps, Instance /cpu_tb/UUT/DATAPATH/REG_FILE1/A_BUS_MUX/muxloop(9)\Ui/ : Warning: NUM
at 0 ps, Instance /cpu_tb/UUT/DATAPATH/REG_FILE1/A_BUS_MUX/muxloop(10)\Ui/ : Warning: NUI
at 0 ps, Instance /cpu_tb/UUT/DATAPATH/REG_FILE1/A_BUS_MUX/muxloop(11)\Ui/ : Warning: NUI
at 0 ps, Instance /cpu_tb/UUT/DATAPATH/REG_FILE1/A_BUS_MUX/muxloop(12)\Ui/ : Warning: NUI
at 0 ps, Instance /cpu_tb/UUT/DATAPATH/REG_FILE1/A_BUS_MUX/muxloop(13)\Ui/ : Warning: NUI
at 0 ps, Instance /cpu_tb/UUT/DATAPATH/REG_FILE1/A_BUS_MUX/muxloop(14)\Ui/ : Warning: NUI
at 0 ps, Instance /cpu_tb/UUT/DATAPATH/REG_FILE1/A_BUS_MUX/muxloop(15)\Ui/ : Warning: NUI

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at 0 ps, Instance /cpu_tb/UUT/DATAPATH/REG_FILE1/regloop(1)\Regi/I1(9)\VU0/U0/ : Warning: NUM
 at 0 ps, Instance /cpu_tb/UUT/DATAPATH/REG_FILE1/regloop(1)\Regi/I1(10)\VU0/U0/ : Warning: NU
 at 0 ps, Instance /cpu_tb/UUT/DATAPATH/REG_FILE1/regloop(1)\Regi/I1(11)\VU0/U0/ : Warning: NU
 at 0 ps, Instance /cpu_tb/UUT/DATAPATH/REG_FILE1/regloop(1)\Regi/I1(12)\VU0/U0/ : Warning: NU
 at 0 ps, Instance /cpu_tb/UUT/DATAPATH/REG_FILE1/regloop(1)\Regi/I1(13)\VU0/U0/ : Warning: NU
 at 0 ps, Instance /cpu_tb/UUT/DATAPATH/REG_FILE1/regloop(1)\Regi/I1(14)\VU0/U0/ : Warning: NU
 at 0 ps, Instance /cpu_tb/UUT/DATAPATH/REG_FILE1/regloop(1)\Regi/I1(15)\VU0/U0/ : Warning: NU
 at 0 ps, Instance /cpu_tb/UUT/DATAPATH/REG_FILE1/regloop(0)\Regi/I1(0)\VU0/U0/ : Warning: NUM
 at 0 ps, Instance /cpu_tb/UUT/DATAPATH/REG_FILE1/regloop(0)\Regi/I1(1)\VU0/U0/ : Warning: NUM
 at 0 ps, Instance /cpu_tb/UUT/DATAPATH/REG_FILE1/regloop(0)\Regi/I1(2)\VU0/U0/ : Warning: NUM
 at 0 ps, Instance /cpu_tb/UUT/DATAPATH/REG_FILE1/regloop(0)\Regi/I1(3)\VU0/U0/ : Warning: NUM
 at 0 ps, Instance /cpu_tb/UUT/DATAPATH/REG_FILE1/regloop(0)\Regi/I1(4)\VU0/U0/ : Warning: NUM
 at 0 ps, Instance /cpu_tb/UUT/DATAPATH/REG_FILE1/regloop(0)\Regi/I1(5)\VU0/U0/ : Warning: NUM
 at 0 ps, Instance /cpu_tb/UUT/DATAPATH/REG_FILE1/regloop(0)\Regi/I1(6)\VU0/U0/ : Warning: NUM
 at 0 ps, Instance /cpu_tb/UUT/DATAPATH/REG_FILE1/regloop(0)\Regi/I1(7)\VU0/U0/ : Warning: NUM
 at 0 ps, Instance /cpu_tb/UUT/DATAPATH/REG_FILE1/regloop(0)\Regi/I1(8)\VU0/U0/ : Warning: NUM
 at 0 ps, Instance /cpu_tb/UUT/DATAPATH/REG_FILE1/regloop(0)\Regi/I1(9)\VU0/U0/ : Warning: NUM
 at 0 ps, Instance /cpu_tb/UUT/DATAPATH/REG_FILE1/regloop(0)\Regi/I1(10)\VU0/U0/ : Warning: NU
 at 0 ps, Instance /cpu_tb/UUT/DATAPATH/REG_FILE1/regloop(0)\Regi/I1(11)\VU0/U0/ : Warning: NU
 at 0 ps, Instance /cpu_tb/UUT/DATAPATH/REG_FILE1/regloop(0)\Regi/I1(12)\VU0/U0/ : Warning: NU
 at 0 ps, Instance /cpu_tb/UUT/DATAPATH/REG_FILE1/regloop(0)\Regi/I1(13)\VU0/U0/ : Warning: NU
 at 0 ps, Instance /cpu_tb/UUT/DATAPATH/REG_FILE1/regloop(0)\Regi/I1(14)\VU0/U0/ : Warning: NU
 at 0 ps, Instance /cpu_tb/UUT/DATAPATH/REG_FILE1/regloop(0)\Regi/I1(15)\VU0/U0/ : Warning: NU
 at 0 ps, Instance /cpu_tb/UUT/JB_CTRL/PC_ctr/I1(0)\Ui/U0/ : Warning: NUMERIC_STD.TO_INTEGE
 at 0 ps, Instance /cpu_tb/UUT/JB_CTRL/PC_ctr/I1(1)\Ui/U0/ : Warning: NUMERIC_STD.TO_INTEGE
 at 0 ps, Instance /cpu_tb/UUT/JB_CTRL/PC_ctr/I1(2)\Ui/U0/ : Warning: NUMERIC_STD.TO_INTEGE
 at 0 ps, Instance /cpu_tb/UUT/JB_CTRL/PC_ctr/I1(3)\Ui/U0/ : Warning: NUMERIC_STD.TO_INTEGE
 at 0 ps, Instance /cpu_tb/UUT/JB_CTRL/PC_ctr/I1(4)\Ui/U0/ : Warning: NUMERIC_STD.TO_INTEGE
 at 0 ps, Instance /cpu_tb/UUT/JB_CTRL/PC_ctr/I1(5)\Ui/U0/ : Warning: NUMERIC_STD.TO_INTEGE
 at 0 ps, Instance /cpu_tb/UUT/JB_CTRL/PC_ctr/I1(6)\Ui/U0/ : Warning: NUMERIC_STD.TO_INTEGE
 at 0 ps, Instance /cpu_tb/UUT/JB_CTRL/PC_ctr/I1(7)\Ui/U0/ : Warning: NUMERIC_STD.TO_INTEGE
 at 0 ps, Instance /cpu_tb/UUT/JB_CTRL/PC_ctr/I1(8)\Ui/U0/ : Warning: NUMERIC_STD.TO_INTEGE
 at 0 ps, Instance /cpu_tb/UUT/JB_CTRL/PC_ctr/I1(9)\Ui/U0/ : Warning: NUMERIC_STD.TO_INTEGE
 at 0 ps, Instance /cpu_tb/UUT/JB_CTRL/PC_ctr/I1(10)\Ui/U0/ : Warning: NUMERIC_STD.TO_INTEGE
 at 0 ps, Instance /cpu_tb/UUT/JB_CTRL/PC_ctr/I1(11)\Ui/U0/ : Warning: NUMERIC_STD.TO_INTEGE
 at 0 ps, Instance /cpu_tb/UUT/JB_CTRL/PC_ctr/I1(12)\Ui/U0/ : Warning: NUMERIC_STD.TO_INTEGE
 at 0 ps, Instance /cpu_tb/UUT/JB_CTRL/PC_ctr/I1(13)\Ui/U0/ : Warning: NUMERIC_STD.TO_INTEGE
 at 0 ps, Instance /cpu_tb/UUT/JB_CTRL/PC_ctr/I1(14)\Ui/U0/ : Warning: NUMERIC_STD.TO_INTEGE
 at 0 ps, Instance /cpu_tb/UUT/JB_CTRL/PC_ctr/I1(15)\Ui/U0/ : Warning: NUMERIC_STD.TO_INTEGE
 at 0 ps: Note: ROM: addr: 0IR: 40593CMD: R(2)≤=1
 at 0 ps, Instance /cpu_tb/DATAMEM/ : Warning: NUMERIC_STD.TO_INTEGER: metavalue detected, r
 at 300 ns(1): Note: REG FILE:00000000/cpu_tb/UUT/DATAPATH/REG_FILE1/).
 at 300 ns(1): Note: PC: 0N: '0'C: '0'V: '0'Z: '0'PL: '0'JB: '0'BC: '1'JB_address: 17/cpu_tb/UUT/JB_CTRL/
 at 300 ns(5): Note: ROM: addr: 1IR: 15831CMD: R(7)≤=M(R(2))
 at 500 ns(2): Note: RAM: 000000000000=14620/cpu_tb/DATAMEM/).
 at 700 ns(1): Note: REG FILE:00000100/cpu_tb/UUT/DATAPATH/REG_FILE1/).
 at 700 ns(1): Note: PC: 1N: '0'C: '0'V: '0'Z: '0'PL: '0'JB: '1'BC: '0'JB_address: 1/cpu_tb/UUT/JB_CTRL/
 at 700 ns(5): Note: ROM: addr: 2IR: 7751CMD: R(1)≤=R(7)
 at 900 ns(2): Note: RAM: 000000000000=14620/cpu_tb/DATAMEM/).
 at 1100 ns(1): Note: REG FILE:20000100/cpu_tb/UUT/DATAPATH/REG_FILE1/).
 at 1100 ns(1): Note: PC: 2N: '0'C: '0'V: '0'Z: '0'PL: '0'JB: '0'BC: '1'JB_address: 15/cpu_tb/UUT/JB_CTR
 at 1100 ns(5): Note: ROM: addr: 3IR: 33018CMD: R(3)≤=R(7)+2
 at 1300 ns(2): Note: RAM: 000000000000=14620/cpu_tb/DATAMEM/).
 at 1500 ns(1): Note: REG FILE:20000120/cpu_tb/UUT/DATAPATH/REG_FILE1/).
 at 1500 ns(1): Note: PC: 3N: '0'C: '0'V: '0'Z: '0'PL: '0'JB: '0'BC: '0'JB_address: 26/cpu_tb/UUT/JB_CTF
 at 1500 ns(5): Note: ROM: addr: 4IR: 33359CMD: R(1)≤=R(1)-7
 at 1700 ns(2): Note: RAM: 000000000000=14620/cpu_tb/DATAMEM/).
 at 1900 ns(1): Note: REG FILE:20004120/cpu_tb/UUT/DATAPATH/REG_FILE1/).
 at 1900 ns(1): Note: PC: 4N: '1'C: '0'V: '0'Z: '0'PL: '0'JB: '0'BC: '1'JB_address: 15/cpu_tb/UUT/JB_CTF

at 1900 ns(5): Note: ROM: $\bar{a}ddr: 5IR: 49676CMD: IF R(1) < 0; (PC = PC + (4))$
 at 2100 ns(2): Note: RAM: $000000000000-14620 (/cpu_tb/DATAMEM/)$.
 at 2300 ns(1): Note: REG FILE: $200041-50 (/cpu_tb/UUT/DATAPATH/REG_FILE1/)$.
 at 2300 ns(1): Note: PC: $5N: '1'C: '0'V: '0'Z: '0'PL: '1'JB: '0'BC: '1'JB_address: 4 (/cpu_tb/UUT/JB_CTRL$
 at 2300 ns(5): Note: ROM: $\bar{a}ddr: 9IR: 56773CMD: IF R(0) = 0; (PC = PC + (-3))$
 at 2500 ns(2): Note: RAM: $000000000000-14620 (/cpu_tb/DATAMEM/)$.
 at 2700 ns(1): Note: REG FILE: $200041-50 (/cpu_tb/UUT/DATAPATH/REG_FILE1/)$.
 at 2700 ns(1): Note: PC: $9N: '0'C: '0'V: '0'Z: '1'PL: '1'JB: '0'BC: '0'JB_address: -3 (/cpu_tb/UUT/JB_CTR$
 at 2700 ns(5): Note: ROM: $\bar{a}ddr: 6IR: 11CMD: R(0) \leq R(1) PLUS R(3)$
 at 2900 ns(2): Note: RAM: $000000000000-14620 (/cpu_tb/DATAMEM/)$.
 at 3100 ns(1): Note: REG FILE: $200041-50 (/cpu_tb/UUT/DATAPATH/REG_FILE1/)$.
 at 3100 ns(1): Note: PC: $6N: '1'C: '0'V: '0'Z: '0'PL: '0'JB: '0'BC: '0'JB_address: 3 (/cpu_tb/UUT/JB_CTRL$
 at 3100 ns(5): Note: ROM: $\bar{a}ddr: 7IR: 24088CMD: M(R(3)) \leq R(0)$
 at 3300 ns(2): Note: RAM: $000000000000-14620 (/cpu_tb/DATAMEM/)$.
 at 3500 ns(1): Note: REG FILE: $200041-5-1 (/cpu_tb/UUT/DATAPATH/REG_FILE1/)$.
 at 3500 ns(1): Note: PC: $7N: '1'C: '1'V: '0'Z: '0'PL: '0'JB: '0'BC: '1'JB_address: 0 (/cpu_tb/UUT/JB_CTRL$
 at 3500 ns(5): Note: ROM: $\bar{a}ddr: 8IR: 8007CMD: R(5) \leq R(7)$
 at 3700 ns(2): Note: RAM: $000000000000-14620 (/cpu_tb/DATAMEM/)$.
 at 3900 ns(1): Note: REG FILE: $200041-5-1 (/cpu_tb/UUT/DATAPATH/REG_FILE1/)$.
 at 3900 ns(1): Note: PC: $8N: '0'C: '1'V: '1'Z: '0'PL: '0'JB: '0'BC: '1'JB_address: -17 (/cpu_tb/UUT/JB_CTI$
 at 3900 ns(5): Note: ROM: $\bar{a}ddr: 9IR: 56773CMD: IF R(0) = 0; (PC = PC + (-3))$
 at 4100 ns(2): Note: RAM: $000000000000-14620 (/cpu_tb/DATAMEM/)$.
 at 4300 ns(1): Note: REG FILE: $202041-5-1 (/cpu_tb/UUT/DATAPATH/REG_FILE1/)$.
 at 4300 ns(1): Note: PC: $9N: '1'C: '1'V: '0'Z: '0'PL: '1'JB: '0'BC: '0'JB_address: -3 (/cpu_tb/UUT/JB_CTR$
 at 4300 ns(5): Note: ROM: $\bar{a}ddr: 10IR: 15751CMD: R(6) \leq M(R(0))$
 at 4500 ns(2): Note: RAM: $000000000000-14620 (/cpu_tb/DATAMEM/)$.
 at 4700 ns(1): Note: REG FILE: $202041-5-1 (/cpu_tb/UUT/DATAPATH/REG_FILE1/)$.
 at 4700 ns(1): Note: PC: $10N: '1'C: '1'V: '0'Z: '0'PL: '0'JB: '1'BC: '0'JB_address: -1 (/cpu_tb/UUT/JB_CTI$
 at 4700 ns(5): Note: ROM: $\bar{a}ddr: 11IR: 6542CMD: R(6) \leq R(1) XOR R(6)$
 at 4900 ns(2): Note: RAM: $000000000000-14620 (/cpu_tb/DATAMEM/)$.
 at 5100 ns(1): Note: REG FILE: $202041-5-1 (/cpu_tb/UUT/DATAPATH/REG_FILE1/)$.
 at 5100 ns(1): Note: PC: $11N: '1'C: '0'V: '0'Z: '0'PL: '0'JB: '0'BC: '0'JB_address: -10 (/cpu_tb/UUT/JB_C1$
 at 5100 ns(5): Note: ROM: $\bar{a}ddr: 12IR: 7942CMD: R(4) \leq R(6)$
 at 5300 ns(2): Note: RAM: $000000000000-14620 (/cpu_tb/DATAMEM/)$.
 at 5500 ns(1): Note: REG FILE: $2-52041-5-1 (/cpu_tb/UUT/DATAPATH/REG_FILE1/)$.
 at 5500 ns(1): Note: PC: $12N: '1'C: '1'V: '0'Z: '0'PL: '0'JB: '0'BC: '1'JB_address: -26 (/cpu_tb/UUT/JB_C$
 at 5500 ns(5): Note: ROM: $\bar{a}ddr: 13IR: 1968CMD: R(6) \leq R(6) MINUS 1$
 at 5700 ns(2): Note: RAM: $000000000000-14620 (/cpu_tb/DATAMEM/)$.
 at 5900 ns(1): Note: REG FILE: $2-52-541-5-1 (/cpu_tb/UUT/DATAPATH/REG_FILE1/)$.
 at 5900 ns(1): Note: PC: $13N: '1'C: '1'V: '0'Z: '0'PL: '0'JB: '0'BC: '1'JB_address: -16 (/cpu_tb/UUT/JB_C$
 at 5900 ns(5): Note: ROM: $\bar{a}ddr: 14IR: 50164CMD: IF R(6) < 0; (PC = PC + (-4))$
 at 6100 ns(2): Note: RAM: $000000000000-14620 (/cpu_tb/DATAMEM/)$.
 at 6300 ns(1): Note: REG FILE: $2-62-541-5-1 (/cpu_tb/UUT/DATAPATH/REG_FILE1/)$.
 at 6300 ns(1): Note: PC: $14N: '1'C: '0'V: '0'Z: '0'PL: '1'JB: '0'BC: '1'JB_address: -4 (/cpu_tb/UUT/JB_CTI$
 at 6300 ns(5): Note: ROM: $\bar{a}ddr: 10IR: 15751CMD: R(6) \leq M(R(0))$
 at 6500 ns(2): Note: RAM: $000000000000-14620 (/cpu_tb/DATAMEM/)$.
 at 6700 ns(1): Note: REG FILE: $2-62-541-5-1 (/cpu_tb/UUT/DATAPATH/REG_FILE1/)$.
 at 6700 ns(1): Note: PC: $10N: '1'C: '1'V: '0'Z: '0'PL: '0'JB: '1'BC: '0'JB_address: -1 (/cpu_tb/UUT/JB_CTI$
 at 6700 ns(5): Note: ROM: $\bar{a}ddr: 11IR: 6542CMD: R(6) \leq R(1) XOR R(6)$
 at 6900 ns(2): Note: RAM: $000000000000-14620 (/cpu_tb/DATAMEM/)$.
 at 7100 ns(1): Note: REG FILE: $202-541-5-1 (/cpu_tb/UUT/DATAPATH/REG_FILE1/)$.
 at 7100 ns(1): Note: PC: $11N: '1'C: '0'V: '0'Z: '0'PL: '0'JB: '0'BC: '0'JB_address: -10 (/cpu_tb/UUT/JB_C1$
 at 7100 ns(5): Note: ROM: $\bar{a}ddr: 12IR: 7942CMD: R(4) \leq R(6)$
 at 7300 ns(2): Note: RAM: $000000000000-14620 (/cpu_tb/DATAMEM/)$.
 at 7500 ns(1): Note: REG FILE: $2-52-541-5-1 (/cpu_tb/UUT/DATAPATH/REG_FILE1/)$.
 at 7500 ns(1): Note: PC: $12N: '1'C: '1'V: '0'Z: '0'PL: '0'JB: '0'BC: '1'JB_address: -26 (/cpu_tb/UUT/JB_C$
 at 7500 ns(5): Note: ROM: $\bar{a}ddr: 13IR: 1968CMD: R(6) \leq R(6) MINUS 1$
 at 7700 ns(2): Note: RAM: $000000000000-14620 (/cpu_tb/DATAMEM/)$.
 at 7900 ns(1): Note: REG FILE: $2-52-541-5-1 (/cpu_tb/UUT/DATAPATH/REG_FILE1/)$.

at 7900 ns(1): Note: PC: 13N: '1'C: '1'V: '0'Z: '0'PL: '0'JB: '0'BC: '1'JB_address: -16 (/cpu_tb/UUT/JB_C
 at 7900 ns(5): Note: ROM: addr: 14IR: 50164CMD: IF R(6) < 0; (PC= PC + (-4))
 at 8100 ns(2): Note: RAM: 000000000000-1-14620 (/cpu_tb/DATAMEM/).
 at 8300 ns(1): Note: REG FILE:2-62-541-5-1 (/cpu_tb/UUT/DATAPATH/REG_FILE1/).
 at 8300 ns(1): Note: PC: 14N: '1'C: '0'V: '0'Z: '0'PL: '1'JB: '0'BC: '1'JB_address: -4 (/cpu_tb/UUT/JB_CTI
 at 8300 ns(5): Note: ROM: addr: 10IR: 15751CMD: R(6)≤M(R(0))
 at 8500 ns(2): Note: RAM: 000000000000-1-14620 (/cpu_tb/DATAMEM/).
 at 8700 ns(1): Note: REG FILE:2-62-541-5-1 (/cpu_tb/UUT/DATAPATH/REG_FILE1/).
 at 8700 ns(1): Note: PC: 10N: '1'C: '1'V: '0'Z: '0'PL: '0'JB: '1'BC: '0'JB_address: -1 (/cpu_tb/UUT/JB_CTI
 at 8700 ns(5): Note: ROM: addr: 11IR: 6542CMD: R(6)≤R(1) XOR R(6)
 at 8900 ns(2): Note: RAM: 000000000000-1-14620 (/cpu_tb/DATAMEM/).
 at 9100 ns(1): Note: REG FILE:202-541-5-1 (/cpu_tb/UUT/DATAPATH/REG_FILE1/).
 at 9100 ns(1): Note: PC: 11N: '1'C: '0'V: '0'Z: '0'PL: '0'JB: '0'BC: '0'JB_address: -10 (/cpu_tb/UUT/JB_CTI
 at 9100 ns(5): Note: ROM: addr: 12IR: 7942CMD: R(4)≤R(6)
 at 9300 ns(2): Note: RAM: 000000000000-1-14620 (/cpu_tb/DATAMEM/).
 at 9500 ns(1): Note: REG FILE:2-52-541-5-1 (/cpu_tb/UUT/DATAPATH/REG_FILE1/).
 at 9500 ns(1): Note: PC: 12N: '1'C: '1'V: '0'Z: '0'PL: '0'JB: '0'BC: '1'JB_address: -26 (/cpu_tb/UUT/JB_C
 at 9500 ns(5): Note: ROM: addr: 13IR: 1968CMD: R(6)≤R(6) MINUS 1
 at 9700 ns(2): Note: RAM: 000000000000-1-14620 (/cpu_tb/DATAMEM/).
 at 9900 ns(1): Note: REG FILE:2-52-541-5-1 (/cpu_tb/UUT/DATAPATH/REG_FILE1/).
 at 9900 ns(1): Note: PC: 13N: '1'C: '1'V: '0'Z: '0'PL: '0'JB: '0'BC: '1'JB_address: -16 (/cpu_tb/UUT/JB_C
 at 9900 ns(5): Note: ROM: addr: 14IR: 50164CMD: IF R(6) < 0; (PC= PC + (-4))

rence is considered.

the differences between the Lite and the Full version.

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