

BARREL SHIFTER

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-- *****
-- **** STUDENT: 64000225
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-- KOMENTARJI K OCENI NALOGE
-- Matej Možek: Ni pripomb
-- *****

library ieee;
use ieee.std_logic_1164.all;
use IEEE.numeric_std.all;
use WORK.cordic_pkg.all;

ENTITY barrel_shifter_sra IS
    GENERIC(
        width : integer := 32;
        size : integer := 32
    );
    PORT(
        input : IN std_logic_vector ( WIDTH-1 DOWNT0 0 );
        output : OUT std_logic_vector ( WIDTH-1 DOWNT0 0 );
        n : IN std_logic_vector ( sizeof( size - 1 ) - 1 DOWNT0 0 )
    );
END barrel_shifter_sra;

architecture ndv of barrel_shifter_sra is
    type barrel_shifter_type is array ( 0 to size - 1 ) of std_logic_vector ( width - 1 downto 0 );
    signal barrel_shifter : barrel_shifter_type := ( others => ( others => '0' ) );

begin

    shifts: process ( input ) is
    begin
        for i in size-1 downto 0 loop
            barrel_shifter( i ) <= std_logic_vector( resize( signed( input( WIDTH - 1 downto i ) ),
output'length ) );
        end loop;
    end process;

    output <= barrel_shifter( to_integer( unsigned( n ) ) );

end ndv;

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-- *****
-- **** STUDENT: 64190088
-- *****
-- KOMENTARJI K OCENI NALOGE
-- Matej Možek: Ni pripomb
-- *****

library ieee;
use ieee.std_logic_1164.all;
use IEEE.numeric_std.all;
use WORK.cordic_pkg.all;

ENTITY barrel_shifter_sra IS
    GENERIC(
        width : integer := 32;
        size : integer := 32
    );
    PORT(
        input : IN std_logic_vector ( WIDTH-1 DOWNT0 0 );
        output : OUT std_logic_vector ( WIDTH-1 DOWNT0 0 );
        n : IN std_logic_vector ( sizeof( size - 1 ) - 1 DOWNT0 0 )
    );
END barrel_shifter_sra;

architecture ndv of barrel_shifter_sra is
    type barrel_shifter_type is array ( 0 to size - 1 ) of std_logic_vector ( width - 1 downto 0 );
    signal barrel_shifter : barrel_shifter_type := ( others => ( others => '0' ) );

begin

    process( input )
    begin
        for i in size-1 downto 0 loop
            barrel_shifter( i ) <= std_logic_vector( resize( signed( input( WIDTH - 1 downto i ) ),
output'length ) );
        end loop;
    end process;

    output <= barrel_shifter( to_integer( unsigned( n ) ) );

end ndv;

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-- *****
-- **** STUDENT: 64200163
-- *****
-- KOMENTARJI K OCENI NALOGE
-- Matej Možek: Ni pripomb
-- *****

library ieee;
use ieee.std_logic_1164.all;
use ieee.numeric_std.all;
use work.cordic_pkg.all;

entity barrel_shifter_sra is
    generic(
        width : integer := 32;
        size : integer := 32
    );
    port(
        input : in std_logic_vector( width - 1 downto 0 );
        output : out std_logic_vector( width - 1 downto 0 );
        n : in std_logic_vector ( sizeof( size - 1 ) - 1 downto 0 )
    );
end barrel_shifter_sra;

architecture ndv of barrel_shifter_sra is
    type barrel_shifter_type is array ( 0 to size - 1 ) of std_logic_vector ( width - 1 downto 0 );
    signal barrel_shifter : barrel_shifter_type := ( others => ( others => '0' ) );
begin
    shift_right_arithmetic : process( input )
    begin
        for i in size - 1 downto 0 loop
            barrel_shifter( i ) <= std_logic_vector( resize( signed( input( width - 1 downto i ) ),
output'length ) );
        end loop;
    end process;
    output <= barrel_shifter( to_integer( unsigned( n ) ) );
end ndv;

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-- *****
-- **** STUDENT: 64200296
-- *****
-- KOMENTARJI K OCENI NALOGE
-- Matej Možek: Ni pripomb
-- *****

library ieee;
use ieee.std_logic_1164.all;
use IEEE.numeric_std.all;
use WORK.cordic_pkg.all;

ENTITY barrel_shifter_sra IS
    GENERIC(
        width : integer := 32;
        size : integer := 32
    );
    PORT(
        input : IN std_logic_vector ( WIDTH-1 DOWNT0 0 );
        output : OUT std_logic_vector ( WIDTH-1 DOWNT0 0 );
        n : IN std_logic_vector ( sizeof( size - 1 ) - 1 DOWNT0 0 )
    );
END barrel_shifter_sra;

architecture ndv of barrel_shifter_sra is
    type barrel_shifter_type is array ( 0 to size - 1 ) of std_logic_vector ( width - 1 downto 0 );
    signal barrel_shifter : barrel_shifter_type := ( others => ( others => '0' ) );
begin
    shift: process ( input ) is
    begin
        for i in size-1 downto 0 loop
            barrel_shifter( i ) <= std_logic_vector( resize( signed( input( WIDTH - 1 downto i ) ),
output'length ) );
        end loop;
    end process;

    output <= barrel_shifter( to_integer( unsigned( n ) ) );
end ndv;

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-- *****
-- **** STUDENT: 64200385
-- *****
-- KOMENTARJI K OCENI NALOGE
-- Matej Možek: Ni pripomb
-- *****

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library ieee;
use ieee.std_logic_1164.all;
use IEEE.numeric_std.all;
use WORK.cordic_pkg.all;

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ENTITY barrel_shifter_sra IS
    GENERIC(
        width : integer := 32;
        size : integer := 32
    );
    PORT(
        input : IN std_logic_vector ( WIDTH-1 DOWNT0 0 );
        output : OUT std_logic_vector ( WIDTH-1 DOWNT0 0 );
        n : IN std_logic_vector ( sizeof( size - 1 ) - 1 DOWNT0 0 )
    );
END barrel_shifter_sra;

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architecture ndv of barrel_shifter_sra is

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    type barrel_shifter_type is array ( 0 to size - 1 ) of std_logic_vector ( width - 1 downto 0 );
    signal barrel_shifter : barrel_shifter_type := ( others => ( others => '0' ) );
begin

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    barrelshifts: process( input ) is
    begin
        for i in 0 to size - 1 loop
            barrel_shifter( i )      <= std_logic_vector( resize( signed( input( width - 1 downto i ) ), output'length ) );
        end loop;
    end process;

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    output      <= barrel_shifter( to_integer( unsigned( n ) ) );
end ndv;

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-- *****
-- **** STUDENT: 64210132
-- *****
-- KOMENTARJI K OCENI NALOGE
-- Matej Možek: Ni pripomb
-- *****

library ieee;
use ieee.std_logic_1164.all;
use IEEE.numeric_std.all;
use WORK.cordic_pkg.all;

ENTITY barrel_shifter_sra IS
    GENERIC(
        width : integer := 32;
        size : integer := 32
    );
    PORT(
        input : IN std_logic_vector ( WIDTH-1 DOWNT0 0 );
        output : OUT std_logic_vector ( WIDTH-1 DOWNT0 0 );
        n : IN std_logic_vector ( sizeof( size - 1 ) - 1 DOWNT0 0 )
    );
END barrel_shifter_sra;

architecture ndv of barrel_shifter_sra is
    type barrel_shifter_type is array ( 0 to size - 1 ) of std_logic_vector ( width - 1 downto 0 );
    signal barrel_shifter : barrel_shifter_type := ( others => ( others => '0' ) );
begin

    P1: process ( input ) is
    begin
        for i in size-1 downto 0 loop
            barrel_shifter( i ) <= std_logic_vector( resize( signed( input( WIDTH - 1 downto i ) ),
output'length ) );
        end loop;
    end process;

    output <= barrel_shifter( to_integer( unsigned( n ) ) );

end ndv;

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-- *****
-- **** STUDENT: 64210290
-- *****
-- KOMENTARJI K OCENI NALOGE
-- Matej Možek: Ni pripomb
-- *****

LIBRARY ieee;
USE ieee.std_logic_1164.all;
USE IEEE.numeric_std.all;
USE WORK.cordic_pkg.all;

ENTITY barrel_shifter_sra IS
    GENERIC(
        width : INTEGER:= 32;
        size : INTEGER:= 32
    );
    PORT(
        input : IN STD_LOGIC_VECTOR ( WIDTH-1 DOWNT0 0 );
        output : OUT STD_LOGIC_VECTOR ( WIDTH-1 DOWNT0 0 );
        n : IN STD_LOGIC_VECTOR ( sizeof( size - 1 ) - 1 DOWNT0 0 )
    );
END barrel_shifter_sra;

ARCHITECTURE ndv OF barrel_shifter_sra IS

    type barrel_shifter_type is array ( 0 to size - 1 ) of std_logic_vector ( width - 1 downto 0 );
    signal barrel_shifter : barrel_shifter_type := ( others => ( others => '0' ) );

BEGIN

    barrel_proc : process( input )
    begin
        for i in 0 to size-1 loop
            barrel_shifter( i ) <= std_logic_vector( resize( signed( input( width-1 downto i ) ),output'length
) );
        end loop;
    end process;

    output <= barrel_shifter( to_integer( unsigned( n ) ) );

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END ndv;
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-- *****
-- **** STUDENT: 64210382
-- *****
-- KOMENTARJI K OCENI NALOGE
-- Matej Možek: Ni pripomb
-- *****

library ieee;
use ieee.std_logic_1164.all;
use IEEE.numeric_std.all;
use WORK.cordic_pkg.all;

ENTITY barrel_shifter_sra IS
    GENERIC(
        width : integer := 32;
        size : integer := 32
    );
    PORT(
        input : IN std_logic_vector ( WIDTH-1 DOWNT0 0 );
        output : OUT std_logic_vector ( WIDTH-1 DOWNT0 0 );
        n : IN std_logic_vector ( sizeof( size - 1 ) - 1 DOWNT0 0 )
    );
END barrel_shifter_sra;

architecture ndv of barrel_shifter_sra is
    type barrel_shifter_type is array ( 0 to size - 1 ) of std_logic_vector ( width - 1 downto 0 );
    signal barrel_shifter : barrel_shifter_type := ( others => ( others => '0' ) );
begin
    shifts: process ( input ) is
        begin
            for i in size-1 downto 0 loop
                barrel_shifter( i ) <= std_logic_vector( resize( signed( input( WIDTH - 1 downto i ) ),
output'length ) );
            end loop;
        end process;

        output <= barrel_shifter( to_integer( unsigned( n ) ) );
    end ndv;

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-- *****
-- **** STUDENT: 64210384
-- *****
-- KOMENTARJI K OCENI NALOGE
-- Matej Možek: Ni pripomb
-- *****

library ieee;
use ieee.std_logic_1164.all;
use IEEE.numeric_std.all;
use WORK.cordic_pkg.all;

ENTITY barrel_shifter_sra IS
    GENERIC(
        width : integer := 32;
        size : integer := 32
    );
    PORT(
        input : IN std_logic_vector ( width-1 DOWNT0 0 );
        output : OUT std_logic_vector ( width-1 DOWNT0 0 );
        n : IN std_logic_vector ( sizeof( size - 1 ) - 1 DOWNT0 0 )
    );
END barrel_shifter_sra;

architecture ndv of barrel_shifter_sra is
    type barrel_shifter_type is array ( 0 to size - 1 ) of std_logic_vector ( width - 1 downto 0 );
    signal barrel_shifter : barrel_shifter_type := ( others => ( others => '0' ) );
begin
    shifts: process ( input ) is
    begin
        for i in size-1 downto 0 loop
            barrel_shifter( i ) <= std_logic_vector( resize( signed( input( width - 1 downto i ) ),
output'length ) );
        end loop;
    end process;
    output <= barrel_shifter( to_integer( unsigned( n ) ) );
end ndv;

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-- *****
-- **** STUDENT: 64210445
-- *****
-- KOMENTARJI K OCENI NALOGE
-- Matej Možek: Ni pripomb
-- *****

library ieee;
use ieee.std_logic_1164.all;
use IEEE.numeric_std.all;
use WORK.cordic_pkg.all;

ENTITY barrel_shifter_sra IS
    GENERIC(
        width : integer := 32;
        size : integer := 32
    );
    PORT(
        input : IN std_logic_vector ( WIDTH-1 DOWNT0 0 );
        output : OUT std_logic_vector ( WIDTH-1 DOWNT0 0 );
        n : IN std_logic_vector ( sizeof( size - 1 ) - 1 DOWNT0 0 )
    );
END barrel_shifter_sra;

architecture ndv of barrel_shifter_sra is
    type barrel_shifter_type is array ( 0 to size - 1 ) of std_logic_vector ( width - 1 downto 0 );
    signal barrel_shifter : barrel_shifter_type := ( others => ( others => '0' ) );
begin

    shifts: process ( input ) is
    begin
        for i in size-1 downto 0 loop
            barrel_shifter( i ) <= std_logic_vector( resize( signed( input( WIDTH - 1 downto i ) ),
output'length ) );
        end loop;
    end process;

    output <= barrel_shifter( to_integer( unsigned( n ) ) );

end ndv;

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-- *****
-- **** STUDENT: 64210455
-- *****
-- KOMENTARJI K OCENI NALOGE
-- Matej Možek: Ni pripomb
-- *****

library ieee;
use ieee.std_logic_1164.all;
use IEEE.numeric_std.all;
use WORK.cordic_pkg.all;

ENTITY barrel_shifter_sra IS
    GENERIC(
        width : integer := 32;
        size : integer := 32
    );
    PORT(
        input : IN std_logic_vector ( WIDTH-1 DOWNT0 0 );
        output : OUT std_logic_vector ( WIDTH-1 DOWNT0 0 );
        n : IN std_logic_vector ( sizeof( size - 1 ) - 1 DOWNT0 0 )
    );
END barrel_shifter_sra;

architecture ndv of barrel_shifter_sra is

type barrel_shifter_type is array ( 0 to size - 1 ) of std_logic_vector ( width - 1 downto 0 );
signal barrel_shifter : barrel_shifter_type := ( others => ( others => '0' ) );
begin
    b_s: process( input ) is
    begin
        for i in 0 to size - 1 loop
            barrel_shifter( i ) <= std_logic_vector( resize( signed( input( width - 1 downto i ) ),
output'length ) );
        end loop;
    end process;

    output <= barrel_shifter( to_integer( unsigned( n ) ) );
end ndv;

```

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-- *****
-- **** STUDENT: 64210457
-- *****
-- KOMENTARJI K OCENI NALOGE
-- Matej Možek: Ni pripomb
-- *****

library ieee;
use ieee.std_logic_1164.all;
use IEEE.numeric_std.all;
use WORK.cordic_pkg.all;

ENTITY barrel_shifter_sra IS
    GENERIC(
        width : integer := 32;
        size : integer := 32
    );
    PORT(
        input : IN std_logic_vector ( WIDTH-1 DOWNT0 0 );
        output : OUT std_logic_vector ( WIDTH-1 DOWNT0 0 );
        n : IN std_logic_vector ( sizeof( size - 1 ) - 1 DOWNT0 0 )
    );
END barrel_shifter_sra;

architecture ndv of barrel_shifter_sra is
    type barrel_shifter_type is array ( 0 to size - 1 ) of std_logic_vector ( width - 1 downto 0 );
    signal barrel_shifter : barrel_shifter_type := ( others => ( others => '0' ) );
begin
    shifts: process ( input ) is
    begin
        for i in size-1 downto 0 loop
            barrel_shifter( i ) <= std_logic_vector( resize( signed( input( WIDTH - 1 downto i ) ),
output'length ) );
        end loop;
    end process;

    output <= barrel_shifter( to_integer( unsigned( n ) ) );
end ndv;

```

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-- *****
-- **** PREDLOGA VAJE
-- *****
-- KOMENTARJI K OCENI NALOGE
-- Matej Možek: Ni pripomb
-- *****

library ieee;
use ieee.std_logic_1164.all;
use IEEE.numeric_std.all;
use WORK.cordic_pkg.all;

ENTITY barrel_shifter_sra IS
    GENERIC(
        width : integer := 32;
        size : integer := 32
    );
    PORT(
        input : IN std_logic_vector ( WIDTH-1 DOWNT0 0 );
        output : OUT std_logic_vector ( WIDTH-1 DOWNT0 0 );
        n : IN std_logic_vector ( sizeof( size - 1 ) - 1 DOWNT0 0 )
    );
END barrel_shifter_sra;

architecture ndv of barrel_shifter_sra is
    type barrel_shifter_type is array ( 0 to size - 1 ) of std_logic_vector ( width - 1 downto 0 );
    signal barrel_shifter : barrel_shifter_type := ( others => ( others => '0' ) );

begin
    process( input )
    begin
        for i in size-1 downto 0 loop
            barrel_shifter( i ) <= std_logic_vector( resize( signed( input( WIDTH - 1 downto i ) ),
output'length ) );
        end loop;
    end process;

    output <= barrel_shifter( to_integer( unsigned( n ) ) );    -- bus demultiplexer

end ndv;

```

