

>xst -fih barrel_shifter_sra.xst	>xst -fih barrel_shifter_sra.xst
Release 14.7 - xst P.20131013 (m64)	Release 14.7 - xst P.20131013 (m64)
Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.	Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.
-> Parameter TMPDIR set to /xst/proj/nar/tmp	-> Parameter TMPDIR set to /xst/proj/nar/tmp
Total REAL time to Xst completion: 2.58 secs	Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 1.42 secs	Total CPU time to Xst completion: 0.23 secs
-> WARNING:Xst:3164 - Option "-debug" found multiple times in the command line. Only the first occurrence is considered.	-> WARNING:Xst:3164 - Option "-debug" found multiple times in the command line. Only the first occurrence is considered.
HDL Compiler	HDL Compiler
Compiling vhdl file "C:\vhdl\NDV_DN\2024\08_CORDIC\STUDENT\IBARREL_SHIFTER_SRA\cordic_pk4.vhd" in Library isim temp.	Compiling vhdl file "C:\vhdl\NDV_DN\2024\08_CORDIC\STUDENT\IBARREL_SHIFTER_SRA\cordic_pk4.vhd" in Library isim temp.
Package <cordic_pk4> compiled.	Package <cordic_pk4> compiled.
Package body <cordic_pk4> compiled.	Package body <cordic_pk4> compiled.
Compiling vhdl file "C:\vhdl\NDV_DN\2024\08_CORDIC\STUDENT\IBARREL_SHIFTER_SRA\barrel_shifter_sra.vhd" in Library isim temp.	Compiling vhdl file "C:\vhdl\NDV_DN\2024\08_CORDIC\STUDENT\IBARREL_SHIFTER_SRA\barrel_shifter_sra.vhd" in Library isim temp.
Entity <barrel_shifter_sra> compiled.	Entity <barrel_shifter_sra> compiled.
Entity <barrel_shifter_sra> (Architecture <ndy>) compiled.	Entity <barrel_shifter_sra> (Architecture <ndy>) compiled.
Total REAL time to Xst completion: 4.59 secs	Total REAL time to Xst completion: 2.00 secs
Total CPU time to Xst completion: 3.49 secs	Total CPU time to Xst completion: 1.52 secs
->	->
Total memory usage is 4477155 kilobytes	Total memory usage is 4477172 kilobytes
Number of errors : 0 (0 filtered)	Number of errors : 0 (0 filtered)
Number of warnings : 1 (0 filtered)	Number of warnings : 1 (0 filtered)
Number of infos : 0 (0 filtered)	Number of infos : 0 (0 filtered)
>fuse -incremental -o barrel_shifter_sra_tb.isim beh.exe -prj barrel_shifter_sra_tb.prj -top barrel_shifter_sra_tb	>fuse -incremental -o barrel_shifter_sra_tb.isim beh.exe -prj barrel_shifter_sra_tb.prj -top barrel_shifter_sra_tb
(Sim P.20131013 (signature 0x708090))	(Sim P.20131013 (signature 0x708090))
Number of CPUs detected in this system: 8	Number of CPUs detected in this system: 8
Turning on multi-threading, number of parallel sub-compilation jobs: 16	Turning on multi-threading, number of parallel sub-compilation jobs: 16
Determining compilation order of HDL files	Determining compilation order of HDL files
Parsing VHDL file "cordic_pk4.vhd" into library work	Parsing VHDL file "cordic_pk4.vhd" into library work
Parsing VHDL file "barrel_shifter_sra.vhd" into library work	Parsing VHDL file "barrel_shifter_sra.vhd" into library work
Parsing VHDL file "barrel_shifter_sra_tb.vhd" into library work	Parsing VHDL file "barrel_shifter_sra_tb.vhd" into library work
Starting static elaboration	Starting static elaboration
Completed static elaboration	Completed static elaboration
Compiling package standard	Compiling package standard
Compiling package textio	Compiling package textio
Compiling package std_logic_1164	Compiling package std_logic_1164
Compiling package numeric_std	Compiling package numeric_std
Compiling package cordic_pk4	Compiling package cordic_pk4
Compiling package math_real	Compiling package math_real
Compiling package std_logic_textio	Compiling package std_logic_textio
Compiling architecture ndy of entity barrel_shifter_sra [barrel_shifter_sra(32,32)]	Compiling architecture ndy of entity barrel_shifter_sra [barrel_shifter_sra(32,32)]
Compiling architecture rtl of entity barrel_shifter_sra_tb	Compiling architecture rtl of entity barrel_shifter_sra_tb
Time Resolution for simulation is 1ps	Time Resolution for simulation is 1ps
Waiting for 1 sub-compilation(s) to finish...	Waiting for 1 sub-compilation(s) to finish...
Compiled to VHDL Units	Compiled to VHDL Units
Built simulation executable barrel_shifter_sra_tb.isim_beh.exe	Built simulation executable barrel_shifter_sra_tb.isim_beh.exe
Fuse Memory Usage: 37008 KB	Fuse Memory Usage: 37580 KB
Fuse CPU Usage: 937 ms	Fuse CPU Usage: 875 ms
>barrel_shifter_sra_tb.isim beh.exe -icbatch isim.tcl -wdb barrel_shifter_sra_tb.isim_beh.wdb	>barrel_shifter_sra_tb.isim beh.exe -icbatch isim.tcl -wdb barrel_shifter_sra_tb.isim_beh.wdb
(Sim P.20131013 (signature 0x708090))	(Sim P.20131013 (signature 0x708090))
WARNING: A WERPACK license was found.	WARNING: A WERPACK license was found.
WARNING: Please use Xilinx License Configuration Manager to check out a full ISim license.	WARNING: Please use Xilinx License Configuration Manager to check out a full ISim license.
WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for more information on the differences between the Lite and the Full version.	WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for more information on the differences between the Lite and the Full version.
This is a Lite version of ISim.	This is a Lite version of ISim.
Time resolution is 1 ps	Time resolution is 1 ps
Simulator is doing circuit initialization process.	Simulator is doing circuit initialization process.
Finished circuit initialization process.	Finished circuit initialization process.

>xel -fh barrel_shifter.sra.xst		>xel -fh barrel_shifter.sra.xst	
Release 14.7 - xel P.20131013 (n164)		Release 14.7 - xel P.20131013 (n164)	
Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.		Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.	
-> Parameter TMPDIR set to /xstprojav/tmp		-> Parameter TMPDIR set to /xstprojav/tmp	
Total REAL time to Xst completion: 0.00 secs		Total REAL time to Xst completion: 0.00 secs	
Total CPU time to Xst completion: 0.25 secs		Total CPU time to Xst completion: 0.23 secs	
-> WARNING: Xst:3164 - Option "-debug" found multiple times in the command line. Only the first occurrence is considered.		-> WARNING: Xst:3164 - Option "-debug" found multiple times in the command line. Only the first occurrence is considered.	
+ HDL Compilation		+ HDL Compilation	
Compiling vhdl file "C:\vhdl\NDV_DN\2024\08_CORDIC\STUDENT\BARREL_SHIFTER_SRA\cordic_pkq.vhd" in Library isim_temp.		Compiling vhdl file "C:\vhdl\NDV_DN\2024\08_CORDIC\STUDENT\BARREL_SHIFTER_SRA\cordic_pkq.vhd" in Library isim_temp.	
Package <cordic_pkq> compiled.		Package <cordic_pkq> compiled.	
Package body <cordic_pkq> compiled.		Package body <cordic_pkq> compiled.	
Compiling vhdl file "C:\vhdl\NDV_DN\2024\08_CORDIC\STUDENT\BARREL_SHIFTER_SRA\barrel_shifter.sra.vhd" in Library isim_temp.		Compiling vhdl file "C:\vhdl\NDV_DN\2024\08_CORDIC\STUDENT\BARREL_SHIFTER_SRA\barrel_shifter.sra.vhd" in Library isim_temp.	
Entity <barrel_shifter.sra> compiled.		Entity <barrel_shifter.sra> compiled.	
Entity <barrel_shifter.sra> (Architecture <ndy>) compiled.		Entity <barrel_shifter.sra> (Architecture <ndy>) compiled.	
Total REAL time to Xst completion: 1.00 secs		Total REAL time to Xst completion: 2.00 secs	
Total CPU time to Xst completion: 9.37 secs		Total CPU time to Xst completion: 1.52 secs	
->		->	
Total memory usage is 4477164 kilobytes		Total memory usage is 4477172 kilobytes	
Number of errors : 0 (0 filtered)		Number of errors : 0 (0 filtered)	
Number of warnings : 1 (0 filtered)		Number of warnings : 1 (0 filtered)	
Number of infos : 0 (0 filtered)		Number of infos : 0 (0 filtered)	
+Use incremental -o barrel_shifter.sra.tb.isim_beh.exe -pri barrel_shifter.sra.tb.pri_top barrel_shifter.sra.tb		+Use incremental -o barrel_shifter.sra.tb.isim_beh.exe -pri barrel_shifter.sra.tb.pri_top barrel_shifter.sra.tb	
(Isim P.20131013 (signature 0x7708090))		(Isim P.20131013 (signature 0x7708090))	
Number of CPUs detected in this system: 8		Number of CPUs detected in this system: 8	
Turning on multi-threading, number of parallel sub-compilation jobs: 16		Turning on multi-threading, number of parallel sub-compilation jobs: 16	
Determining compilation order of HDL files		Determining compilation order of HDL files	
Parsing VHDL file "cordic_pkq.vhd" into library work		Parsing VHDL file "cordic_pkq.vhd" into library work	
Parsing VHDL file "barrel_shifter.sra.vhd" into library work		Parsing VHDL file "barrel_shifter.sra.vhd" into library work	
Parsing VHDL file "barrel_shifter.sra.tb.vhd" into library work		Parsing VHDL file "barrel_shifter.sra.tb.vhd" into library work	
Starting static elaboration		Starting static elaboration	
Completed static elaboration		Completed static elaboration	
Compiling package standard		Compiling package standard	
Compiling package textio		Compiling package textio	
Compiling package std_logic_1164		Compiling package std_logic_1164	
Compiling package numeric_std		Compiling package numeric_std	
Compiling package cordic_pkq		Compiling package cordic_pkq	
Compiling package math_real		Compiling package math_real	
Compiling package std_logic_textio		Compiling package std_logic_textio	
Compiling architecture ndv of entity barrel_shifter.sra (barrel_shifter.sra(32,32))		Compiling architecture ndv of entity barrel_shifter.sra (barrel_shifter.sra(32,32))	
Compiling architecture tl of entity barrel_shifter.sra.tb		Compiling architecture tl of entity barrel_shifter.sra.tb	
Time Resolution for simulation is 1ps.		Time Resolution for simulation is 1ps.	
Compiled 10 VHDL Units		Waiting for 1 sub-compilation(s) to finish.	
Built simulation executable barrel_shifter.sra.tb.isim_beh.exe		Compiled 10 VHDL Units	
Fuse Memory Usage: 37320 KB		Built simulation executable barrel_shifter.sra.tb.isim_beh.exe	
Fuse CPU Usage: 921 ms		Fuse Memory Usage: 37580 KB	
-barrel_shifter.sra.tb.isim_beh.exe -clbatch isim.tcl -wdb barrel_shifter.sra.tb.isim_beh.wdb		Fuse CPU Usage: 875 ms	
(Isim P.20131013 (signature 0x7708090))		-barrel_shifter.sra.tb.isim_beh.exe -clbatch isim.tcl -wdb barrel_shifter.sra.tb.isim_beh.wdb	
WARNING: A WEBPACK license was found.		(Isim P.20131013 (signature 0x7708090))	
WARNING: Please use Xilinx License Configuration Manager to check out a full ISim license.		WARNING: A WEBPACK license was found.	
WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for more information on the differences between the Lite and the Full version.		WARNING: Please use Xilinx License Configuration Manager to check out a full ISim license.	
This is a Lite version of ISim.		WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for more information on the differences between the Lite and the Full version.	
Time resolution is 1 ps		This is a Lite version of ISim.	
Simulator is doing circuit initialization process.		Time resolution is 1 ps	
Finished circuit initialization process.		Simulator is doing circuit initialization process.	
		Finished circuit initialization process.	

>xst -fih barrel_shifter_sra.xst	>xst -fih barrel_shifter_sra.xst
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Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.	Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.
-> Parameter TMPDIR set to /xst/proj/nar/tmp	-> Parameter TMPDIR set to /xst/proj/nar/tmp
Total REAL time to Xst completion: 0.00 secs	Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.23 secs	Total CPU time to Xst completion: 0.23 secs
-> WARNING:Xst:3164 - Option "-debug" found multiple times in the command line. Only the first occurrence is considered.	-> WARNING:Xst:3164 - Option "-debug" found multiple times in the command line. Only the first occurrence is considered.
HDL Compiler	HDL Compiler
Compiling vhdl file "C:\vhdl\NDV_DN\2024\08_CORDIC\STUDENT\IBARREL_SHIFTER_SRA\cordic_pkq.vhd" in Library isim temp.	Compiling vhdl file "C:\vhdl\NDV_DN\2024\08_CORDIC\STUDENT\IBARREL_SHIFTER_SRA\cordic_pkq.vhd" in Library isim temp.
Package <cordic_pkq> compiled.	Package <cordic_pkq> compiled.
Package body <cordic_pkq> compiled.	Package body <cordic_pkq> compiled.
Compiling vhdl file "C:\vhdl\NDV_DN\2024\08_CORDIC\STUDENT\IBARREL_SHIFTER_SRA\barrel_shifter_sra.vhd" in Library isim temp.	Compiling vhdl file "C:\vhdl\NDV_DN\2024\08_CORDIC\STUDENT\IBARREL_SHIFTER_SRA\barrel_shifter_sra.vhd" in Library isim temp.
Entity <barrel_shifter_sra> compiled.	Entity <barrel_shifter_sra> compiled.
Entity <barrel_shifter_sra> (Architecture <ndy>) compiled.	Entity <barrel_shifter_sra> (Architecture <ndy>) compiled.
Total REAL time to Xst completion: 0.00 secs	Total REAL time to Xst completion: 2.00 secs
Total CPU time to Xst completion: 0.33 secs	Total CPU time to Xst completion: 1.52 secs
->	->
Total memory usage is 4477136 kilobytes	Total memory usage is 4477172 kilobytes
Number of errors : 0 (0 filtered)	Number of errors : 0 (0 filtered)
Number of warnings : 1 (0 filtered)	Number of warnings : 1 (0 filtered)
Number of infos : 0 (0 filtered)	Number of infos : 0 (0 filtered)
>fuse -incremental -o barrel_shifter_sra_tb.isim beh.exe -prj barrel_shifter_sra_tb.prj -top barrel_shifter_sra_tb	>fuse -incremental -o barrel_shifter_sra_tb.isim beh.exe -prj barrel_shifter_sra_tb.prj -top barrel_shifter_sra_tb
(Sim P.20131013 (signature 0x708090))	(Sim P.20131013 (signature 0x708090))
Number of CPUs detected in this system: 8	Number of CPUs detected in this system: 8
Turning on multi-threading, number of parallel sub-compilation jobs: 16	Turning on multi-threading, number of parallel sub-compilation jobs: 16
Determining compilation order of HDL files	Determining compilation order of HDL files
Parsing VHDL file "cordic_pkq.vhd" into library work	Parsing VHDL file "cordic_pkq.vhd" into library work
Parsing VHDL file "barrel_shifter_sra.vhd" into library work	Parsing VHDL file "barrel_shifter_sra.vhd" into library work
Parsing VHDL file "barrel_shifter_sra_tb.vhd" into library work	Parsing VHDL file "barrel_shifter_sra_tb.vhd" into library work
Starting static elaboration	Starting static elaboration
Completed static elaboration	Completed static elaboration
Compiling package standard	Compiling package standard
Compiling package textio	Compiling package textio
Compiling package std_logic_1164	Compiling package std_logic_1164
Compiling package numeric_std	Compiling package numeric_std
Compiling package cordic_pkq	Compiling package cordic_pkq
Compiling package math_real	Compiling package math_real
Compiling package std_logic_textio	Compiling package std_logic_textio
Compiling architecture ndy of entity barrel_shifter_sra [barrel_shifter_sra(32,32)]	Compiling architecture ndy of entity barrel_shifter_sra [barrel_shifter_sra(32,32)]
Compiling architecture rtl of entity barrel_shifter_sra_tb	Compiling architecture rtl of entity barrel_shifter_sra_tb
Time Resolution for simulation is 1ps	Time Resolution for simulation is 1ps
Waiting for 1 sub-compilation(s) to finish...	Waiting for 1 sub-compilation(s) to finish...
Compiled to VHDL Units	Compiled to VHDL Units
Built simulation executable barrel_shifter_sra_tb.isim_beh.exe	Built simulation executable barrel_shifter_sra_tb.isim_beh.exe
Fuse Memory Usage: 37372 KB	Fuse Memory Usage: 37580 KB
Fuse CPU Usage: 874 ms	Fuse CPU Usage: 875 ms
>barrel_shifter_sra_tb.isim beh.exe -icbatch isim.tcl -wdb barrel_shifter_sra_tb.isim_beh.wdb	>barrel_shifter_sra_tb.isim beh.exe -icbatch isim.tcl -wdb barrel_shifter_sra_tb.isim_beh.wdb
(Sim P.20131013 (signature 0x708090))	(Sim P.20131013 (signature 0x708090))
WARNING: A WERPACK license was found.	WARNING: A WERPACK license was found.
WARNING: Please use Xilinx License Configuration Manager to check out a full ISim license.	WARNING: Please use Xilinx License Configuration Manager to check out a full ISim license.
WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for more information on the differences between the Lite and the Full version.	WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for more information on the differences between the Lite and the Full version.
This is a Lite version of ISim.	This is a Lite version of ISim.
Time resolution is 1 ps	Time resolution is 1 ps
Simulator is doing circuit initialization process.	Simulator is doing circuit initialization process.
Finished circuit initialization process.	Finished circuit initialization process.

>xst -fih barrel_shifter_sra.xst	>xst -fih barrel_shifter_sra.xst
Release 14.7 - xst P.20131013 (m64)	Release 14.7 - xst P.20131013 (m64)
Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.	Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.
-> Parameter TMPDIR set to /xst/proj/nar/tmp	-> Parameter TMPDIR set to /xst/proj/nar/tmp
Total REAL time to Xst completion: 0.00 secs	Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.23 secs	Total CPU time to Xst completion: 0.23 secs
-> WARNING:Xst:3164 - Option "-debug" found multiple times in the command line. Only the first occurrence is considered.	-> WARNING:Xst:3164 - Option "-debug" found multiple times in the command line. Only the first occurrence is considered.
HDL Compiler	HDL Compiler
Compiling vhdl file "C:\vhdl\NDV_DN\2024\08_CORDIC\STUDENT\IBARREL_SHIFTER_SRA\cordic_pkq.vhd" in Library isim temp.	Compiling vhdl file "C:\vhdl\NDV_DN\2024\08_CORDIC\STUDENT\IBARREL_SHIFTER_SRA\cordic_pkq.vhd" in Library isim temp.
Package <cordic_pkq> compiled.	Package <cordic_pkq> compiled.
Package body <cordic_pkq> compiled.	Package body <cordic_pkq> compiled.
Compiling vhdl file "C:\vhdl\NDV_DN\2024\08_CORDIC\STUDENT\IBARREL_SHIFTER_SRA\barrel_shifter_sra.vhd" in Library isim temp.	Compiling vhdl file "C:\vhdl\NDV_DN\2024\08_CORDIC\STUDENT\IBARREL_SHIFTER_SRA\barrel_shifter_sra.vhd" in Library isim temp.
Entity <barrel_shifter_sra> compiled.	Entity <barrel_shifter_sra> compiled.
Entity <barrel_shifter_sra> (Architecture <ndy>) compiled.	Entity <barrel_shifter_sra> (Architecture <ndy>) compiled.
Total REAL time to Xst completion: 0.00 secs	Total REAL time to Xst completion: 2.00 secs
Total CPU time to Xst completion: 0.32 secs	Total CPU time to Xst completion: 1.52 secs
->	->
Total memory usage is 4477184 kilobytes	Total memory usage is 4477172 kilobytes
Number of errors : 0 (0 filtered)	Number of errors : 0 (0 filtered)
Number of warnings : 1 (0 filtered)	Number of warnings : 1 (0 filtered)
Number of infos : 0 (0 filtered)	Number of infos : 0 (0 filtered)
>fuse -incremental -o barrel_shifter_sra_tb.isim beh.exe -prj barrel_shifter_sra_tb.prj -top barrel_shifter_sra_tb	>fuse -incremental -o barrel_shifter_sra_tb.isim beh.exe -prj barrel_shifter_sra_tb.prj -top barrel_shifter_sra_tb
(Sim P.20131013 (signature 0x708090))	(Sim P.20131013 (signature 0x708090))
Number of CPUs detected in this system: 8	Number of CPUs detected in this system: 8
Turning on multi-threading, number of parallel sub-compilation jobs: 16	Turning on multi-threading, number of parallel sub-compilation jobs: 16
Determining compilation order of HDL files	Determining compilation order of HDL files
Parsing VHDL file "cordic_pkq.vhd" into library work	Parsing VHDL file "cordic_pkq.vhd" into library work
Parsing VHDL file "barrel_shifter_sra.vhd" into library work	Parsing VHDL file "barrel_shifter_sra.vhd" into library work
Parsing VHDL file "barrel_shifter_sra_tb.vhd" into library work	Parsing VHDL file "barrel_shifter_sra_tb.vhd" into library work
Starting static elaboration	Starting static elaboration
Completed static elaboration	Completed static elaboration
Compiling package standard	Compiling package standard
Compiling package textio	Compiling package textio
Compiling package std_logic_1164	Compiling package std_logic_1164
Compiling package numeric_std	Compiling package numeric_std
Compiling package cordic_pkq	Compiling package cordic_pkq
Compiling package math_real	Compiling package math_real
Compiling package std_logic_textio	Compiling package std_logic_textio
Compiling architecture ndy of entity barrel_shifter_sra [barrel_shifter_sra(32,32)]	Compiling architecture ndy of entity barrel_shifter_sra [barrel_shifter_sra(32,32)]
Compiling architecture rtl of entity barrel_shifter_sra_tb	Compiling architecture rtl of entity barrel_shifter_sra_tb
Time Resolution for simulation is 1ps	Time Resolution for simulation is 1ps
Waiting for 1 sub-compilation(s) to finish...	Waiting for 1 sub-compilation(s) to finish...
Compiled to VHDL Units	Compiled to VHDL Units
Built simulation executable barrel_shifter_sra_tb.isim_beh.exe	Built simulation executable barrel_shifter_sra_tb.isim_beh.exe
Fuse Memory Usage: 37400 KB	Fuse Memory Usage: 37580 KB
Fuse CPU Usage: 899 ms	Fuse CPU Usage: 875 ms
>barrel_shifter_sra_tb.isim beh.exe -icbatch isim.tcl -wdb barrel_shifter_sra_tb.isim_beh.wdb	>barrel_shifter_sra_tb.isim beh.exe -icbatch isim.tcl -wdb barrel_shifter_sra_tb.isim_beh.wdb
(Sim P.20131013 (signature 0x708090))	(Sim P.20131013 (signature 0x708090))
WARNING: A WERPACK license was found.	WARNING: A WERPACK license was found.
WARNING: Please use Xilinx License Configuration Manager to check out a full ISim license.	WARNING: Please use Xilinx License Configuration Manager to check out a full ISim license.
WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for more information on the differences between the Lite and the Full version.	WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for more information on the differences between the Lite and the Full version.
This is a Lite version of ISim.	This is a Lite version of ISim.
Time resolution is 1 ps	Time resolution is 1 ps
Simulator is doing circuit initialization process.	Simulator is doing circuit initialization process.
Finished circuit initialization process.	Finished circuit initialization process.

>xst -fih barrel_shifter_sra.xst	>xst -fih barrel_shifter_sra.xst
Release 14.7 - xst P.20131013 (m64)	Release 14.7 - xst P.20131013 (m64)
Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.	Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.
-> Parameter TMPDIR set to /xst/proj/nar/tmp	-> Parameter TMPDIR set to /xst/proj/nar/tmp
Total REAL time to Xst completion: 1.88 secs	Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.24 secs	Total CPU time to Xst completion: 0.23 secs
-> WARNING:Xst:3164 - Option "-debug" found multiple times in the command line. Only the first occurrence is considered.	-> WARNING:Xst:3164 - Option "-debug" found multiple times in the command line. Only the first occurrence is considered.
HDL Compiler	HDL Compiler
Compiling vhdl file "C:\vhdl\NDV_DN\2024\08_CORDIC\STUDENT\IBARREL_SHIFTER_SRA\cordic_pk4.vhd" in Library isim temp.	Compiling vhdl file "C:\vhdl\NDV_DN\2024\08_CORDIC\STUDENT\IBARREL_SHIFTER_SRA\cordic_pk4.vhd" in Library isim temp.
Package <cordic_pk4> compiled.	Package <cordic_pk4> compiled.
Package body <cordic_pk4> compiled.	Package body <cordic_pk4> compiled.
Compiling vhdl file "C:\vhdl\NDV_DN\2024\08_CORDIC\STUDENT\IBARREL_SHIFTER_SRA\barrel_shifter_sra.vhd" in Library isim temp.	Compiling vhdl file "C:\vhdl\NDV_DN\2024\08_CORDIC\STUDENT\IBARREL_SHIFTER_SRA\barrel_shifter_sra.vhd" in Library isim temp.
Entity <barrel_shifter_sra> compiled.	Entity <barrel_shifter_sra> compiled.
Entity <barrel_shifter_sra> (Architecture <ndy>) compiled.	Entity <barrel_shifter_sra> (Architecture <ndy>) compiled.
Total REAL time to Xst completion: 1.88 secs	Total REAL time to Xst completion: 2.00 secs
Total CPU time to Xst completion: 0.73 secs	Total CPU time to Xst completion: 1.52 secs
->	->
Total memory usage is 4477145 kilobytes	Total memory usage is 4477172 kilobytes
Number of errors : 0 (0 filtered)	Number of errors : 0 (0 filtered)
Number of warnings : 1 (0 filtered)	Number of warnings : 1 (0 filtered)
Number of infos : 0 (0 filtered)	Number of infos : 0 (0 filtered)
>fuse -incremental -o barrel_shifter_sra_tb.isim beh.exe -prj barrel_shifter_sra_tb.prj -top barrel_shifter_sra_tb	>fuse -incremental -o barrel_shifter_sra_tb.isim beh.exe -prj barrel_shifter_sra_tb.prj -top barrel_shifter_sra_tb
(Sim P.20131013 (signature 0x708090))	(Sim P.20131013 (signature 0x708090))
Number of CPUs detected in this system: 8	Number of CPUs detected in this system: 8
Turning on multi-threading, number of parallel sub-compilation jobs: 16	Turning on multi-threading, number of parallel sub-compilation jobs: 16
Determining compilation order of HDL files	Determining compilation order of HDL files
Parsing VHDL file "cordic_pk4.vhd" into library work	Parsing VHDL file "cordic_pk4.vhd" into library work
Parsing VHDL file "barrel_shifter_sra.vhd" into library work	Parsing VHDL file "barrel_shifter_sra.vhd" into library work
Parsing VHDL file "barrel_shifter_sra_tb.vhd" into library work	Parsing VHDL file "barrel_shifter_sra_tb.vhd" into library work
Starting static elaboration	Starting static elaboration
Completed static elaboration	Completed static elaboration
Compiling package standard	Compiling package standard
Compiling package textio	Compiling package textio
Compiling package std_logic_1164	Compiling package std_logic_1164
Compiling package numeric_std	Compiling package numeric_std
Compiling package cordic_pk4	Compiling package cordic_pk4
Compiling package math_real	Compiling package math_real
Compiling package std_logic_textio	Compiling package std_logic_textio
Compiling architecture ndy of entity barrel_shifter_sra [barrel_shifter_sra(32,32)]	Compiling architecture ndy of entity barrel_shifter_sra [barrel_shifter_sra(32,32)]
Compiling architecture rtl of entity barrel_shifter_sra_tb	Compiling architecture rtl of entity barrel_shifter_sra_tb
Time Resolution for simulation is 1ps	Time Resolution for simulation is 1ps
Waiting for 1 sub-compilation(s) to finish...	Waiting for 1 sub-compilation(s) to finish...
Compiled to VHDL Units	Compiled to VHDL Units
Built simulation executable barrel_shifter_sra_tb.isim_beh.exe	Built simulation executable barrel_shifter_sra_tb.isim_beh.exe
Fuse Memory Usage: 37396 KB	Fuse Memory Usage: 37580 KB
Fuse CPU Usage: 921 ms	Fuse CPU Usage: 875 ms
>barrel_shifter_sra_tb.isim beh.exe -icbatch isim.tcl -wdb barrel_shifter_sra_tb.isim_beh.wdb	>barrel_shifter_sra_tb.isim beh.exe -icbatch isim.tcl -wdb barrel_shifter_sra_tb.isim_beh.wdb
(Sim P.20131013 (signature 0x708090))	(Sim P.20131013 (signature 0x708090))
WARNING: A WERPACK license was found.	WARNING: A WERPACK license was found.
WARNING: Please use Xilinx License Configuration Manager to check out a full ISim license.	WARNING: Please use Xilinx License Configuration Manager to check out a full ISim license.
WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for more information on the differences between the Lite and the Full version.	WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for more information on the differences between the Lite and the Full version.
This is a Lite version of ISim.	This is a Lite version of ISim.
Time resolution is 1 ps	Time resolution is 1 ps
Simulator is doing circuit initialization process.	Simulator is doing circuit initialization process.
Finished circuit initialization process.	Finished circuit initialization process.

>xel -fh barrel_shifter_sra.xst		>xel -fh barrel_shifter_sra.xst	
Release 14.7 - xel P.20131013 (n164)		Release 14.7 - xel P.20131013 (n164)	
Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.		Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.	
-> Parameter TMPDIR set to /xstprojdir/tmp		-> Parameter TMPDIR set to /xstprojdir/tmp	
Total REAL time to Xst completion: 0.00 secs		Total REAL time to Xst completion: 0.00 secs	
Total CPU time to Xst completion: 0.25 secs		Total CPU time to Xst completion: 0.23 secs	
-> WARNING:Xst:3164 - Option "-debug" found multiple times in the command line. Only the first occurrence is considered.		-> WARNING:Xst:3164 - Option "-debug" found multiple times in the command line. Only the first occurrence is considered.	
* HDL Compilation		* HDL Compilation	
Compiling vhdl file "C:\vhdl\NDV_DN\2024\08_CORDIC\STUDENT\BARREL_SHIFTER_SRA\cordic_pkq.vhd" in Library isim_temp.		Compiling vhdl file "C:\vhdl\NDV_DN\2024\08_CORDIC\STUDENT\BARREL_SHIFTER_SRA\cordic_pkq.vhd" in Library isim_temp.	
Package <cordic_pkq> compiled.		Package <cordic_pkq> compiled.	
Package body <cordic_pkq> compiled.		Package body <cordic_pkq> compiled.	
Compiling vhdl file "C:\vhdl\NDV_DN\2024\08_CORDIC\STUDENT\BARREL_SHIFTER_SRA\barrel_shifter_sra.vhd" in Library isim_temp.		Compiling vhdl file "C:\vhdl\NDV_DN\2024\08_CORDIC\STUDENT\BARREL_SHIFTER_SRA\barrel_shifter_sra.vhd" in Library isim_temp.	
Entity <barrel_shifter_sra> compiled.		Entity <barrel_shifter_sra> compiled.	
Entity <barrel_shifter_sra> (Architecture <ndy>) compiled.		Entity <barrel_shifter_sra> (Architecture <ndy>) compiled.	
Total REAL time to Xst completion: 1.00 secs		Total REAL time to Xst completion: 2.00 secs	
Total CPU time to Xst completion: 0.60 secs		Total CPU time to Xst completion: 1.52 secs	
->		->	
Total memory usage is 4477180 kilobytes		Total memory usage is 4477172 kilobytes	
Number of errors : 0 (0 filtered)		Number of errors : 0 (0 filtered)	
Number of warnings : 1 (0 filtered)		Number of warnings : 1 (0 filtered)	
Number of infos : 0 (0 filtered)		Number of infos : 0 (0 filtered)	
->Use incremental -o barrel_shifter_sra.tb.isim_beh.exe -pri barrel_shifter_sra.tb.pri -top barrel_shifter_sra.tb		->Use incremental -o barrel_shifter_sra.tb.isim_beh.exe -pri barrel_shifter_sra.tb.pri -top barrel_shifter_sra.tb	
(Isim P.20131013 (signature 0x7708090))		(Isim P.20131013 (signature 0x7708090))	
Number of CPUs detected in this system: 8		Number of CPUs detected in this system: 8	
Turning on multi-threading, number of parallel sub-compilation jobs: 16		Turning on multi-threading, number of parallel sub-compilation jobs: 16	
Determining compilation order of HDL files		Determining compilation order of HDL files	
Parsing VHDL file "cordic_pkq.vhd" into library work		Parsing VHDL file "cordic_pkq.vhd" into library work	
Parsing VHDL file "barrel_shifter_sra.vhd" into library work		Parsing VHDL file "barrel_shifter_sra.vhd" into library work	
Parsing VHDL file "barrel_shifter_sra.tb.vhd" into library work		Parsing VHDL file "barrel_shifter_sra.tb.vhd" into library work	
Starting static elaboration		Starting static elaboration	
Completed static elaboration		Completed static elaboration	
Compiling package standard		Compiling package standard	
Compiling package textio		Compiling package textio	
Compiling package std_logic_1164		Compiling package std_logic_1164	
Compiling package numeric_std		Compiling package numeric_std	
Compiling package cordic_pkq		Compiling package cordic_pkq	
Compiling package math_real		Compiling package math_real	
Compiling package std_logic_textio		Compiling package std_logic_textio	
Compiling architecture ndv of entity barrel_shifter_sra (barrel_shifter_sra(32,32))		Compiling architecture ndv of entity barrel_shifter_sra (barrel_shifter_sra(32,32))	
Compiling architecture tl of entity barrel_shifter_sra.tb		Compiling architecture tl of entity barrel_shifter_sra.tb	
Time Resolution for simulation is 1ps.		Time Resolution for simulation is 1ps.	
Compiled 10 VHDL Units		Waiting for 1 sub-compilation(s) to finish.	
Built simulation executable barrel_shifter_sra.tb.isim_beh.exe		Compiled 10 VHDL Units	
Fuse Memory Usage: 37300 KB		Built simulation executable barrel_shifter_sra.tb.isim_beh.exe	
Fuse CPU Usage: 906 ms		Fuse Memory Usage: 37580 KB	
-> barrel_shifter_sra.tb.isim_beh.exe -clbatch isim.tcl -wdb barrel_shifter_sra.tb.isim_beh.wdb		Fuse CPU Usage: 875 ms	
(Isim P.20131013 (signature 0x7708090))		-> barrel_shifter_sra.tb.isim_beh.exe -clbatch isim.tcl -wdb barrel_shifter_sra.tb.isim_beh.wdb	
WARNING: A WEBPACK license was found.		(Isim P.20131013 (signature 0x7708090))	
WARNING: Please use Xilinx License Configuration Manager to check out a full ISim license.		WARNING: A WEBPACK license was found.	
WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for more information on the differences between the Lite and the Full version.		WARNING: Please use Xilinx License Configuration Manager to check out a full ISim license.	
This is a Lite version of ISim.		WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for more information on the differences between the Lite and the Full version.	
Time resolution is 1 ps		This is a Lite version of ISim.	
Simulator is doing circuit initialization process.		Time resolution is 1 ps	
Finished circuit initialization process.		Simulator is doing circuit initialization process.	
		Finished circuit initialization process.	

>xst -fih barrel_shifter_sra.xst	>xst -fih barrel_shifter_sra.xst
Release 14.7 - xst P.20131013 (m64)	Release 14.7 - xst P.20131013 (m64)
Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.	Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.
-> Parameter TMPDIR set to /xst/proj/nav/tmp	-> Parameter TMPDIR set to /xst/proj/nav/tmp
Total REAL time to Xst completion: 1.88 secs	Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.76 secs	Total CPU time to Xst completion: 0.23 secs
-> WARNING:Xst:3164 - Option "-debug" found multiple times in the command line. Only the first occurrence is considered.	-> WARNING:Xst:3164 - Option "-debug" found multiple times in the command line. Only the first occurrence is considered.
HDL Compiler	HDL Compiler
Compiling vhdl file "C:\vhdl\NDV_DN\2024\08_CORDIC\STUDENT\IBARREL_SHIFTER_SRA\cordic_pkq.vhd" in Library isim temp.	Compiling vhdl file "C:\vhdl\NDV_DN\2024\08_CORDIC\STUDENT\IBARREL_SHIFTER_SRA\cordic_pkq.vhd" in Library isim temp.
Package <cordic_pkq> compiled.	Package <cordic_pkq> compiled.
Package body <cordic_pkq> compiled.	Package body <cordic_pkq> compiled.
Compiling vhdl file "C:\vhdl\NDV_DN\2024\08_CORDIC\STUDENT\IBARREL_SHIFTER_SRA\barrel_shifter_sra.vhd" in Library isim temp.	Compiling vhdl file "C:\vhdl\NDV_DN\2024\08_CORDIC\STUDENT\IBARREL_SHIFTER_SRA\barrel_shifter_sra.vhd" in Library isim temp.
Entity <barrel_shifter_sra> compiled.	Entity <barrel_shifter_sra> compiled.
Entity <barrel_shifter_sra> (Architecture <ndy>) compiled.	Entity <barrel_shifter_sra> (Architecture <ndy>) compiled.
Total REAL time to Xst completion: 2.00 secs	Total REAL time to Xst completion: 2.00 secs
Total CPU time to Xst completion: 1.97 secs	Total CPU time to Xst completion: 1.52 secs
->	->
Total memory usage is 4477164 kilobytes	Total memory usage is 4477172 kilobytes
Number of errors : 0 (0 filtered)	Number of errors : 0 (0 filtered)
Number of warnings : 1 (0 filtered)	Number of warnings : 1 (0 filtered)
Number of infos : 0 (0 filtered)	Number of infos : 0 (0 filtered)
>fuse -incremental -o barrel_shifter_sra_tb.isim beh.exe -prj barrel_shifter_sra_tb.prj -top barrel_shifter_sra_tb	>fuse -incremental -o barrel_shifter_sra_tb.isim beh.exe -prj barrel_shifter_sra_tb.prj -top barrel_shifter_sra_tb
(Sim P.20131013 (signature 0x708090))	(Sim P.20131013 (signature 0x708090))
Number of CPUs detected in this system: 8	Number of CPUs detected in this system: 8
Turning on multi-threading, number of parallel sub-compilation jobs: 16	Turning on multi-threading, number of parallel sub-compilation jobs: 16
Determining compilation order of HDL files	Determining compilation order of HDL files
Parsing VHDL file "cordic_pkq.vhd" into library work	Parsing VHDL file "cordic_pkq.vhd" into library work
Parsing VHDL file "barrel_shifter_sra.vhd" into library work	Parsing VHDL file "barrel_shifter_sra.vhd" into library work
Parsing VHDL file "barrel_shifter_sra_tb.vhd" into library work	Parsing VHDL file "barrel_shifter_sra_tb.vhd" into library work
Starting static elaboration	Starting static elaboration
Completed static elaboration	Completed static elaboration
Compiling package standard	Compiling package standard
Compiling package textio	Compiling package textio
Compiling package std_logic_1164	Compiling package std_logic_1164
Compiling package numeric_std	Compiling package numeric_std
Compiling package cordic_pkq	Compiling package cordic_pkq
Compiling package math_real	Compiling package math_real
Compiling package std_logic_textio	Compiling package std_logic_textio
Compiling architecture ndy of entity barrel_shifter_sra [barrel_shifter_sra(32.32)]	Compiling architecture ndy of entity barrel_shifter_sra [barrel_shifter_sra(32.32)]
Compiling architecture rtl of entity barrel_shifter_sra_tb	Compiling architecture rtl of entity barrel_shifter_sra_tb
Time Resolution for simulation is 1ps	Time Resolution for simulation is 1ps
Waiting for 1 sub-compilation(s) to finish...	Waiting for 1 sub-compilation(s) to finish...
Compiled to VHDL Units	Compiled to VHDL Units
Built simulation executable barrel_shifter_sra_tb.isim_beh.exe	Built simulation executable barrel_shifter_sra_tb.isim_beh.exe
Fuse Memory Usage: 37424 KB	Fuse Memory Usage: 37580 KB
Fuse CPU Usage: 983 ms	Fuse CPU Usage: 875 ms
>barrel_shifter_sra_tb.isim beh.exe -icbatch isim.tcl -wdb barrel_shifter_sra_tb.isim_beh.wdb	>barrel_shifter_sra_tb.isim beh.exe -icbatch isim.tcl -wdb barrel_shifter_sra_tb.isim_beh.wdb
(Sim P.20131013 (signature 0x708090))	(Sim P.20131013 (signature 0x708090))
WARNING: A WERPACK license was found.	WARNING: A WERPACK license was found.
WARNING: Please use Xilinx License Configuration Manager to check out a full ISim license.	WARNING: Please use Xilinx License Configuration Manager to check out a full ISim license.
WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for more information on the differences between the Lite and the Full version.	WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for more information on the differences between the Lite and the Full version.
This is a Lite version of ISim.	This is a Lite version of ISim.
Time resolution is 1 ps	Time resolution is 1 ps
Simulator is doing circuit initialization process.	Simulator is doing circuit initialization process.
Finished circuit initialization process.	Finished circuit initialization process.

>xst -fih barrel_shifter_sra.xst	>xst -fih barrel_shifter_sra.xst
Release 14.7 - xst P.20131013 (m64)	Release 14.7 - xst P.20131013 (m64)
Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.	Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.
-> Parameter TMPDIR set to /xst/proj/nar/tmp	-> Parameter TMPDIR set to /xst/proj/nar/tmp
Total REAL time to Xst completion: 0.00 secs	Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.22 secs	Total CPU time to Xst completion: 0.23 secs
-> WARNING:Xst:3164 - Option "-debug" found multiple times in the command line. Only the first occurrence is considered.	-> WARNING:Xst:3164 - Option "-debug" found multiple times in the command line. Only the first occurrence is considered.
HDL Compiler	HDL Compiler
Compiling vhdl file "C:\vhdl\NDV_DN\2024\08_CORDIC\STUDENT\IBARREL_SHIFTER_SRA\cordic_pk4.vhd" in Library isim temp.	Compiling vhdl file "C:\vhdl\NDV_DN\2024\08_CORDIC\STUDENT\IBARREL_SHIFTER_SRA\cordic_pk4.vhd" in Library isim temp.
Package <cordic_pk4> compiled.	Package <cordic_pk4> compiled.
Package body <cordic_pk4> compiled.	Package body <cordic_pk4> compiled.
Compiling vhdl file "C:\vhdl\NDV_DN\2024\08_CORDIC\STUDENT\IBARREL_SHIFTER_SRA\barrel_shifter_sra.vhd" in Library isim temp.	Compiling vhdl file "C:\vhdl\NDV_DN\2024\08_CORDIC\STUDENT\IBARREL_SHIFTER_SRA\barrel_shifter_sra.vhd" in Library isim temp.
Entity <barrel_shifter_sra> compiled.	Entity <barrel_shifter_sra> compiled.
Entity <barrel_shifter_sra> (Architecture <ndy>) compiled.	Entity <barrel_shifter_sra> (Architecture <ndy>) compiled.
Total REAL time to Xst completion: 1.00 secs	Total REAL time to Xst completion: 2.00 secs
Total CPU time to Xst completion: 0.75 secs	Total CPU time to Xst completion: 1.52 secs
->	->
Total memory usage is 4477140 kilobytes	Total memory usage is 4477172 kilobytes
Number of errors : 0 (0 filtered)	Number of errors : 0 (0 filtered)
Number of warnings : 1 (0 filtered)	Number of warnings : 1 (0 filtered)
Number of infos : 0 (0 filtered)	Number of infos : 0 (0 filtered)
>fuse -incremental -o barrel_shifter_sra_tb_isim_beh.exe -prj barrel_shifter_sra_tb.prj -top barrel_shifter_sra_tb	>fuse -incremental -o barrel_shifter_sra_tb_isim_beh.exe -prj barrel_shifter_sra_tb.prj -top barrel_shifter_sra_tb
(Sim P.20131013 (signature 0x708090))	(Sim P.20131013 (signature 0x708090))
Number of CPUs detected in this system: 8	Number of CPUs detected in this system: 8
Turning on multi-threading, number of parallel sub-compilation jobs: 16	Turning on multi-threading, number of parallel sub-compilation jobs: 16
Determining compilation order of HDL files	Determining compilation order of HDL files
Parsing VHDL file "cordic_pk4.vhd" into library work	Parsing VHDL file "cordic_pk4.vhd" into library work
Parsing VHDL file "barrel_shifter_sra.vhd" into library work	Parsing VHDL file "barrel_shifter_sra.vhd" into library work
Parsing VHDL file "barrel_shifter_sra_tb.vhd" into library work	Parsing VHDL file "barrel_shifter_sra_tb.vhd" into library work
Starting static elaboration	Starting static elaboration
Completed static elaboration	Completed static elaboration
Compiling package standard	Compiling package standard
Compiling package textio	Compiling package textio
Compiling package std_logic_1164	Compiling package std_logic_1164
Compiling package numeric_std	Compiling package numeric_std
Compiling package cordic_pk4	Compiling package cordic_pk4
Compiling package math_real	Compiling package math_real
Compiling package std_logic_textio	Compiling package std_logic_textio
Compiling architecture ndy of entity barrel_shifter_sra [barrel_shifter_sra(32.32)]	Compiling architecture ndy of entity barrel_shifter_sra [barrel_shifter_sra(32.32)]
Compiling architecture rtl of entity barrel_shifter_sra_tb	Compiling architecture rtl of entity barrel_shifter_sra_tb
Time Resolution for simulation is 1ps	Time Resolution for simulation is 1ps
Waiting for 1 sub-compilation(s) to finish...	Waiting for 1 sub-compilation(s) to finish...
Compiled to VHDL Units	Compiled to VHDL Units
Built simulation executable barrel_shifter_sra_tb_isim_beh.exe	Built simulation executable barrel_shifter_sra_tb_isim_beh.exe
Fuse Memory Usage: 37448 KB	Fuse Memory Usage: 37580 KB
Fuse CPU Usage: 811 ms	Fuse CPU Usage: 875 ms
>barrel_shifter_sra_tb_isim_beh.exe -icibatch isim.tcl -wdb barrel_shifter_sra_tb_isim_beh.wdb	>barrel_shifter_sra_tb_isim_beh.exe -icibatch isim.tcl -wdb barrel_shifter_sra_tb_isim_beh.wdb
(Sim P.20131013 (signature 0x708090))	(Sim P.20131013 (signature 0x708090))
WARNING: A WERPACK license was found.	WARNING: A WERPACK license was found.
WARNING: Please use Xilinx License Configuration Manager to check out a full ISim license.	WARNING: Please use Xilinx License Configuration Manager to check out a full ISim license.
WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for more information on the differences between the Lite and the Full version.	WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for more information on the differences between the Lite and the Full version.
This is a Lite version of ISim.	This is a Lite version of ISim.
Time resolution is 1 ps	Time resolution is 1 ps
Simulator is doing circuit initialization process.	Simulator is doing circuit initialization process.
Finished circuit initialization process.	Finished circuit initialization process.

>xst -fih barrel_shifter_sra.xst	>xst -fih barrel_shifter_sra.xst
Release 14.7 - xst P.20131013 (m64)	Release 14.7 - xst P.20131013 (m64)
Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.	Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.
-> Parameter TMPDIR set to /xst/proj/nar/tmp	-> Parameter TMPDIR set to /xst/proj/nar/tmp
Total REAL time to Xst completion: 0.00 secs	Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.24 secs	Total CPU time to Xst completion: 0.23 secs
-> WARNING:Xst:3164 - Option "-debug" found multiple times in the command line. Only the first occurrence is considered.	-> WARNING:Xst:3164 - Option "-debug" found multiple times in the command line. Only the first occurrence is considered.
HDL Compiler	HDL Compiler
Compiling vhdl file "C:\vhdl\NDV_DN\2024\08_CORDIC\STUDENT\IBARREL_SHIFTER_SRA\cordic_pkq.vhd" in Library isim temp.	Compiling vhdl file "C:\vhdl\NDV_DN\2024\08_CORDIC\STUDENT\IBARREL_SHIFTER_SRA\cordic_pkq.vhd" in Library isim temp.
Package <cordic_pkq> compiled.	Package <cordic_pkq> compiled.
Package body <cordic_pkq> compiled.	Package body <cordic_pkq> compiled.
Compiling vhdl file "C:\vhdl\NDV_DN\2024\08_CORDIC\STUDENT\IBARREL_SHIFTER_SRA\barrel_shifter_sra.vhd" in Library isim temp.	Compiling vhdl file "C:\vhdl\NDV_DN\2024\08_CORDIC\STUDENT\IBARREL_SHIFTER_SRA\barrel_shifter_sra.vhd" in Library isim temp.
Entity <barrel_shifter_sra> compiled.	Entity <barrel_shifter_sra> compiled.
Entity <barrel_shifter_sra> (Architecture <ndy>) compiled.	Entity <barrel_shifter_sra> (Architecture <ndy>) compiled.
Total REAL time to Xst completion: 2.00 secs	Total REAL time to Xst completion: 2.00 secs
Total CPU time to Xst completion: 2.38 secs	Total CPU time to Xst completion: 1.52 secs
->	->
Total memory usage is 4477180 kilobytes	Total memory usage is 4477172 kilobytes
Number of errors : 0 (0 filtered)	Number of errors : 0 (0 filtered)
Number of warnings : 1 (0 filtered)	Number of warnings : 1 (0 filtered)
Number of infos : 0 (0 filtered)	Number of infos : 0 (0 filtered)
>fuse -incremental -o barrel_shifter_sra_tb.isim beh.exe -prj barrel_shifter_sra_tb.prj -top barrel_shifter_sra_tb	>fuse -incremental -o barrel_shifter_sra_tb.isim beh.exe -prj barrel_shifter_sra_tb.prj -top barrel_shifter_sra_tb
(Sim P.20131013 (signature 0x708090))	(Sim P.20131013 (signature 0x708090))
Number of CPUs detected in this system: 8	Number of CPUs detected in this system: 8
Turning on multi-threading, number of parallel sub-compilation jobs: 16	Turning on multi-threading, number of parallel sub-compilation jobs: 16
Determining compilation order of HDL files	Determining compilation order of HDL files
Parsing VHDL file "cordic_pkq.vhd" into library work	Parsing VHDL file "cordic_pkq.vhd" into library work
Parsing VHDL file "barrel_shifter_sra.vhd" into library work	Parsing VHDL file "barrel_shifter_sra.vhd" into library work
Parsing VHDL file "barrel_shifter_sra_tb.vhd" into library work	Parsing VHDL file "barrel_shifter_sra_tb.vhd" into library work
Starting static elaboration	Starting static elaboration
Completed static elaboration	Completed static elaboration
Compiling package standard	Compiling package standard
Compiling package textio	Compiling package textio
Compiling package std_logic_1164	Compiling package std_logic_1164
Compiling package numeric_std	Compiling package numeric_std
Compiling package cordic_pkq	Compiling package cordic_pkq
Compiling package math_real	Compiling package math_real
Compiling package std_logic_textio	Compiling package std_logic_textio
Compiling architecture ndy of entity barrel_shifter_sra [barrel_shifter_sra(32.32)]	Compiling architecture ndy of entity barrel_shifter_sra [barrel_shifter_sra(32.32)]
Compiling architecture rtl of entity barrel_shifter_sra_tb	Compiling architecture rtl of entity barrel_shifter_sra_tb
Time Resolution for simulation is 1ps	Time Resolution for simulation is 1ps
Waiting for 1 sub-compilation(s) to finish...	Waiting for 1 sub-compilation(s) to finish...
Compiled to VHDL Units	Compiled to VHDL Units
Built simulation executable barrel_shifter_sra_tb.isim_beh.exe	Built simulation executable barrel_shifter_sra_tb.isim_beh.exe
Fuse Memory Usage: 37396 KB	Fuse Memory Usage: 37580 KB
Fuse CPU Usage: 874 ms	Fuse CPU Usage: 875 ms
>barrel_shifter_sra_tb.isim beh.exe -icibatch isim.tcl -wdb barrel_shifter_sra_tb.isim_beh.wdb	>barrel_shifter_sra_tb.isim beh.exe -icibatch isim.tcl -wdb barrel_shifter_sra_tb.isim_beh.wdb
(Sim P.20131013 (signature 0x708090))	(Sim P.20131013 (signature 0x708090))
WARNING: A WERPACK license was found.	WARNING: A WERPACK license was found.
WARNING: Please use Xilinx License Configuration Manager to check out a full ISim license.	WARNING: Please use Xilinx License Configuration Manager to check out a full ISim license.
WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for more information on the differences between the Lite and the Full version.	WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for more information on the differences between the Lite and the Full version.
This is a Lite version of ISim.	This is a Lite version of ISim.
Time resolution is 1 ps	Time resolution is 1 ps
Simulator is doing circuit initialization process.	Simulator is doing circuit initialization process.
Finished circuit initialization process.	Finished circuit initialization process.

>xst -fH barrel_shifter_sra.xst	>xst -fH barrel_shifter_sra.xst
Release 14.7 - xst P.20131013 (m64)	Release 14.7 - xst P.20131013 (m64)
Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.	Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.
-> Parameter TMPDIR set to /xst/proj/nar/tmp	-> Parameter TMPDIR set to /xst/proj/nar/tmp
Total REAL time to Xst completion: 0.00 secs	Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.23 secs	Total CPU time to Xst completion: 0.23 secs
-> WARNING:Xst:3164 - Option "-debug" found multiple times in the command line. Only the first occurrence is considered.	-> WARNING:Xst:3164 - Option "-debug" found multiple times in the command line. Only the first occurrence is considered.
HDL Compiler	HDL Compiler
Compiling vhdl file "C:\vhdl\NDV_DN\2024\08_CORDIC\STUDENT\IBARREL_SHIFTER_SRA\cordic_pkq.vhd" in Library isim temp.	Compiling vhdl file "C:\vhdl\NDV_DN\2024\08_CORDIC\STUDENT\IBARREL_SHIFTER_SRA\cordic_pkq.vhd" in Library isim temp.
Package <cordic_pkq> compiled.	Package <cordic_pkq> compiled.
Package body <cordic_pkq> compiled.	Package body <cordic_pkq> compiled.
Compiling vhdl file "C:\vhdl\NDV_DN\2024\08_CORDIC\STUDENT\IBARREL_SHIFTER_SRA\barrel_shifter_sra.vhd" in Library isim temp.	Compiling vhdl file "C:\vhdl\NDV_DN\2024\08_CORDIC\STUDENT\IBARREL_SHIFTER_SRA\barrel_shifter_sra.vhd" in Library isim temp.
Entity <barrel_shifter_sra> compiled.	Entity <barrel_shifter_sra> compiled.
Entity <barrel_shifter_sra> (Architecture <ndy>) compiled.	Entity <barrel_shifter_sra> (Architecture <ndy>) compiled.
Total REAL time to Xst completion: 0.00 secs	Total REAL time to Xst completion: 2.00 secs
Total CPU time to Xst completion: 0.50 secs	Total CPU time to Xst completion: 1.52 secs
->	->
Total memory usage is 4477105 kilobytes	Total memory usage is 4477172 kilobytes
Number of errors : 0 (0 filtered)	Number of errors : 0 (0 filtered)
Number of warnings : 1 (0 filtered)	Number of warnings : 1 (0 filtered)
Number of infos : 0 (0 filtered)	Number of infos : 0 (0 filtered)
>fuse -incremental -o barrel_shifter_sra_tb.isim beh.exe -prj barrel_shifter_sra_tb.prj -top barrel_shifter_sra_tb	>fuse -incremental -o barrel_shifter_sra_tb.isim beh.exe -prj barrel_shifter_sra_tb.prj -top barrel_shifter_sra_tb
(Sim P.20131013 (signature 0x708090))	(Sim P.20131013 (signature 0x708090))
Number of CPUs detected in this system: 8	Number of CPUs detected in this system: 8
Turning on multi-threading, number of parallel sub-compilation jobs: 16	Turning on multi-threading, number of parallel sub-compilation jobs: 16
Determining compilation order of HDL files	Determining compilation order of HDL files
Parsing VHDL file "cordic_pkq.vhd" into library work	Parsing VHDL file "cordic_pkq.vhd" into library work
Parsing VHDL file "barrel_shifter_sra.vhd" into library work	Parsing VHDL file "barrel_shifter_sra.vhd" into library work
Parsing VHDL file "barrel_shifter_sra_tb.vhd" into library work	Parsing VHDL file "barrel_shifter_sra_tb.vhd" into library work
Starting static elaboration	Starting static elaboration
Completed static elaboration	Completed static elaboration
Compiling package standard	Compiling package standard
Compiling package textio	Compiling package textio
Compiling package std_logic_1164	Compiling package std_logic_1164
Compiling package numeric_std	Compiling package numeric_std
Compiling package cordic_pkq	Compiling package cordic_pkq
Compiling package math_real	Compiling package math_real
Compiling package std_logic_textio	Compiling package std_logic_textio
Compiling architecture ndy of entity barrel_shifter_sra [barrel_shifter_sra(32.32)]	Compiling architecture ndy of entity barrel_shifter_sra [barrel_shifter_sra(32.32)]
Compiling architecture rtl of entity barrel_shifter_sra_tb	Compiling architecture rtl of entity barrel_shifter_sra_tb
Time Resolution for simulation is 1ps	Time Resolution for simulation is 1ps
Waiting for 1 sub-compilation(s) to finish...	Waiting for 1 sub-compilation(s) to finish...
Compiled to VHDL Units	Compiled to VHDL Units
Built simulation executable barrel_shifter_sra_tb.isim_beh.exe	Built simulation executable barrel_shifter_sra_tb.isim_beh.exe
Fuse Memory Usage: 37376 KB	Fuse Memory Usage: 37580 KB
Fuse CPU Usage: 921 ms	Fuse CPU Usage: 875 ms
>barrel_shifter_sra_tb.isim beh.exe -icbatch isim.tcl -wdb barrel_shifter_sra_tb.isim_beh.wdb	>barrel_shifter_sra_tb.isim beh.exe -icbatch isim.tcl -wdb barrel_shifter_sra_tb.isim_beh.wdb
(Sim P.20131013 (signature 0x708090))	(Sim P.20131013 (signature 0x708090))
WARNING: A WERPACK license was found.	WARNING: A WERPACK license was found.
WARNING: Please use Xilinx License Configuration Manager to check out a full ISim license.	WARNING: Please use Xilinx License Configuration Manager to check out a full ISim license.
WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for more information on the differences between the Lite and the Full version.	WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for more information on the differences between the Lite and the Full version.
This is a Lite version of ISim.	This is a Lite version of ISim.
Time resolution is 1 ps	Time resolution is 1 ps
Simulator is doing circuit initialization process.	Simulator is doing circuit initialization process.
Finished circuit initialization process.	Finished circuit initialization process.

>xst -fih barrel_shifter_sra.xst	>xst -fih barrel_shifter_sra.xst
Release 14.7 - xst P.20131013 (m64)	Release 14.7 - xst P.20131013 (m64)
Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.	Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.
-> Parameter TMPDIR set to /xst/projnav.tmp	-> Parameter TMPDIR set to /xst/projnav.tmp
Total REAL time to Xst completion: 0.00 secs	Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.23 secs	Total CPU time to Xst completion: 0.23 secs
-> WARNING:Xst:3164 - Option "-debug" found multiple times in the command line. Only the first occurrence is considered.	-> WARNING:Xst:3164 - Option "-debug" found multiple times in the command line. Only the first occurrence is considered.
HDL Compiler	HDL Compiler
Compiling vhdl file "C:\vhdl\NDV_DN\2024\08_CORDIC\STUDENT\IBARREL_SHIFTER_SRA\cordic_pkq.vhd" in Library isim temp.	Compiling vhdl file "C:\vhdl\NDV_DN\2024\08_CORDIC\STUDENT\IBARREL_SHIFTER_SRA\cordic_pkq.vhd" in Library isim temp.
Package <cordic_pkq> compiled.	Package <cordic_pkq> compiled.
Package body <cordic_pkq> compiled.	Package body <cordic_pkq> compiled.
Compiling vhdl file "C:\vhdl\NDV_DN\2024\08_CORDIC\STUDENT\IBARREL_SHIFTER_SRA\barrel_shifter_sra.vhd" in Library isim temp.	Compiling vhdl file "C:\vhdl\NDV_DN\2024\08_CORDIC\STUDENT\IBARREL_SHIFTER_SRA\barrel_shifter_sra.vhd" in Library isim temp.
Entity <barrel_shifter_sra> compiled.	Entity <barrel_shifter_sra> compiled.
Entity <barrel_shifter_sra> (Architecture <ndy>) compiled.	Entity <barrel_shifter_sra> (Architecture <ndy>) compiled.
Total REAL time to Xst completion: 1.09 secs	Total REAL time to Xst completion: 2.00 secs
Total CPU time to Xst completion: 0.71 secs	Total CPU time to Xst completion: 1.52 secs
->	->
Total memory usage is 4477132 kilobytes	Total memory usage is 4477172 kilobytes
Number of errors : 0 (0 filtered)	Number of errors : 0 (0 filtered)
Number of warnings : 1 (0 filtered)	Number of warnings : 1 (0 filtered)
Number of infos : 0 (0 filtered)	Number of infos : 0 (0 filtered)
>fuse -incremental -o barrel_shifter_sra_tb.isim beh.exe -prj barrel_shifter_sra_tb.prj -top barrel_shifter_sra_tb	>fuse -incremental -o barrel_shifter_sra_tb.isim beh.exe -prj barrel_shifter_sra_tb.prj -top barrel_shifter_sra_tb
(Sim P.20131013 (signature 0x708090))	(Sim P.20131013 (signature 0x708090))
Number of CPUs detected in this system: 8	Number of CPUs detected in this system: 8
Turning on multi-threading, number of parallel sub-compilation jobs: 16	Turning on multi-threading, number of parallel sub-compilation jobs: 16
Determining compilation order of HDL files	Determining compilation order of HDL files
Parsing VHDL file "cordic_pkq.vhd" into library work	Parsing VHDL file "cordic_pkq.vhd" into library work
Parsing VHDL file "barrel_shifter_sra.vhd" into library work	Parsing VHDL file "barrel_shifter_sra.vhd" into library work
Parsing VHDL file "barrel_shifter_sra_tb.vhd" into library work	Parsing VHDL file "barrel_shifter_sra_tb.vhd" into library work
Starting static elaboration	Starting static elaboration
Completed static elaboration	Completed static elaboration
Compiling package standard	Compiling package standard
Compiling package textio	Compiling package textio
Compiling package std_logic_1164	Compiling package std_logic_1164
Compiling package numeric_std	Compiling package numeric_std
Compiling package cordic_pkq	Compiling package cordic_pkq
Compiling package math_real	Compiling package math_real
Compiling package std_logic_textio	Compiling package std_logic_textio
Compiling architecture ndy of entity barrel_shifter_sra [barrel_shifter_sra(32.32)]	Compiling architecture ndy of entity barrel_shifter_sra [barrel_shifter_sra(32.32)]
Compiling architecture rtl of entity barrel_shifter_sra_tb	Compiling architecture rtl of entity barrel_shifter_sra_tb
Time Resolution for simulation is 1ps	Time Resolution for simulation is 1ps
Waiting for 1 sub-compilation(s) to finish...	Waiting for 1 sub-compilation(s) to finish...
Compiled to VHDL Units	Compiled to VHDL Units
Built simulation executable barrel_shifter_sra_tb.isim_beh.exe	Built simulation executable barrel_shifter_sra_tb.isim_beh.exe
Fuse Memory Usage: 37316 KB	Fuse Memory Usage: 37580 KB
Fuse CPU Usage: 937 ms	Fuse CPU Usage: 875 ms
>barrel_shifter_sra_tb.isim beh.exe -icibatch isim.tcl -wdb barrel_shifter_sra_tb.isim_beh.wdb	>barrel_shifter_sra_tb.isim beh.exe -icibatch isim.tcl -wdb barrel_shifter_sra_tb.isim_beh.wdb
(Sim P.20131013 (signature 0x708090))	(Sim P.20131013 (signature 0x708090))
WARNING: A WERPACK license was found.	WARNING: A WERPACK license was found.
WARNING: Please use Xilinx License Configuration Manager to check out a full ISim license.	WARNING: Please use Xilinx License Configuration Manager to check out a full ISim license.
WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for more information on the differences between the Lite and the Full version.	WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for more information on the differences between the Lite and the Full version.
This is a Lite version of ISim.	This is a Lite version of ISim.
Time resolution is 1 ps	Time resolution is 1 ps
Simulator is doing circuit initialization process.	Simulator is doing circuit initialization process.
Finished circuit initialization process.	Finished circuit initialization process.

>xel -fh barrel_shifter_sra.xst		>xel -fh barrel_shifter_sra.xst	
Release 14.7 - xel P.20131013 (n164)		Release 14.7 - xel P.20131013 (n164)	
Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.		Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.	
-> Parameter TMPDIR set to /xstprocnsv/tmp		-> Parameter TMPDIR set to /xstprocnsv/tmp	
Total REAL time to Xst completion: 1.00 secs		Total REAL time to Xst completion: 0.00 secs	
Total CPU time to Xst completion: 0.23 secs		Total CPU time to Xst completion: 0.23 secs	
-> WARNING: Xst:3164 - Option "-debug" found multiple times in the command line. Only the first occurrence is considered.		-> WARNING: Xst:3164 - Option "-debug" found multiple times in the command line. Only the first occurrence is considered.	
+ HDL Compilation		+ HDL Compilation	
Compiling vhdl file "C:\vhdl\NDV_DN\2024\08_CORDIC\STUDENT\BARREL_SHIFTER_SRA\cordic_pkq.vhd" in Library isim_temp.		Compiling vhdl file "C:\vhdl\NDV_DN\2024\08_CORDIC\STUDENT\BARREL_SHIFTER_SRA\cordic_pkq.vhd" in Library isim_temp.	
Package <cordic_pkq> compiled.		Package <cordic_pkq> compiled.	
Package body <cordic_pkq> compiled.		Package body <cordic_pkq> compiled.	
Compiling vhdl file "C:\vhdl\NDV_DN\2024\08_CORDIC\STUDENT\BARREL_SHIFTER_SRA\barrel_shifter_sra.vhd" in Library isim_temp.		Compiling vhdl file "C:\vhdl\NDV_DN\2024\08_CORDIC\STUDENT\BARREL_SHIFTER_SRA\barrel_shifter_sra.vhd" in Library isim_temp.	
Entity <barrel_shifter_sra> compiled.		Entity <barrel_shifter_sra> compiled.	
Entity <barrel_shifter_sra> (Architecture <ndv>) compiled.		Entity <barrel_shifter_sra> (Architecture <ndv>) compiled.	
Total REAL time to Xst completion: 1.00 secs		Total REAL time to Xst completion: 2.00 secs	
Total CPU time to Xst completion: 0.35 secs		Total CPU time to Xst completion: 1.52 secs	
->		->	
Total memory usage is 4477132 kilobytes		Total memory usage is 4477172 kilobytes	
Number of errors : 0 (0 filtered)		Number of errors : 0 (0 filtered)	
Number of warnings : 1 (0 filtered)		Number of warnings : 1 (0 filtered)	
Number of infos : 0 (0 filtered)		Number of infos : 0 (0 filtered)	
+Use incremental -o barrel_shifter_sra.tb.isim_beh.exe -pri barrel_shifter_sra.tb.pri_top_barrel_shifter_sra.tb		+Use incremental -o barrel_shifter_sra.tb.isim_beh.exe -pri barrel_shifter_sra.tb.pri_top_barrel_shifter_sra.tb	
(Isim P.20131013 (signature 0x7708090))		(Isim P.20131013 (signature 0x7708090))	
Number of CPUs detected in this system: 8		Number of CPUs detected in this system: 8	
Turning on multi-threading, number of parallel sub-compilation jobs: 16		Turning on multi-threading, number of parallel sub-compilation jobs: 16	
Determining compilation order of HDL files		Determining compilation order of HDL files	
Parsing VHDL file "cordic_pkq.vhd" into library work		Parsing VHDL file "cordic_pkq.vhd" into library work	
Parsing VHDL file "barrel_shifter_sra.vhd" into library work		Parsing VHDL file "barrel_shifter_sra.vhd" into library work	
Parsing VHDL file "barrel_shifter_sra.tb.vhd" into library work		Parsing VHDL file "barrel_shifter_sra.tb.vhd" into library work	
Starting static elaboration		Starting static elaboration	
Completed static elaboration		Completed static elaboration	
Compiling package standard		Compiling package standard	
Compiling package textio		Compiling package textio	
Compiling package std_logic_1164		Compiling package std_logic_1164	
Compiling package numeric_std		Compiling package numeric_std	
Compiling package cordic_pkq		Compiling package cordic_pkq	
Compiling package math_real		Compiling package math_real	
Compiling package std_logic_textio		Compiling package std_logic_textio	
Compiling architecture ndv of entity barrel_shifter_sra (barrel_shifter_sra(32,32))		Compiling architecture ndv of entity barrel_shifter_sra (barrel_shifter_sra(32,32))	
Compiling architecture rl of entity barrel_shifter_sra.tb		Compiling architecture rl of entity barrel_shifter_sra.tb	
Time Resolution for simulation is 1ps.		Time Resolution for simulation is 1ps.	
Compiled 10 VHDL Units		Waiting for 1 sub-compilation(s) to finish.	
Built simulation executable barrel_shifter_sra.tb.isim_beh.exe		Compiled 10 VHDL Units	
Fuse Memory Usage: 37444 KB		Built simulation executable barrel_shifter_sra.tb.isim_beh.exe	
Fuse CPU Usage: 811 ms		Fuse Memory Usage: 37580 KB	
-barrel_shifter_sra.tb.isim_beh.exe -clbatch isim.tcl -wdb barrel_shifter_sra.tb.isim_beh.wdb		Fuse CPU Usage: 875 ms	
(Isim P.20131013 (signature 0x7708090))		-barrel_shifter_sra.tb.isim_beh.exe -clbatch isim.tcl -wdb barrel_shifter_sra.tb.isim_beh.wdb	
WARNING: A WEBPACK license was found.		(Isim P.20131013 (signature 0x7708090))	
WARNING: Please use Xilinx License Configuration Manager to check out a full ISim license.		WARNING: A WEBPACK license was found.	
WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for more information on the differences between the Lite and the Full version.		WARNING: Please use Xilinx License Configuration Manager to check out a full ISim license.	
This is a Lite version of ISim.		WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for more information on the differences between the Lite and the Full version.	
Time resolution is 1 ps		This is a Lite version of ISim.	
Simulator is doing circuit initialization process.		Time resolution is 1 ps	
Finished circuit initialization process.		Simulator is doing circuit initialization process.	
		Finished circuit initialization process.	

```

>xst -ifn barrel_shifter_sra.xst
Release 14.7 - xst P.20131013 (nt64)
Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.
--> Parameter TMPDIR set to ./xst/projnav.tmp
Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.23 secs

--> WARNING:Xst:3164 - Option "-debug" found multiple times in the command line. Only the first occurrence
*           HDL Compilation           *
Compiling vhdl file "C:/vhd/NDV_DN/2024/08_CORDIC/STUDENTI/BARREL_SHIFTER_SRA/cordic_1
Package <cordic_pkg> compiled.
Package body <cordic_pkg> compiled.
Compiling vhdl file "C:/vhd/NDV_DN/2024/08_CORDIC/STUDENTI/BARREL_SHIFTER_SRA/barrel_s
Entity <barrel_shifter_sra> compiled.
Entity <barrel_shifter_sra> (Architecture <ndv>) compiled.
Total REAL time to Xst completion: 2.00 secs
Total CPU time to Xst completion: 1.52 secs

-->
Total memory usage is 4477172 kilobytes
Number of errors   : 0 ( 0 filtered)
Number of warnings : 1 ( 0 filtered)
Number of infos    : 0 ( 0 filtered)
>fuse -incremental -o barrel_shifter_sra_tb_isim_beh.exe -prj barrel_shifter_sra_tb.prj -top barrel_shifte
ISim P.20131013 (signature 0x7708f090)
Number of CPUs detected in this system: 8
Turning on mult-threading, number of parallel sub-compilation jobs: 16
Determining compilation order of HDL files
Parsing VHDL file "cordic_pkg.vhd" into library work
Parsing VHDL file "barrel_shifter_sra.vhd" into library work
Parsing VHDL file "barrel_shifter_sra_tb.vhd" into library work
Starting static elaboration
Completed static elaboration
Compiling package standard
Compiling package textio
Compiling package std_logic_1164
Compiling package numeric_std
Compiling package cordic_pkg
Compiling package math_real
Compiling package std_logic_textio
Compiling architecture ndv of entity barrel_shifter_sra [\barrel_shifter_sra(32,32)]
Compiling architecture rtl of entity barrel_shifter_sra_tb
Time Resolution for simulation is 1ps.
Waiting for 1 sub-compilation(s) to finish...
Compiled 10 VHDL Units
Built simulation executable barrel_shifter_sra_tb_isim_beh.exe
Fuse Memory Usage: 37580 KB
Fuse CPU Usage: 875 ms
>barrel_shifter_sra_tb_isim_beh.exe -tclbatch isim.tcl -wdb barrel_shifter_sra_tb_isim_beh.wdb
ISim P.20131013 (signature 0x7708f090)
WARNING: A WEBPACK license was found.
WARNING: Please use Xilinx License Configuration Manager to check out a full ISim license.
WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for more information on t
This is a Lite version of ISim.
Time resolution is 1 ps
Simulator is doing circuit initialization process.
Finished circuit initialization process.

```

rence is considered.

pkg.vhd" in Library isim_temp.

shifter_sra.vhd" in Library isim_temp.

er_sra_tb

the differences between the Lite and the Full version.