

>xst -ifn CORDIC_FSM.xst	>xst -ifn CORDIC_FSM.xst
Release 14.7 - xst P.20131013 (n654)	Release 14.7 - xst P.20131013 (n654)
Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.	Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.
-> Parameter TMPDIR set to /xstprocnar/tmp	-> Parameter TMPDIR set to /xstprocnar/tmp
Total REAL time to Xst completion: 0.50 secs	Total REAL time to Xst completion: 1.00 secs
Total CPU time to Xst completion: 0.24 secs	Total CPU time to Xst completion: 0.27 secs
-> WARNING:Xst:3164 - Option "-debug" found multiple times in the command line. Only the first occurrence is considered.	-> WARNING:Xst:3164 - Option "-debug" found multiple times in the command line. Only the first occurrence is considered.
* HDL Compilation	* HDL Compilation
Compiling vhdl file "cordic_fsm.vhd" in Library work.	Compiling vhdl file "cordic_fsm.vhd" in Library work.
Entity <CORDIC_FSM> compiled.	Entity <CORDIC_FSM> compiled.
Entity <CORDIC_FSM> (Architecture <rtl>) compiled.	Entity <CORDIC_FSM> (Architecture <rtl>) compiled.
Total REAL time to Xst completion: 0.50 secs	Total REAL time to Xst completion: 1.00 secs
Total CPU time to Xst completion: 0.24 secs	Total CPU time to Xst completion: 0.27 secs
->	->
Total memory usage is 4468976 kilobytes	Total memory usage is 4468936 kilobytes
Number of errors : 0 (0 filtered)	Number of errors : 0 (0 filtered)
Number of warnings : 1 (0 filtered)	Number of warnings : 1 (0 filtered)
Number of infos : 0 (0 filtered)	Number of infos : 0 (0 filtered)
->fuse -incremental -o CORDIC_FSM_tb.isim_beh.exe -pri CORDIC_FSM_tb.pri-top CORDIC_FSM_tb	->fuse -incremental -o CORDIC_FSM_tb.isim_beh.exe -pri CORDIC_FSM_tb.pri-top CORDIC_FSM_tb
(Sim P.20131013 (signature 0x708090))	(Sim P.20131013 (signature 0x708090))
Number of CPUs detected in this system: 8	Number of CPUs detected in this system: 8
Turning on multi-threading, number of parallel sub-compilation jobs: 16	Turning on multi-threading, number of parallel sub-compilation jobs: 16
Determining compilation order of HDL files	Determining compilation order of HDL files
Parsing VHDL file "cordic_fsm.vhd" into library work	Parsing VHDL file "cordic_fsm.vhd" into library work
Parsing VHDL file "CORDIC_FSM_tb.vhd" into library work	Parsing VHDL file "CORDIC_FSM_tb.vhd" into library work
Starting static elaboration	Starting static elaboration
Completed static elaboration	Completed static elaboration
Compiling package standard	Compiling package standard
Compiling package std_logic_1164	Compiling package std_logic_1164
Compiling package numeric_std	Compiling package numeric_std
Compiling package textio	Compiling package textio
Compiling package std_logic_textio	Compiling package std_logic_textio
Compiling architecture rtl of entity CORDIC_FSM (cordic_fsm_default)	Compiling architecture rtl of entity CORDIC_FSM (cordic_fsm_default)
Compiling architecture rtl of entity cordic_fsm_tb	Compiling architecture rtl of entity cordic_fsm_tb
Time Resolution for simulation is 1ps.	Time Resolution for simulation is 1ps.
Waiting for 1 sub-compilation(s) to finish...	Waiting for 1 sub-compilation(s) to finish...
Compiled 8 VHDL Units	Compiled 8 VHDL Units
Built simulation executable CORDIC_FSM_tb.isim_beh.exe	Built simulation executable CORDIC_FSM_tb.isim_beh.exe
Fuse Memory Usage: 36776 KB	Fuse Memory Usage: 36780 KB
Fuse CPU Usage: 751 ms	Fuse CPU Usage: 859 ms
->CORDIC_FSM_tb.isim_beh.exe -icbatch isim.tcl -wdb CORDIC_FSM_tb.isim_beh.wdb	->CORDIC_FSM_tb.isim_beh.exe -icbatch isim.tcl -wdb CORDIC_FSM_tb.isim_beh.wdb
(Sim P.20131013 (signature 0x708090))	(Sim P.20131013 (signature 0x708090))
WARNING: A WEBPACK license was found.	WARNING: A WEBPACK license was found.
WARNING: Please use Xilinx License Configuration Manager to check out a full ISim license.	WARNING: Please use Xilinx License Configuration Manager to check out a full ISim license.
WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for more information on the differences between the Lite and the Full version.	WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for more information on the differences between the Lite and the Full version.
This is a Lite version of ISim.	This is a Lite version of ISim.
Time resolution is 1 ps	Time resolution is 1 ps
Simulator is doing circuit initialization process.	Simulator is doing circuit initialization process.
Finished circuit initialization process.	Finished circuit initialization process.

>xst -ifn CORDIC_FSM.xst	>xst -ifn CORDIC_FSM.xst
Release 14.7 - xst P.20131013 (n654)	Release 14.7 - xst P.20131013 (n654)
Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.	Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.
-> Parameter TMPDIR set to %xstprodir/tmp	-> Parameter TMPDIR set to %xstprodir/tmp
Total REAL time to Xst completion: 1.00 secs	Total REAL time to Xst completion: 1.00 secs
Total CPU time to Xst completion: 0.25 secs	Total CPU time to Xst completion: 0.27 secs
-> WARNING:Xst:3164 - Option "-debug" found multiple times in the command line. Only the first occurrence is considered.	-> WARNING:Xst:3164 - Option "-debug" found multiple times in the command line. Only the first occurrence is considered.
* HDL Compilation	* HDL Compilation
Compiling vhdl file "cordic_fsm.vhd" in Library work.	Compiling vhdl file "cordic_fsm.vhd" in Library work.
Entity <CORDIC_FSM> compiled.	Entity <CORDIC_FSM> compiled.
Entity <CORDIC_FSM (Architecture <rtb>) compiled.	Entity <CORDIC_FSM (Architecture <rtb>) compiled.
Total REAL time to Xst completion: 1.00 secs	Total REAL time to Xst completion: 1.00 secs
Total CPU time to Xst completion: 0.30 secs	Total CPU time to Xst completion: 0.35 secs
->	->
Total memory usage is 4465940 kilobytes	Total memory usage is 4468936 kilobytes
Number of errors : 0 (0 filtered)	Number of errors : 0 (0 filtered)
Number of warnings : 1 (0 filtered)	Number of warnings : 1 (0 filtered)
Number of infos : 0 (0 filtered)	Number of infos : 0 (0 filtered)
->fuse -incremental -o CORDIC_FSM_tb.isim_beh.exe -pri CORDIC_FSM_tb.pri-top CORDIC_FSM_tb	->fuse -incremental -o CORDIC_FSM_tb.isim_beh.exe -pri CORDIC_FSM_tb.pri-top CORDIC_FSM_tb
(ISim P.20131013 (signature 0x7098090))	(ISim P.20131013 (signature 0x7098090))
Number of CPUs detected in this system: 8	Number of CPUs detected in this system: 8
Turning on multi-threading, number of parallel sub-compilation jobs: 16	Turning on multi-threading, number of parallel sub-compilation jobs: 16
Determining compilation order of HDL files	Determining compilation order of HDL files
Parsing VHDL file "cordic_fsm.vhd" into library work	Parsing VHDL file "cordic_fsm.vhd" into library work
Parsing VHDL file "CORDIC_FSM_tb.vhd" into library work	Parsing VHDL file "CORDIC_FSM_tb.vhd" into library work
Starting static elaboration	Starting static elaboration
Completed static elaboration	Completed static elaboration
Compiling package standard	Compiling package standard
Compiling package std_logic_1164	Compiling package std_logic_1164
Compiling package numeric_std	Compiling package numeric_std
Compiling package textio	Compiling package textio
Compiling package std_logic_textio	Compiling package std_logic_textio
Compiling architecture rtl of entity CORDIC_FSM (cordic_fsm_default)	Compiling architecture rtl of entity CORDIC_FSM (cordic_fsm_default)
Compiling architecture rtl of entity cordic_fsm_tb	Compiling architecture rtl of entity cordic_fsm_tb
Time Resolution for simulation is 1ps.	Time Resolution for simulation is 1ps.
Waiting for 1 sub-compilation(s) to finish...	Waiting for 1 sub-compilation(s) to finish...
Compiled 8 VHDL Units	Compiled 8 VHDL Units
Built simulation executable CORDIC_FSM_tb.isim_beh.exe	Built simulation executable CORDIC_FSM_tb.isim_beh.exe
Fuse Memory Usage: 36500 KB	Fuse Memory Usage: 36750 KB
Fuse CPU Usage: 843 ms	Fuse CPU Usage: 859 ms
->CORDIC_FSM_tb.isim_beh.exe -icbatch isim.tcl -wdb CORDIC_FSM_tb.isim_beh.wdb	->CORDIC_FSM_tb.isim_beh.exe -icbatch isim.tcl -wdb CORDIC_FSM_tb.isim_beh.wdb
(ISim P.20131013 (signature 0x7098090))	(ISim P.20131013 (signature 0x7098090))
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This is a Lite version of ISim.	This is a Lite version of ISim.
Time resolution is 1 ps	Time resolution is 1 ps
Simulator is doing circuit initialization process.	Simulator is doing circuit initialization process.
Finished circuit initialization process.	Finished circuit initialization process.

>xst -ifn CORDIC_FSM.xst	>xst -ifn CORDIC_FSM.xst
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Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.	Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.
-> Parameter TMPDIR set to /xstprocnar/tmp	-> Parameter TMPDIR set to /xstprocnar/tmp
Total REAL time to Xst completion: 0.00 secs	Total REAL time to Xst completion: 1.00 secs
Total CPU time to Xst completion: 0.41 secs	Total CPU time to Xst completion: 0.27 secs
-> WARNING:Xst:3164 - Option "-debug" found multiple times in the command line. Only the first occurrence is considered.	-> WARNING:Xst:3164 - Option "-debug" found multiple times in the command line. Only the first occurrence is considered.
* HDL Compilation	* HDL Compilation
Compiling vhdl file "cordic_fsm.vhd" in Library work.	Compiling vhdl file "cordic_fsm.vhd" in Library work.
Entity <CORDIC_FSM> compiled.	Entity <CORDIC_FSM> compiled.
Entity <CORDIC_FSM> (Architecture <rtl>) compiled.	Entity <CORDIC_FSM> (Architecture <rtl>) compiled.
Total REAL time to Xst completion: 1.00 secs	Total REAL time to Xst completion: 1.00 secs
Total CPU time to Xst completion: 0.49 secs	Total CPU time to Xst completion: 0.35 secs
->	->
Total memory usage is 4468932 kilobytes	Total memory usage is 4468936 kilobytes
Number of errors : 0 (0 filtered)	Number of errors : 0 (0 filtered)
Number of warnings : 1 (0 filtered)	Number of warnings : 1 (0 filtered)
Number of infos : 0 (0 filtered)	Number of infos : 0 (0 filtered)
->fuse -incremental -o CORDIC_FSM_tb.isim_beh.exe -pri CORDIC_FSM_tb.pri-top CORDIC_FSM_tb	->fuse -incremental -o CORDIC_FSM_tb.isim_beh.exe -pri CORDIC_FSM_tb.pri-top CORDIC_FSM_tb
(Sim P.20131013 (signature 0x708090))	(Sim P.20131013 (signature 0x708090))
Number of CPUs detected in this system: 8	Number of CPUs detected in this system: 8
Turning on multi-threading, number of parallel sub-compilation jobs: 16	Turning on multi-threading, number of parallel sub-compilation jobs: 16
Determining compilation order of HDL files	Determining compilation order of HDL files
Parsing VHDL file "cordic_fsm.vhd" into library work	Parsing VHDL file "cordic_fsm.vhd" into library work
Parsing VHDL file "CORDIC_FSM_tb.vhd" into library work	Parsing VHDL file "CORDIC_FSM_tb.vhd" into library work
Starting static elaboration	Starting static elaboration
Completed static elaboration	Completed static elaboration
Compiling package standard	Compiling package standard
Compiling package std_logic_1164	Compiling package std_logic_1164
Compiling package numeric_std	Compiling package numeric_std
Compiling package textio	Compiling package textio
Compiling package std_logic_textio	Compiling package std_logic_textio
Compiling architecture rtl of entity CORDIC_FSM (cordic_fsm_default)	Compiling architecture rtl of entity CORDIC_FSM (cordic_fsm_default)
Compiling architecture rtl of entity cordic_fsm_tb	Compiling architecture rtl of entity cordic_fsm_tb
Time Resolution for simulation is 1ps.	Time Resolution for simulation is 1ps.
Waiting for 1 sub-compilation(s) to finish...	Waiting for 1 sub-compilation(s) to finish...
Compiled 8 VHDL Units	Compiled 8 VHDL Units
Built simulation executable CORDIC_FSM_tb.isim_beh.exe	Built simulation executable CORDIC_FSM_tb.isim_beh.exe
Fuse Memory Usage: 36740 KB	Fuse Memory Usage: 36750 KB
Fuse CPU Usage: 827 ms	Fuse CPU Usage: 859 ms
->CORDIC_FSM_tb.isim_beh.exe -icbatch isim.tcl -wdb CORDIC_FSM_tb.isim_beh.wdb	->CORDIC_FSM_tb.isim_beh.exe -icbatch isim.tcl -wdb CORDIC_FSM_tb.isim_beh.wdb
(Sim P.20131013 (signature 0x708090))	(Sim P.20131013 (signature 0x708090))
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This is a Lite version of ISim.	This is a Lite version of ISim.
Time resolution is 1 ps	Time resolution is 1 ps
Simulator is doing circuit initialization process.	Simulator is doing circuit initialization process.
Finished circuit initialization process.	Finished circuit initialization process.

>xst -ifn CORDIC_FSM.xst	>xst -ifn CORDIC_FSM.xst
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Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.	Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.
-> Parameter TMPDIR set to /xstprojnav/tmp	-> Parameter TMPDIR set to /xstprojnav/tmp
Total REAL time to Xst completion: 0.00 secs	Total REAL time to Xst completion: 1.00 secs
Total CPU time to Xst completion: 0.23 secs	Total CPU time to Xst completion: 0.27 secs
-> WARNING:Xst:3164 - Option "-debug" found multiple times in the command line. Only the first occurrence is considered.	-> WARNING:Xst:3164 - Option "-debug" found multiple times in the command line. Only the first occurrence is considered.
* HDL Compilation	* HDL Compilation
Compiling vhdl file "cordic_fsm.vhd" in Library work.	Compiling vhdl file "cordic_fsm.vhd" in Library work.
Entity <CORDIC_FSM> compiled.	Entity <CORDIC_FSM> compiled.
Entity <CORDIC_FSM> (Architecture <rtl>) compiled.	Entity <CORDIC_FSM> (Architecture <rtl>) compiled.
Total REAL time to Xst completion: 0.00 secs	Total REAL time to Xst completion: 1.00 secs
Total CPU time to Xst completion: 0.29 secs	Total CPU time to Xst completion: 0.35 secs
->	->
Total memory usage is 4468972 kilobytes	Total memory usage is 4468936 kilobytes
Number of errors : 0 (0 filtered)	Number of errors : 0 (0 filtered)
Number of warnings : 1 (0 filtered)	Number of warnings : 1 (0 filtered)
Number of infos : 0 (0 filtered)	Number of infos : 0 (0 filtered)
->fuse -incremental -o CORDIC_FSM_tb.isim_beh.exe -pri CORDIC_FSM_tb.pri-top CORDIC_FSM_tb	->fuse -incremental -o CORDIC_FSM_tb.isim_beh.exe -pri CORDIC_FSM_tb.pri-top CORDIC_FSM_tb
(Sim P.20131013 (signature 0x708090))	(Sim P.20131013 (signature 0x708090))
Number of CPUs detected in this system: 8	Number of CPUs detected in this system: 8
Turning on multi-threading, number of parallel sub-compilation jobs: 16	Turning on multi-threading, number of parallel sub-compilation jobs: 16
Determining compilation order of HDL files	Determining compilation order of HDL files
Parsing VHDL file "cordic_fsm.vhd" into library work	Parsing VHDL file "cordic_fsm.vhd" into library work
Parsing VHDL file "CORDIC_FSM_tb.vhd" into library work	Parsing VHDL file "CORDIC_FSM_tb.vhd" into library work
Starting static elaboration	Starting static elaboration
Completed static elaboration	Completed static elaboration
Compiling package standard	Compiling package standard
Compiling package std_logic_1164	Compiling package std_logic_1164
Compiling package numeric_std	Compiling package numeric_std
Compiling package textio	Compiling package textio
Compiling package std_logic_textio	Compiling package std_logic_textio
Compiling architecture rtl of entity CORDIC_FSM (cordic_fsm_default)	Compiling architecture rtl of entity CORDIC_FSM (cordic_fsm_default)
Compiling architecture rtl of entity cordic_fsm_tb	Compiling architecture rtl of entity cordic_fsm_tb
Time Resolution for simulation is 1ps.	Time Resolution for simulation is 1ps.
Waiting for 1 sub-compilation(s) to finish...	Waiting for 1 sub-compilation(s) to finish...
Compiled 8 VHDL Units	Compiled 8 VHDL Units
Built simulation executable CORDIC_FSM_tb.isim_beh.exe	Built simulation executable CORDIC_FSM_tb.isim_beh.exe
Fuse Memory Usage: 36796 KB	Fuse Memory Usage: 36780 KB
Fuse CPU Usage: 827 ms	Fuse CPU Usage: 859 ms
->CORDIC_FSM_tb.isim_beh.exe -icbatch isim.tcl -wdb CORDIC_FSM_tb.isim_beh.wdb	->CORDIC_FSM_tb.isim_beh.exe -icbatch isim.tcl -wdb CORDIC_FSM_tb.isim_beh.wdb
(Sim P.20131013 (signature 0x708090))	(Sim P.20131013 (signature 0x708090))
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This is a Lite version of ISim.	This is a Lite version of ISim.
Time resolution is 1 ps	Time resolution is 1 ps
Simulator is doing circuit initialization process.	Simulator is doing circuit initialization process.
Finished circuit initialization process.	Finished circuit initialization process.

>xst -ifn CORDIC_FSM.xst	>xst -ifn CORDIC_FSM.xst
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Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.	Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.
-> Parameter TMPDIR set to /xstprocnar/tmp	-> Parameter TMPDIR set to /xstprocnar/tmp
Total REAL time to Xst completion: 0.50 secs	Total REAL time to Xst completion: 1.00 secs
Total CPU time to Xst completion: 0.24 secs	Total CPU time to Xst completion: 0.27 secs
-> WARNING:Xst:3164 - Option "-debug" found multiple times in the command line. Only the first occurrence is considered.	-> WARNING:Xst:3164 - Option "-debug" found multiple times in the command line. Only the first occurrence is considered.
* HDL Compilation	* HDL Compilation
Compiling vhdl file "cordic_fsm.vhd" in Library work.	Compiling vhdl file "cordic_fsm.vhd" in Library work.
Entity <CORDIC_FSM> compiled.	Entity <CORDIC_FSM> compiled.
Entity <CORDIC_FSM> (Architecture <rtl>) compiled.	Entity <CORDIC_FSM> (Architecture <rtl>) compiled.
Total REAL time to Xst completion: 0.50 secs	Total REAL time to Xst completion: 1.00 secs
Total CPU time to Xst completion: 0.52 secs	Total CPU time to Xst completion: 0.35 secs
->	->
Total memory usage is 4468992 kilobytes	Total memory usage is 4468936 kilobytes
Number of errors : 0 (0 filtered)	Number of errors : 0 (0 filtered)
Number of warnings : 1 (0 filtered)	Number of warnings : 1 (0 filtered)
Number of infos : 0 (0 filtered)	Number of infos : 0 (0 filtered)
->fuse -incremental -o CORDIC_FSM_tb.isim_beh.exe -pri CORDIC_FSM_tb.pri-top CORDIC_FSM_tb	->fuse -incremental -o CORDIC_FSM_tb.isim_beh.exe -pri CORDIC_FSM_tb.pri-top CORDIC_FSM_tb
(ISim P.20131013 (signature 0x708090))	(ISim P.20131013 (signature 0x708090))
Number of CPUs detected in this system: 8	Number of CPUs detected in this system: 8
Turning on multi-threading, number of parallel sub-compilation jobs: 16	Turning on multi-threading, number of parallel sub-compilation jobs: 16
Determining compilation order of HDL files	Determining compilation order of HDL files
Parsing VHDL file "cordic_fsm.vhd" into library work	Parsing VHDL file "cordic_fsm.vhd" into library work
Parsing VHDL file "CORDIC_FSM_tb.vhd" into library work	Parsing VHDL file "CORDIC_FSM_tb.vhd" into library work
Starting static elaboration	Starting static elaboration
Completed static elaboration	Completed static elaboration
Compiling package standard	Compiling package standard
Compiling package std_logic_1164	Compiling package std_logic_1164
Compiling package numeric_std	Compiling package numeric_std
Compiling package textio	Compiling package textio
Compiling package std_logic_textio	Compiling package std_logic_textio
Compiling architecture rtl of entity CORDIC_FSM (cordic_fsm_default)	Compiling architecture rtl of entity CORDIC_FSM (cordic_fsm_default)
Compiling architecture rtl of entity cordic_fsm_tb	Compiling architecture rtl of entity cordic_fsm_tb
Time Resolution for simulation is 1ps.	Time Resolution for simulation is 1ps.
Waiting for 1 sub-compilation(s) to finish...	Waiting for 1 sub-compilation(s) to finish...
Compiled 8 VHDL Units	Compiled 8 VHDL Units
Built simulation executable CORDIC_FSM_tb.isim_beh.exe	Built simulation executable CORDIC_FSM_tb.isim_beh.exe
Fuse Memory Usage: 36564 KB	Fuse Memory Usage: 36750 KB
Fuse CPU Usage: 850 ms	Fuse CPU Usage: 859 ms
->CORDIC_FSM_tb.isim_beh.exe -icbatch isim.tcl -wdb CORDIC_FSM_tb.isim_beh.wdb	->CORDIC_FSM_tb.isim_beh.exe -icbatch isim.tcl -wdb CORDIC_FSM_tb.isim_beh.wdb
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This is a Lite version of ISim.	This is a Lite version of ISim.
Time resolution is 1 ps	Time resolution is 1 ps
Simulator is doing circuit initialization process.	Simulator is doing circuit initialization process.
Finished circuit initialization process.	Finished circuit initialization process.

>set -h CORDIC_FSM.xst	>set -h CORDIC_FSM.xst
Release 14.7 - xst P.20131013 (n64)	Release 14.7 - xst P.20131013 (n64)
Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.	Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.
-> Parameter TMPDIR set to /xstprograw/tmp	-> Parameter TMPDIR set to /xstprograw/tmp
Total REAL time to Xst completion: 1.00 secs	Total REAL time to Xst completion: 1.00 secs
Total CPU time to Xst completion: 0.41 secs	Total CPU time to Xst completion: 0.27 secs
-> WARNING:Xst:3164 - Option "-debug" found multiple times in the command line. Only the first occurrence is considered.	-> WARNING:Xst:3164 - Option "-debug" found multiple times in the command line. Only the first occurrence is considered.
* HDL Compilation *	* HDL Compilation *
Compiling vhdl file 'cordic_fsm.vhd' in Library work.	Compiling vhdl file 'cordic_fsm.vhd' in Library work.
Entity <CORDIC_FSM> compiled.	Entity <CORDIC_FSM> compiled.
Entity <CORDIC_FSM> (Architecture <rtl>) compiled.	Entity <CORDIC_FSM> (Architecture <rtl>) compiled.
Total REAL time to Xst completion: 1.00 secs	Total REAL time to Xst completion: 1.00 secs
Total CPU time to Xst completion: 1.21 secs	Total CPU time to Xst completion: 0.35 secs
->	->
Total memory usage is 4468948 kilobytes	Total memory usage is 4468936 kilobytes
Number of errors : 0 (0 filtered)	Number of errors : 0 (0 filtered)
Number of warnings : 1 (0 filtered)	Number of warnings : 1 (0 filtered)
Number of infos : 0 (0 filtered)	Number of infos : 0 (0 filtered)
->Use incremental -o CORDIC_FSM_tb_isim_beh.exe -prj CORDIC_FSM_tb_top CORDIC_FSM_tb	->Use incremental -o CORDIC_FSM_tb_isim_beh.exe -prj CORDIC_FSM_tb_top CORDIC_FSM_tb
(Sim P.20131013 (signature 0x7708090))	(Sim P.20131013 (signature 0x7708090))
Number of CPUs detected in this system: 8	Number of CPUs detected in this system: 8
Turning on multi-threading, number of parallel sub-compilation jobs: 16	Turning on multi-threading, number of parallel sub-compilation jobs: 16
Determining compilation order of HDL files	Determining compilation order of HDL files
Parsing VHDL file 'cordic_fsm.vhd' into library work	Parsing VHDL file 'cordic_fsm.vhd' into library work
Parsing VHDL file 'CORDIC_FSM_tb.vhd' into library work	Parsing VHDL file 'CORDIC_FSM_tb.vhd' into library work
Starting static elaboration	Starting static elaboration
Completed static elaboration	Completed static elaboration
Compiling package standard	Compiling package standard
Compiling package std_logic_1164	Compiling package std_logic_1164
Compiling package numeric_std	Compiling package numeric_std
Compiling package textio	Compiling package textio
Compiling package std_logic_textio	Compiling package std_logic_textio
Compiling architecture rtl of entity CORDIC_FSM [cordic_fsm_default]	Compiling architecture rtl of entity CORDIC_FSM [cordic_fsm_default]
Compiling architecture rtl of entity cordic_fsm_tb	Compiling architecture rtl of entity cordic_fsm_tb
Time Resolution for simulation is 1ps.	Time Resolution for simulation is 1ps.
Compiled 8 VHDL Units	Waiting for 1 sub-compilation(s) to finish.
Built simulation executable CORDIC_FSM_tb_isim_beh.exe	Built simulation executable CORDIC_FSM_tb_isim_beh.exe
Fuse Memory Usage: 36884 KB	Fuse Memory Usage: 36780 KB
Fuse CPU Usage: 936 ms	Fuse CPU Usage: 859 ms
->CORDIC_FSM_tb_isim_beh.exe -jcbatch isim.tcl -wdb CORDIC_FSM_tb_isim_beh.wdb	->CORDIC_FSM_tb_isim_beh.exe -jcbatch isim.tcl -wdb CORDIC_FSM_tb_isim_beh.wdb
(Sim P.20131013 (signature 0x7708090))	(Sim P.20131013 (signature 0x7708090))
WARNING: A WEBPACK license was found.	WARNING: A WEBPACK license was found.
WARNING: Please use Xilinx License Configuration Manager to check out a full ISim license.	WARNING: Please use Xilinx License Configuration Manager to check out a full ISim license.
WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for more information on the differences between the Lite and the Full version.	WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for more information on the differences between the Lite and the Full version.
This is a Lite version of ISim.	This is a Lite version of ISim.
Time resolution is 1 ps	Time resolution is 1 ps
Simulator is doing circuit initialization process.	Simulator is doing circuit initialization process.
Finished circuit initialization process.	Finished circuit initialization process.

>xst -ifn CORDIC_FSM.xst	>xst -ifn CORDIC_FSM.xst
Release 14.7 - xst P.20131013 (n654)	Release 14.7 - xst P.20131013 (n654)
Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.	Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.
-> Parameter TMPDIR set to /xstprocnar/tmp	-> Parameter TMPDIR set to /xstprocnar/tmp
Total REAL time to Xst completion: 0.80 secs	Total REAL time to Xst completion: 1.00 secs
Total CPU time to Xst completion: 0.23 secs	Total CPU time to Xst completion: 0.27 secs
-> WARNING:Xst:3164 - Option "-debug" found multiple times in the command line. Only the first occurrence is considered.	-> WARNING:Xst:3164 - Option "-debug" found multiple times in the command line. Only the first occurrence is considered.
* HDL Compilation	* HDL Compilation
Compiling vhdl file "cordic_fsm.vhd" in Library work.	Compiling vhdl file "cordic_fsm.vhd" in Library work.
Entity <CORDIC_FSM> compiled.	Entity <CORDIC_FSM> compiled.
Entity <CORDIC_FSM> (Architecture <rtl>) compiled.	Entity <CORDIC_FSM> (Architecture <rtl>) compiled.
Total REAL time to Xst completion: 0.80 secs	Total REAL time to Xst completion: 1.00 secs
Total CPU time to Xst completion: 0.29 secs	Total CPU time to Xst completion: 0.35 secs
->	->
Total memory usage is 4468976 kilobytes	Total memory usage is 4468936 kilobytes
Number of errors : 0 (0 filtered)	Number of errors : 0 (0 filtered)
Number of warnings : 1 (0 filtered)	Number of warnings : 1 (0 filtered)
Number of infos : 0 (0 filtered)	Number of infos : 0 (0 filtered)
->fuse -incremental -o CORDIC_FSM_tb.isim_beh.exe -pri CORDIC_FSM_tb.pri-top CORDIC_FSM_tb	->fuse -incremental -o CORDIC_FSM_tb.isim_beh.exe -pri CORDIC_FSM_tb.pri-top CORDIC_FSM_tb
(Sim P.20131013 (signature 0x708090))	(Sim P.20131013 (signature 0x708090))
Number of CPUs detected in this system: 8	Number of CPUs detected in this system: 8
Turning on multi-threading, number of parallel sub-compilation jobs: 16	Turning on multi-threading, number of parallel sub-compilation jobs: 16
Determining compilation order of HDL files	Determining compilation order of HDL files
Parsing VHDL file "cordic_fsm.vhd" into library work	Parsing VHDL file "cordic_fsm.vhd" into library work
Parsing VHDL file "CORDIC_FSM_tb.vhd" into library work	Parsing VHDL file "CORDIC_FSM_tb.vhd" into library work
Starting static elaboration	Starting static elaboration
Completed static elaboration	Completed static elaboration
Compiling package standard	Compiling package standard
Compiling package std_logic_1164	Compiling package std_logic_1164
Compiling package numeric_std	Compiling package numeric_std
Compiling package textio	Compiling package textio
Compiling package std_logic_textio	Compiling package std_logic_textio
Compiling architecture rtl of entity CORDIC_FSM (cordic_fsm_default)	Compiling architecture rtl of entity CORDIC_FSM (cordic_fsm_default)
Compiling architecture rtl of entity cordic_fsm_tb	Compiling architecture rtl of entity cordic_fsm_tb
Time Resolution for simulation is 1ps.	Time Resolution for simulation is 1ps.
Waiting for 1 sub-compilation(s) to finish...	Waiting for 1 sub-compilation(s) to finish...
Compiled 8 VHDL Units	Compiled 8 VHDL Units
Built simulation executable CORDIC_FSM_tb.isim_beh.exe	Built simulation executable CORDIC_FSM_tb.isim_beh.exe
Fuse Memory Usage: 36852 KB	Fuse Memory Usage: 36780 KB
Fuse CPU Usage: 828 ms	Fuse CPU Usage: 859 ms
->CORDIC_FSM_tb.isim_beh.exe -icbatch isim.tcl -wdb CORDIC_FSM_tb.isim_beh.wdb	->CORDIC_FSM_tb.isim_beh.exe -icbatch isim.tcl -wdb CORDIC_FSM_tb.isim_beh.wdb
(Sim P.20131013 (signature 0x708090))	(Sim P.20131013 (signature 0x708090))
WARNING: A WEBPACK license was found.	WARNING: A WEBPACK license was found.
WARNING: Please use Xilinx License Configuration Manager to check out a full ISim license.	WARNING: Please use Xilinx License Configuration Manager to check out a full ISim license.
WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for more information on the differences between the Lite and the Full version.	WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for more information on the differences between the Lite and the Full version.
This is a Lite version of ISim.	This is a Lite version of ISim.
Time resolution is 1 ps	Time resolution is 1 ps
Simulator is doing circuit initialization process.	Simulator is doing circuit initialization process.
Finished circuit initialization process.	Finished circuit initialization process.

>xst -ifn CORDIC_FSM.xst	>xst -ifn CORDIC_FSM.xst
Release 14.7 - xst P.20131013 (n654)	Release 14.7 - xst P.20131013 (n654)
Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.	Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.
-> Parameter TMPDIR set to /xstprojdir/tmp	-> Parameter TMPDIR set to /xstprojdir/tmp
Total REAL time to Xst completion: 1.00 secs	Total REAL time to Xst completion: 1.00 secs
Total CPU time to Xst completion: 0.26 secs	Total CPU time to Xst completion: 0.27 secs
-> WARNING:Xst:3164 - Option "-debug" found multiple times in the command line. Only the first occurrence is considered.	-> WARNING:Xst:3164 - Option "-debug" found multiple times in the command line. Only the first occurrence is considered.
* HDL Compilation	* HDL Compilation
Compiling vhdl file "cordic_fsm.vhd" in Library work.	Compiling vhdl file "cordic_fsm.vhd" in Library work.
Entity <CORDIC_FSM> compiled.	Entity <CORDIC_FSM> compiled.
Entity <CORDIC_FSM> (Architecture <rtl>) compiled.	Entity <CORDIC_FSM> (Architecture <rtl>) compiled.
Total REAL time to Xst completion: 1.00 secs	Total REAL time to Xst completion: 1.00 secs
Total CPU time to Xst completion: 0.71 secs	Total CPU time to Xst completion: 0.35 secs
->	->
Total memory usage is 4468988 kilobytes	Total memory usage is 4468936 kilobytes
Number of errors : 0 (0 filtered)	Number of errors : 0 (0 filtered)
Number of warnings : 1 (0 filtered)	Number of warnings : 1 (0 filtered)
Number of infos : 0 (0 filtered)	Number of infos : 0 (0 filtered)
->fuse -incremental -o CORDIC_FSM_tb.isim_beh.exe -pri CORDIC_FSM_tb.pri-top CORDIC_FSM_tb	->fuse -incremental -o CORDIC_FSM_tb.isim_beh.exe -pri CORDIC_FSM_tb.pri-top CORDIC_FSM_tb
(Sim P.20131013 (signature 0x708090))	(Sim P.20131013 (signature 0x708090))
Number of CPUs detected in this system: 8	Number of CPUs detected in this system: 8
Turning on multi-threading, number of parallel sub-compilation jobs: 16	Turning on multi-threading, number of parallel sub-compilation jobs: 16
Determining compilation order of HDL files	Determining compilation order of HDL files
Parsing VHDL file "cordic_fsm.vhd" into library work	Parsing VHDL file "cordic_fsm.vhd" into library work
Parsing VHDL file "CORDIC_FSM_tb.vhd" into library work	Parsing VHDL file "CORDIC_FSM_tb.vhd" into library work
Starting static elaboration	Starting static elaboration
Completed static elaboration	Completed static elaboration
Compiling package standard	Compiling package standard
Compiling package std_logic_1164	Compiling package std_logic_1164
Compiling package numeric_std	Compiling package numeric_std
Compiling package textio	Compiling package textio
Compiling package std_logic_textio	Compiling package std_logic_textio
Compiling architecture rtl of entity CORDIC_FSM (cordic_fsm_default)	Compiling architecture rtl of entity CORDIC_FSM (cordic_fsm_default)
Compiling architecture rtl of entity cordic_fsm_tb	Compiling architecture rtl of entity cordic_fsm_tb
Time Resolution for simulation is 1ps.	Time Resolution for simulation is 1ps.
Waiting for 1 sub-compilation(s) to finish...	Waiting for 1 sub-compilation(s) to finish...
Compiled 8 VHDL Units	Compiled 8 VHDL Units
Built simulation executable CORDIC_FSM_tb.isim_beh.exe	Built simulation executable CORDIC_FSM_tb.isim_beh.exe
Fuse Memory Usage: 36748 KB	Fuse Memory Usage: 36750 KB
Fuse CPU Usage: 854 ms	Fuse CPU Usage: 859 ms
->CORDIC_FSM_tb.isim_beh.exe -icbatch isim.tcl -wdb CORDIC_FSM_tb.isim_beh.wdb	->CORDIC_FSM_tb.isim_beh.exe -icbatch isim.tcl -wdb CORDIC_FSM_tb.isim_beh.wdb
(Sim P.20131013 (signature 0x708090))	(Sim P.20131013 (signature 0x708090))
WARNING: A WEBPACK license was found.	WARNING: A WEBPACK license was found.
WARNING: Please use Xilinx License Configuration Manager to check out a full ISim license.	WARNING: Please use Xilinx License Configuration Manager to check out a full ISim license.
WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for more information on the differences between the Lite and the Full version.	WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for more information on the differences between the Lite and the Full version.
This is a Lite version of ISim.	This is a Lite version of ISim.
Time resolution is 1 ps	Time resolution is 1 ps
Simulator is doing circuit initialization process.	Simulator is doing circuit initialization process.
Finished circuit initialization process.	Finished circuit initialization process.

>xst -ifn CORDIC_FSM.xst	>xst -ifn CORDIC_FSM.xst
Release 14.7 - xst P.20131013 (n654)	Release 14.7 - xst P.20131013 (n654)
Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.	Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.
-> Parameter TMPDIR set to /xstprocnar/tmp	-> Parameter TMPDIR set to /xstprocnar/tmp
Total REAL time to Xst completion: 0.80 secs	Total REAL time to Xst completion: 1.00 secs
Total CPU time to Xst completion: 0.24 secs	Total CPU time to Xst completion: 0.27 secs
-> WARNING:Xst:3164 - Option "-debug" found multiple times in the command line. Only the first occurrence is considered.	-> WARNING:Xst:3164 - Option "-debug" found multiple times in the command line. Only the first occurrence is considered.
* HDL Compilation	* HDL Compilation
Compiling vhdl file "cordic_fsm.vhd" in Library work.	Compiling vhdl file "cordic_fsm.vhd" in Library work.
Entity <CORDIC_FSM> compiled.	Entity <CORDIC_FSM> compiled.
Entity <CORDIC_FSM> (Architecture <rtl>) compiled.	Entity <CORDIC_FSM> (Architecture <rtl>) compiled.
Total REAL time to Xst completion: 0.80 secs	Total REAL time to Xst completion: 1.00 secs
Total CPU time to Xst completion: 0.24 secs	Total CPU time to Xst completion: 0.27 secs
->	->
Total memory usage is 4468932 kilobytes	Total memory usage is 4468936 kilobytes
Number of errors : 0 (0 filtered)	Number of errors : 0 (0 filtered)
Number of warnings : 1 (0 filtered)	Number of warnings : 1 (0 filtered)
Number of infos : 0 (0 filtered)	Number of infos : 0 (0 filtered)
->fuse -incremental -o CORDIC_FSM_tb.isim_beh.exe -pri CORDIC_FSM_tb.pri-top CORDIC_FSM_tb	->fuse -incremental -o CORDIC_FSM_tb.isim_beh.exe -pri CORDIC_FSM_tb.pri-top CORDIC_FSM_tb
(Sim P.20131013 (signature 0x708090))	(Sim P.20131013 (signature 0x708090))
Number of CPUs detected in this system: 8	Number of CPUs detected in this system: 8
Turning on multi-threading, number of parallel sub-compilation jobs: 16	Turning on multi-threading, number of parallel sub-compilation jobs: 16
Determining compilation order of HDL files	Determining compilation order of HDL files
Parsing VHDL file "cordic_fsm.vhd" into library work	Parsing VHDL file "cordic_fsm.vhd" into library work
Parsing VHDL file "CORDIC_FSM_tb.vhd" into library work	Parsing VHDL file "CORDIC_FSM_tb.vhd" into library work
Starting static elaboration	Starting static elaboration
Completed static elaboration	Completed static elaboration
Compiling package standard	Compiling package standard
Compiling package std_logic_1164	Compiling package std_logic_1164
Compiling package numeric_std	Compiling package numeric_std
Compiling package textio	Compiling package textio
Compiling package std_logic_textio	Compiling package std_logic_textio
Compiling architecture rtl of entity CORDIC_FSM (cordic_fsm_default)	Compiling architecture rtl of entity CORDIC_FSM (cordic_fsm_default)
Compiling architecture rtl of entity cordic_fsm_tb	Compiling architecture rtl of entity cordic_fsm_tb
Time Resolution for simulation is 1ps.	Time Resolution for simulation is 1ps.
Waiting for 1 sub-compilation(s) to finish...	Waiting for 1 sub-compilation(s) to finish...
Compiled 8 VHDL Units	Compiled 8 VHDL Units
Built simulation executable CORDIC_FSM_tb.isim_beh.exe	Built simulation executable CORDIC_FSM_tb.isim_beh.exe
Fuse Memory Usage: 3624 KB	Fuse Memory Usage: 3676 KB
Fuse CPU Usage: 750 ms	Fuse CPU Usage: 859 ms
->CORDIC_FSM_tb.isim_beh.exe -icbatch isim.tcl -wdb CORDIC_FSM_tb.isim_beh.wdb	->CORDIC_FSM_tb.isim_beh.exe -icbatch isim.tcl -wdb CORDIC_FSM_tb.isim_beh.wdb
(Sim P.20131013 (signature 0x708090))	(Sim P.20131013 (signature 0x708090))
WARNING: A WEBPACK license was found.	WARNING: A WEBPACK license was found.
WARNING: Please use Xilinx License Configuration Manager to check out a full ISim license.	WARNING: Please use Xilinx License Configuration Manager to check out a full ISim license.
WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for more information on the differences between the Lite and the Full version.	WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for more information on the differences between the Lite and the Full version.
This is a Lite version of ISim.	This is a Lite version of ISim.
Time resolution is 1 ps	Time resolution is 1 ps
Simulator is doing circuit initialization process.	Simulator is doing circuit initialization process.
Finished circuit initialization process.	Finished circuit initialization process.

>xst -ifn CORDIC_FSM.xst	>xst -ifn CORDIC_FSM.xst
Release 14.7 - xst P.20131013 (n654)	Release 14.7 - xst P.20131013 (n654)
Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.	Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.
-> Parameter TMPDIR set to /xstprocnar/tmp	-> Parameter TMPDIR set to /xstprocnar/tmp
Total REAL time to Xst completion: 0.88 secs	Total REAL time to Xst completion: 1.00 secs
Total CPU time to Xst completion: 0.28 secs	Total CPU time to Xst completion: 0.27 secs
-> WARNING:Xst:3164 - Option "-debug" found multiple times in the command line. Only the first occurrence is considered.	-> WARNING:Xst:3164 - Option "-debug" found multiple times in the command line. Only the first occurrence is considered.
* HDL Compilation	* HDL Compilation
Compiling vhdl file "cordic_fsm.vhd" in Library work.	Compiling vhdl file "cordic_fsm.vhd" in Library work.
Entity <CORDIC_FSM> compiled.	Entity <CORDIC_FSM> compiled.
Entity <CORDIC_FSM> (Architecture <rtl>) compiled.	Entity <CORDIC_FSM> (Architecture <rtl>) compiled.
Total REAL time to Xst completion: 0.88 secs	Total REAL time to Xst completion: 1.00 secs
Total CPU time to Xst completion: 0.35 secs	Total CPU time to Xst completion: 0.35 secs
->	->
Total memory usage is 4468928 kilobytes	Total memory usage is 4468936 kilobytes
Number of errors : 0 (0 filtered)	Number of errors : 0 (0 filtered)
Number of warnings : 1 (0 filtered)	Number of warnings : 1 (0 filtered)
Number of infos : 0 (0 filtered)	Number of infos : 0 (0 filtered)
->fuse -incremental -o CORDIC_FSM_tb.isim_beh.exe -pri CORDIC_FSM_tb.pri-top CORDIC_FSM_tb	->fuse -incremental -o CORDIC_FSM_tb.isim_beh.exe -pri CORDIC_FSM_tb.pri-top CORDIC_FSM_tb
(ISim P.20131013 (signature 0x708090))	(ISim P.20131013 (signature 0x708090))
Number of CPUs detected in this system: 8	Number of CPUs detected in this system: 8
Turning on multi-threading, number of parallel sub-compilation jobs: 16	Turning on multi-threading, number of parallel sub-compilation jobs: 16
Determining compilation order of HDL files	Determining compilation order of HDL files
Parsing VHDL file "cordic_fsm.vhd" into library work	Parsing VHDL file "cordic_fsm.vhd" into library work
Parsing VHDL file "CORDIC_FSM_tb.vhd" into library work	Parsing VHDL file "CORDIC_FSM_tb.vhd" into library work
Starting static elaboration	Starting static elaboration
Completed static elaboration	Completed static elaboration
Compiling package standard	Compiling package standard
Compiling package std_logic_1164	Compiling package std_logic_1164
Compiling package numeric_std	Compiling package numeric_std
Compiling package textio	Compiling package textio
Compiling package std_logic_textio	Compiling package std_logic_textio
Compiling architecture rtl of entity CORDIC_FSM (cordic_fsm_default)	Compiling architecture rtl of entity CORDIC_FSM (cordic_fsm_default)
Compiling architecture rtl of entity cordic_fsm_tb	Compiling architecture rtl of entity cordic_fsm_tb
Time Resolution for simulation is 1ps.	Time Resolution for simulation is 1ps.
Waiting for 1 sub-compilation(s) to finish...	Waiting for 1 sub-compilation(s) to finish...
Compiled 8 VHDL Units	Compiled 8 VHDL Units
Built simulation executable CORDIC_FSM_tb.isim_beh.exe	Built simulation executable CORDIC_FSM_tb.isim_beh.exe
Fuse Memory Usage: 36632 KB	Fuse Memory Usage: 36780 KB
Fuse CPU Usage: 859 ms	Fuse CPU Usage: 859 ms
->CORDIC_FSM_tb.isim_beh.exe -icbatch isim.tcl -wdb CORDIC_FSM_tb.isim_beh.wdb	->CORDIC_FSM_tb.isim_beh.exe -icbatch isim.tcl -wdb CORDIC_FSM_tb.isim_beh.wdb
(ISim P.20131013 (signature 0x708090))	(ISim P.20131013 (signature 0x708090))
WARNING: A WEBPACK license was found.	WARNING: A WEBPACK license was found.
WARNING: Please use Xilinx License Configuration Manager to check out a full ISim license.	WARNING: Please use Xilinx License Configuration Manager to check out a full ISim license.
WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for more information on the differences between the Lite and the Full version.	WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for more information on the differences between the Lite and the Full version.
This is a Lite version of ISim.	This is a Lite version of ISim.
Time resolution is 1 ps	Time resolution is 1 ps
Simulator is doing circuit initialization process.	Simulator is doing circuit initialization process.
Finished circuit initialization process.	Finished circuit initialization process.

>xst -ifn CORDIC_FSM.xst	>xst -ifn CORDIC_FSM.xst
Release 14.7 - xst P.20131013 (n654)	Release 14.7 - xst P.20131013 (n654)
Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.	Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.
-> Parameter TMPDIR set to /xstprocnar/tmp	-> Parameter TMPDIR set to /xstprocnar/tmp
Total REAL time to Xst completion: 0.00 secs	Total REAL time to Xst completion: 1.00 secs
Total CPU time to Xst completion: 0.23 secs	Total CPU time to Xst completion: 0.27 secs
-> WARNING:Xst:3164 - Option "-debug" found multiple times in the command line. Only the first occurrence is considered.	-> WARNING:Xst:3164 - Option "-debug" found multiple times in the command line. Only the first occurrence is considered.
* HDL Compilation	* HDL Compilation
Compiling vhdl file "cordic_fsm.vhd" in Library work.	Compiling vhdl file "cordic_fsm.vhd" in Library work.
Entity <CORDIC_FSM> compiled.	Entity <CORDIC_FSM> compiled.
Entity <CORDIC_FSM> (Architecture <rtl>) compiled.	Entity <CORDIC_FSM> (Architecture <rtl>) compiled.
Total REAL time to Xst completion: 0.00 secs	Total REAL time to Xst completion: 1.00 secs
Total CPU time to Xst completion: 0.29 secs	Total CPU time to Xst completion: 0.35 secs
->	->
Total memory usage is 4468996 kilobytes	Total memory usage is 4468936 kilobytes
Number of errors : 0 (0 filtered)	Number of errors : 0 (0 filtered)
Number of warnings : 1 (0 filtered)	Number of warnings : 1 (0 filtered)
Number of infos : 0 (0 filtered)	Number of infos : 0 (0 filtered)
->fuse -incremental -o CORDIC_FSM_tb.isim_beh.exe -pri CORDIC_FSM_tb.pri -top CORDIC_FSM_tb	->fuse -incremental -o CORDIC_FSM_tb.isim_beh.exe -pri CORDIC_FSM_tb.pri -top CORDIC_FSM_tb
(Sim P.20131013 (signature 0x708090))	(Sim P.20131013 (signature 0x708090))
Number of CPUs detected in this system: 8	Number of CPUs detected in this system: 8
Turning on multi-threading, number of parallel sub-compilation jobs: 16	Turning on multi-threading, number of parallel sub-compilation jobs: 16
Determining compilation order of HDL files	Determining compilation order of HDL files
Parsing VHDL file "cordic_fsm.vhd" into library work	Parsing VHDL file "cordic_fsm.vhd" into library work
Parsing VHDL file "CORDIC_FSM_tb.vhd" into library work	Parsing VHDL file "CORDIC_FSM_tb.vhd" into library work
Starting static elaboration	Starting static elaboration
Completed static elaboration	Completed static elaboration
Compiling package standard	Compiling package standard
Compiling package std_logic_1164	Compiling package std_logic_1164
Compiling package numeric_std	Compiling package numeric_std
Compiling package textio	Compiling package textio
Compiling package std_logic_textio	Compiling package std_logic_textio
Compiling architecture rtl of entity CORDIC_FSM (cordic_fsm_default)	Compiling architecture rtl of entity CORDIC_FSM (cordic_fsm_default)
Compiling architecture rtl of entity cordic_fsm_tb	Compiling architecture rtl of entity cordic_fsm_tb
Time Resolution for simulation is 1ps.	Time Resolution for simulation is 1ps.
Waiting for 1 sub-compilation(s) to finish...	Waiting for 1 sub-compilation(s) to finish...
Compiled 8 VHDL Units	Compiled 8 VHDL Units
Built simulation executable CORDIC_FSM_tb.isim_beh.exe	Built simulation executable CORDIC_FSM_tb.isim_beh.exe
Fuse Memory Usage: 36796 KB	Fuse Memory Usage: 36780 KB
Fuse CPU Usage: 811 ms	Fuse CPU Usage: 859 ms
->CORDIC_FSM_tb.isim_beh.exe -icbatch isim.tcl -wdb CORDIC_FSM_tb.isim_beh.wdb	->CORDIC_FSM_tb.isim_beh.exe -icbatch isim.tcl -wdb CORDIC_FSM_tb.isim_beh.wdb
(Sim P.20131013 (signature 0x708090))	(Sim P.20131013 (signature 0x708090))
WARNING: A WEBPACK license was found.	WARNING: A WEBPACK license was found.
WARNING: Please use Xilinx License Configuration Manager to check out a full ISim license.	WARNING: Please use Xilinx License Configuration Manager to check out a full ISim license.
WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for more information on the differences between the Lite and the Full version.	WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for more information on the differences between the Lite and the Full version.
This is a Lite version of ISim.	This is a Lite version of ISim.
Time resolution is 1 ps	Time resolution is 1 ps
Simulator is doing circuit initialization process.	Simulator is doing circuit initialization process.
Finished circuit initialization process.	Finished circuit initialization process.

>xst -ifn CORDIC_FSM.xst	>xst -ifn CORDIC_FSM.xst
Release 14.7 - xst P.20131013 (n654)	Release 14.7 - xst P.20131013 (n654)
Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.	Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.
-> Parameter TMPDIR set to /xstprocnar/tmp	-> Parameter TMPDIR set to /xstprocnar/tmp
Total REAL time to Xst completion: 0.60 secs	Total REAL time to Xst completion: 1.00 secs
Total CPU time to Xst completion: 0.23 secs	Total CPU time to Xst completion: 0.27 secs
-> WARNING:Xst:3164 - Option "-debug" found multiple times in the command line. Only the first occurrence is considered.	-> WARNING:Xst:3164 - Option "-debug" found multiple times in the command line. Only the first occurrence is considered.
* HDL Compilation	* HDL Compilation
Compiling vhdl file "cordic_fsm.vhd" in Library work.	Compiling vhdl file "cordic_fsm.vhd" in Library work.
Entity <CORDIC_FSM> compiled.	Entity <CORDIC_FSM> compiled.
Entity <CORDIC_FSM> (Architecture <rtl>) compiled.	Entity <CORDIC_FSM> (Architecture <rtl>) compiled.
Total REAL time to Xst completion: 0.60 secs	Total REAL time to Xst completion: 1.00 secs
Total CPU time to Xst completion: 0.65 secs	Total CPU time to Xst completion: 0.35 secs
->	->
Total memory usage is 4468928 kilobytes	Total memory usage is 4468936 kilobytes
Number of errors : 0 (0 filtered)	Number of errors : 0 (0 filtered)
Number of warnings : 1 (0 filtered)	Number of warnings : 1 (0 filtered)
Number of infos : 0 (0 filtered)	Number of infos : 0 (0 filtered)
->fuse -incremental -o CORDIC_FSM_tb.isim_beh.exe -pri CORDIC_FSM_tb.pri -top CORDIC_FSM_tb	->fuse -incremental -o CORDIC_FSM_tb.isim_beh.exe -pri CORDIC_FSM_tb.pri -top CORDIC_FSM_tb
(ISim P.20131013 (signature 0x708090))	(ISim P.20131013 (signature 0x708090))
Number of CPUs detected in this system: 8	Number of CPUs detected in this system: 8
Turning on multi-threading, number of parallel sub-compilation jobs: 16	Turning on multi-threading, number of parallel sub-compilation jobs: 16
Determining compilation order of HDL files	Determining compilation order of HDL files
Parsing VHDL file "cordic_fsm.vhd" into library work	Parsing VHDL file "cordic_fsm.vhd" into library work
Parsing VHDL file "CORDIC_FSM_tb.vhd" into library work	Parsing VHDL file "CORDIC_FSM_tb.vhd" into library work
Starting static elaboration	Starting static elaboration
Completed static elaboration	Completed static elaboration
Compiling package standard	Compiling package standard
Compiling package std_logic_1164	Compiling package std_logic_1164
Compiling package numeric_std	Compiling package numeric_std
Compiling package textio	Compiling package textio
Compiling package std_logic_textio	Compiling package std_logic_textio
Compiling architecture rtl of entity CORDIC_FSM (cordic_fsm_default)	Compiling architecture rtl of entity CORDIC_FSM (cordic_fsm_default)
Compiling architecture rtl of entity cordic_fsm_tb	Compiling architecture rtl of entity cordic_fsm_tb
Time Resolution for simulation is 1ps.	Time Resolution for simulation is 1ps.
Waiting for 1 sub-compilation(s) to finish...	Waiting for 1 sub-compilation(s) to finish...
Compiled 8 VHDL Units	Compiled 8 VHDL Units
Built simulation executable CORDIC_FSM_tb.isim_beh.exe	Built simulation executable CORDIC_FSM_tb.isim_beh.exe
Fuse Memory Usage: 36540 KB	Fuse Memory Usage: 36750 KB
Fuse CPU Usage: 755 ms	Fuse CPU Usage: 859 ms
->CORDIC_FSM_tb.isim_beh.exe -icbatch isim.tcl -wdb CORDIC_FSM_tb.isim_beh.wdb	->CORDIC_FSM_tb.isim_beh.exe -icbatch isim.tcl -wdb CORDIC_FSM_tb.isim_beh.wdb
(ISim P.20131013 (signature 0x708090))	(ISim P.20131013 (signature 0x708090))
WARNING: A WEBPACK license was found.	WARNING: A WEBPACK license was found.
WARNING: Please use Xilinx License Configuration Manager to check out a full ISim license.	WARNING: Please use Xilinx License Configuration Manager to check out a full ISim license.
WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for more information on the differences between the Lite and the Full version.	WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for more information on the differences between the Lite and the Full version.
This is a Lite version of ISim.	This is a Lite version of ISim.
Time resolution is 1 ps	Time resolution is 1 ps
Simulator is doing circuit initialization process.	Simulator is doing circuit initialization process.
Finished circuit initialization process.	Finished circuit initialization process.

```

>xst -ifn CORDIC_FSM.xst
Release 14.7 - xst P.20131013 (nt64)
Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.
--> Parameter TMPDIR set to ./xst/projnav.tmp
Total REAL time to Xst completion: 1.00 secs
Total CPU time to Xst completion: 0.27 secs

--> WARNING:Xst:3164 - Option "-debug" found multiple times in the command line. Only the first occurrence
*          HDL Compilation          *
Compiling vhdl file "/cordic_fsm.vhd" in Library work.
Entity <CORDIC_FSM> compiled.
Entity <CORDIC_FSM> (Architecture <rtl>) compiled.
Total REAL time to Xst completion: 1.00 secs
Total CPU time to Xst completion: 0.35 secs

-->
Total memory usage is 4468936 kilobytes
Number of errors   : 0 ( 0 filtered)
Number of warnings : 1 ( 0 filtered)
Number of infos   : 0 ( 0 filtered)
>fuse -incremental -o CORDIC_FSM_tb_isim_beh.exe -prj CORDIC_FSM_tb.prj -top CORDIC_FSM_tb
ISim P.20131013 (signature 0x7708f090)
Number of CPUs detected in this system: 8
Turning on mult-threading, number of parallel sub-compilation jobs: 16
Determining compilation order of HDL files
Parsing VHDL file "cordic_fsm.vhd" into library work
Parsing VHDL file "CORDIC_FSM_tb.vhd" into library work
Starting static elaboration
Completed static elaboration
Compiling package standard
Compiling package std_logic_1164
Compiling package numeric_std
Compiling package textio
Compiling package std_logic_textio
Compiling architecture rtl of entity CORDIC_FSM [cordic_fsm_default]
Compiling architecture rtl of entity cordic_fsm_tb
Time Resolution for simulation is 1ps.
Waiting for 1 sub-compilation(s) to finish...
Compiled 8 VHDL Units
Built simulation executable CORDIC_FSM_tb_isim_beh.exe
Fuse Memory Usage: 36780 KB
Fuse CPU Usage: 859 ms
>CORDIC_FSM_tb_isim_beh.exe -tclbatch isim.tcl -wdb CORDIC_FSM_tb_isim_beh.wdb
ISim P.20131013 (signature 0x7708f090)
WARNING: A WEBPACK license was found.
WARNING: Please use Xilinx License Configuration Manager to check out a full ISim license.
WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for more information on t
This is a Lite version of ISim.
Time resolution is 1 ps
Simulator is doing circuit initialization process.
Finished circuit initialization process.

```

rence is considered.

»

.he differences between the Lite and the Full version.