

POVZETEK PORABE ELEMENTOV IN ZAKASNITEV VEZJA

Tabela 1: CLA_ADDER.

VPISNA ŠTEVILKA	BELS	LUT2	LUT3	LUT4	LUT5	LUT6	MUXF7	IO BUFFER	IBUF	OBUF	DELAY (NS)
64000225	24	6	3		6	9		28	17	11	9.101
64190088	24	6	3		6	9		28	17	11	9.101
64200100	24	6	3		6	9		28	17	11	9.101
64200112	24	6	3		6	9		28	17	11	9.101
64200163	24	6	3		6	9		28	17	11	9.101
64200238	24	6	3		6	9		28	17	11	9.101
64200288	24	6	3		6	9		28	17	11	9.101
64200296	24	6	3		6	9		28	17	11	9.101
64200385	24	3	4	2	5	9	1	28	17	11	8.614
64210113	24	6	3		6	9		28	17	11	9.101
64210290	24	6	3		6	9		28	17	11	9.101
64210382	24	6	3		6	9		28	17	11	9.101
64210384	24	6	5		6	7		28	17	11	9.092
64210386	23	6	4		8	5		28	17	11	8.399
64210445	24	6	3		6	9		28	17	11	9.101
64210455	Number of errors : 2 (0 filtered)										
64210457	24	6	3		6	9		28	17	11	9.101
64240429	24	6	3		6	9		28	17	11	9.101
64240430	24	6	3		6	9		28	17	11	9.101
IDEAL	24	6	3		6	9		28	17	11	9.101

Tabela 2: ALU.

VPISNA ŠTEVILKA	BELS	LUT3	LUT4	LUT5	LUT6	MUXF7	IO BUFFER	IBUF	OBUF	DELAY (NS)
64000225	60	4		14	41	1	34	20	14	11.168
64190088	52	2		14	35	1	34	20	14	11.074
64200100	60	4		14	41	1	34	20	14	11.168
64200112	49	3		14	30	2	34	20	14	12.446
64200163	49	3		14	30	2	34	20	14	12.446
64200238	60	4		14	41	1	34	20	14	11.168
64200288	60	4		14	41	1	34	20	14	11.168
64200296	49	2		15	30	2	34	20	14	12.446
64200385	49	3	2	13	28	3	34	20	14	11.603
64210113	60	4		14	41	1	34	20	14	11.168
64210290	59	3		15	40	1	34	20	14	11.892
64210382	60	4		14	41	1	34	20	14	11.168
64210384	52	1		13	34	4	34	20	14	12.374
64210386	60	6		16	37	1	34	20	14	11.632
64210445	60	4		14	41	1	34	20	14	11.168
64210455	Number of errors : 2 (0 filtered)									
64210457	60	4		14	41	1	34	20	14	11.168
64240429	52	2		7	42	1	34	20	14	11.074
64240430	52	1		13	34	4	34	20	14	12.374
IDEAL	62	4		13	43	2	34	20	14	11.243

OCENJEVANJE POTEKA SINTEZE

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Number of errors : 1 (0 filtered)	60
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Number of errors : 1 (0 filtered)	70
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Number of errors : 1 (0 filtered)	78
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-- -----	83
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-- -- - - - - - ..... 93
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# LUT6 : 30 ..... 101
# MUXF7 : 2 ..... 101
# IO Buffers : 34 ..... 101
# IBUF : 20 ..... 101
# OBUF : 14 ..... 101

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Number of errors : 1 (0 filtered)	106
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Primitive and Black Box Usage:	111
-- --	111
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# LUT6 : 9	111
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Number of errors : 0 (0 filtered)	113
Number of errors : 1 (0 filtered)	114
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-- --	119
# BELS : 60	119
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# LUT5 : 14	119
# LUT6 : 41	119
# MUXF7 : 1	119
# IO Buffers : 34	119
# IBUF : 20	119
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Device utilization summary:	119
Maximum combinational path delay: 11.168ns	120
Number of errors : 0 (0 filtered)	121
Number of errors : 1 (0 filtered)	124
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Primitive and Black Box Usage:	129
-- --	129
# BELS : 24	129

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Primitive and Black Box Usage:	137
-- -- -- -- -- -- -- -- --	137
# BELS : 60	137
# LUT3 : 4	137
# LUT5 : 14	137
# LUT6 : 41	137
# MUXF7 : 1	137
# IO Buffers : 34	137
# IBUF : 20	137
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Device utilization summary:	137
Maximum combinational path delay: 11.168ns	138
Number of errors : 0 (0 filtered)	139
Number of errors : 1 (0 filtered)	142
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-- -- -- -- -- -- -- -- --	147
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# LUT2 : 6	147
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# IO Buffers : 28	147
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Number of errors : 1 (0 filtered)	150
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-- --	155
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-- --	165
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-- --	173

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Maximum combinational path delay: 11.603ns	174
Number of errors : 0 (0 filtered).....	175
Number of errors : 1 (0 filtered).....	178
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-- -----	183
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Number of errors : 0 (0 filtered).....	185
Number of errors : 1 (0 filtered).....	186
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-- -----	191
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Number of errors : 1 (0 filtered)	196
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Number of errors : 0 (0 filtered)	203
Number of errors : 1 (0 filtered)	204
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-- -----	209
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Device utilization summary:	255
Maximum combinational path delay: 8.399ns	256
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Maximum combinational path delay: 9.101ns	337
Number of errors : 0 (0 filtered)	338
Number of errors : 1 (0 filtered)	339
Top Level Output File Name : alu_cla.ngc	344
Primitive and Black Box Usage:	344
-- -----	344
# BELS : 52	344
# LUT3 : 1	344
# LUT5 : 13	344
# LUT6 : 34	344
# MUXF7 : 4	344
# IO Buffers : 34	344
# IBUF : 20	344
# OBUF : 14	344
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Number of errors : 0 (0 filtered)	346
Number of errors : 1 (0 filtered)	349
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-- -----	354
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# LUT2 : 6	354
# LUT3 : 3	354
# LUT5 : 6	354
# LUT6 : 9	354
# IO Buffers : 28	354
# IBUF : 17	354
# OBUF : 11	354
Device utilization summary:	354
Maximum combinational path delay: 9.101ns	355
Number of errors : 0 (0 filtered)	356

Number of errors : 1 (0 filtered)	357
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Primitive and Black Box Usage:	362
-- -- -- -- --	362
# BELS : 62	362
# LUT3 : 4	362
# LUT5 : 13	362
# LUT6 : 43	362
# MUXF7 : 2	362
# IO Buffers : 34	362
# IBUF : 20	362
# OBUF : 14	362
Device utilization summary:	362
Maximum combinational path delay: 11.243ns	363
Number of errors : 0 (0 filtered)	364
Number of errors : 1 (0 filtered)	367

```
-- *****
-- **** STUDENT: 64000225
-- *****
-- KOMENTARJI K OCENI NALOGE
-- Matej Možek: Ni pripomb
-- *****
```

```
64000225>rem ***** test cla adder
```

```
64000225>if not exist "xst" mkdir xst
```

```
64000225>cd XST
```

```
64000225\xst>if not exist "projnav.tmp" mkdir "projnav.tmp"
```

```
64000225\xst>cd ..
```

```
64000225>rem ***** test cla operations
```

```
64000225>xst -ifn cla_add_n_bit.xst
Release 14.7 - xst P.20131013 ( nt64 )
Copyright ( c ) 1995-2013 Xilinx, Inc. All rights reserved.
-- > Parameter TMPDIR set to xst/projnav.tmp
```

```
Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.23 secs
```

```
-- > Parameter xsthdpdir set to xst
```

```
Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.23 secs
```

```
-- >
```

```
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- 8.4.5) Cross Clock Domains Report

```
=====
* Synthesis Options Summary *
```

```
=====
-- -- Source Parameters
```

```
Input File Name : "cla_add_n_bit.prj"
```

Ignore Synthesis Constraint File : NO

-- -- Target Parameters

Output File Name : "cla_add_n_bit"

Output Format : NGC

Target Device : xc6slx4-3-tqg144

-- -- Source Options

Top Module Name : cla_add_n_bit

Automatic FSM Extraction : YES

FSM Encoding Algorithm : Auto

Safe Implementation : No

FSM Style : LUT

RAM Extraction : Yes

RAM Style : Auto

ROM Extraction : Yes

Shift Register Extraction : YES

ROM Style : Auto

Resource Sharing : YES

Asynchronous To Synchronous : NO

Shift Register Minimum Size : 2

Use DSP Block : Auto

Automatic Register Balancing : No

-- -- Target Options

LUT Combining : Auto

Reduce Control Sets : Auto

Add IO Buffers : YES

Global Maximum Fanout : 100000

Add Generic Clock Buffer(BUFG) : 16

Register Duplication : YES

Optimize Instantiated Primitives : NO

Use Clock Enable : Auto

Use Synchronous Set : Auto

Use Synchronous Reset : Auto

Pack IO Registers into IOBs : Auto

Equivalent register Removal : YES

-- -- General Options

Optimization Goal : Speed

Optimization Effort : 1

Power Reduction : NO

Keep Hierarchy : No

Netlist Hierarchy : As_Optimized

RTL Output : Yes

Global Optimization : AllClockNets

Read Cores : YES

Write Timing Constraints : NO

Cross Clock Analysis : NO

Hierarchy Separator : /

Bus Delimiter : <>

Case Specifier : Maintain

Slice Utilization Ratio : 100

BRAM Utilization Ratio : 100

DSP48 Utilization Ratio : 100

Auto BRAM Packing : NO

Slice Utilization Ratio Delta : 5

=====

```

=====
* HDL Parsing *
=====
Parsing VHDL file "64000225\cla_gp.vhd" into library work
Parsing entity <cla_gp>.
Parsing architecture <ideal> of entity <cla_gp>.
Parsing VHDL file "64000225\cla_add_n_bit.vhd" into library work
Parsing entity <cla_add_n_bit>.
Parsing architecture <NDV> of entity <cla_add_n_bit>.

=====
* HDL Elaboration *
=====

Elaborating entity <cla_add_n_bit> ( architecture <NDV> ) with generics from
library <work>.

=====
* HDL Synthesis *
=====

Synthesizing Unit <cla_add_n_bit>.
Related source file is "64000225\cla_add_n_bit.vhd".
  n = 8
  Summary:
Unit <cla_add_n_bit> synthesized.

=====
HDL Synthesis Report

Macro Statistics
# Xors : 16
  1-bit xor2 : 16

=====

=====
* Advanced HDL Synthesis *
=====

=====
Advanced HDL Synthesis Report

Macro Statistics
# Xors : 16
  1-bit xor2 : 16

=====

=====
* Low Level Synthesis *
=====

Optimizing unit <cla_add_n_bit> ...

Mapping all equations...
Building and optimizing final netlist ...

```

Found area constraint ratio of 100 (+ 5) on block cla_add_n_bit, actual ratio is 1.

Final Macro Processing ...

=====
Final Register Report

Found no macro

=====
* Partition Report *
=====

Partition Implementation Status

-- -- -- -- -- -- -- -- -- -- -- -- -- --
-- -- -

No Partitions were found in this design.

-- -- -- -- -- -- -- -- -- -- -- -- -- --
-- -- -

=====
* Design Summary *
=====

Top Level Output File Name : cla_add_n_bit.ngc

Primitive and Black Box Usage:

-- -- -- -- -- -- -- -- -- -- -- -- -- --
-- --

BELS : 24
LUT2 : 6
LUT3 : 3
LUT5 : 6
LUT6 : 9
IO Buffers : 28
IBUF : 17
OBUF : 11

Device utilization summary:

-- -- -- -- -- -- -- -- -- -- -- -- -- --
-

Selected Device : 6slx4tqg144-3

Slice Logic Utilization:

Number of Slice LUTs: 24 out of 2400 1%
Number used as Logic: 24 out of 2400 1%

Slice Logic Distribution:

Number of LUT Flip Flop pairs used: 24
Number with an unused Flip Flop: 24 out of 24 100%
Number with an unused LUT: 0 out of 24 0%
Number of fully used LUT-FF pairs: 0 out of 24 0%
Number of unique control sets: 0

IO Utilization:

Number of IOs: 28

Number of bonded IOBs: 28 out of 102 27%

Specific Feature Utilization:

```
-- -- -- -- -- -- -- -- -- -- -- -- -- --  
-
```

Partition Resource Summary:

```
-- -- -- -- -- -- -- -- -- -- -- -- -- --  
-
```

No Partitions were found in this design.

```
-- -- -- -- -- -- -- -- -- -- -- -- -- --  
-
```

=====
Timing Report

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.

FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT
GENERATED AFTER PLACE-and-ROUTE.

Clock Information:

```
-- -- -- -- -- -- -- -- -- -- -- -- -- --
```

No clock signals found in this design

Asynchronous Control Signals Information:

```
-- -- -- -- -- -- -- -- -- -- -- -- -- --  
-- -- -- -- -- -- -- -- -- -- -- -- -- --
```

No asynchronous control signals found in this design

Timing Summary:

```
-- -- -- -- -- -- -- -- -- -- -- -- -- --
```

Speed Grade: -3

Minimum period: No path found

Minimum input arrival time before clock: No path found

Maximum output required time after clock: No path found

Maximum combinational path delay: 9.101ns

Timing Details:

```
-- -- -- -- -- -- -- -- -- -- -- -- -- --
```

All values displayed in nanoseconds (ns)

=====
Timing constraint: Default path analysis

Total number of paths / destination ports: 131 / 11

```
-- -- -- -- -- -- -- -- -- -- -- -- -- --  
-- -- -- -- -- -- -- -- -- -- -- -- -- --  
-- -- -- -- -- -- -- -- -- -- -- -- -- --
```

Delay: 9.101ns (Levels of Logic = 7)

Source: Y<0> (PAD)

Destination: S<7> (PAD)

Data Path: Y<0> to S<7>

Gate Net

Cell:in->out fanout Delay Delay Logical Name (Net Name)

```

--      --      --      --      --      --      --      --      --      --      --
--      --      --      --      --      --      --      --      --      --      --
--      --
IBUF:I->0 6 1.222 0.973 Y_0_IBUF ( Y_0_IBUF )
LUT3:I0->0 2 0.205 0.617 C<3>_SW0 ( N2 )
LUT5:I4->0 3 0.205 0.651 C<3> ( C<3> )
LUT3:I2->0 2 0.205 0.617 C<6>_SW0 ( N4 )
LUT5:I4->0 2 0.205 0.845 C<6> ( C<6> )
LUT5:I2->0 1 0.205 0.579 Mxor_S_sig<7>_xo<0>1 ( S_7_OBUF )
OBUF:I->0 2.571 S_7_OBUF ( S<7> )
--      --      --      --      --      --      --      --      --      --      --
--      --      --      --      --      --      --      --      --      --      --
Total 9.101ns ( 4.818ns logic, 4.283ns route )
( 52.9% logic, 47.1% route )

```

Cross Clock Domains Report:

```

Total REAL time to Xst completion: 8.00 secs
Total CPU time to Xst completion: 7.88 secs

```

```
-- >
```

Total memory usage is 4487500 kilobytes

Number of errors : 0 (0 filtered)

Number of warnings : 0 (0 filtered)

Number of infos : 0 (0 filtered)

```

64000225>fuse -incremental -o cla_add_n_bit_tb_isim_beh.exe -prj
cla_add_n_bit_tb.prj -top cla_add_n_bit_tb
Running: \unwrapped\fuse.exe -incremental -o cla_add_n_bit_tb_isim_beh.exe -prj
cla_add_n_bit_tb.prj -top cla_add_n_bit_tb
ISim P.20131013 ( signature 0x7708f090 )
Number of CPUs detected in this system: 8
Turning on mult-threading, number of parallel sub-compilation jobs: 16
Determining compilation order of HDL files
Parsing VHDL file "cla_gp.vhd" into library work
Parsing VHDL file "cla_add_n_bit.vhd" into library work
Parsing VHDL file "cla_add_n_bit_tb_IDEAL.vhd" into library work
Starting static elaboration
Completed static elaboration
Compiling package standard
Compiling package std_logic_1164
Compiling package textio
Compiling package std_logic_textio
Compiling package numeric_std
Compiling package attributes
Compiling package std_logic_misc
Compiling architecture ndv of entity cla_add_n_bit [\cla_add_n_bit( 8 )\]
Compiling architecture testbench_arch of entity cla_add_n_bit_tb
Time Resolution for simulation is 1ps.
Compiled 10 VHDL Units
Built simulation executable cla_add_n_bit_tb_isim_beh.exe
Fuse Memory Usage: 37444 KB

```

Fuse CPU Usage: 890 ms

```
64000225>cla_add_n_bit_tb_isim_beh.exe -tclbatch isim.tcl -wdb
cla_add_n_bit_tb_isim_beh.wdb
ISim P.20131013 ( signature 0x7708f090 )
WARNING: A WEBPACK license was found.
WARNING: Please use Xilinx License Configuration Manager to check out a full ISim
license.
WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for
more information on the differences between the Lite and the Full version.
This is a Lite version of ISim.
Time resolution is 1 ps
Simulator is doing circuit initialization process.
Finished circuit initialization process.
```

```
64000225>rem ***** test cla flags
```

```
64000225>xst -ifn cla_add_n_bit_flags.xst
Release 14.7 - xst P.20131013 ( nt64 )
Copyright ( c ) 1995-2013 Xilinx, Inc. All rights reserved.
-- > Parameter TMPDIR set to xst/projnav.tmp
```

```
Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.22 secs
```

```
-- > Parameter xsthdpdir set to xst
```

```
Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.22 secs
```

```
-- > ERROR:Xst:438 - Can not open file : cla_add_n_bit_flags.prj
```

```
Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.25 secs
```

```
-- >
```

Total memory usage is 4422880 kilobytes

Number of errors : 1 (0 filtered)

Number of warnings : 0 (0 filtered)

Number of infos : 0 (0 filtered)

```
64000225>fuse -incremental -o cla_add_n_bit_tb_flags_isim_beh.exe -prj
cla_add_n_bit_flags_tb.prj -top cla_add_n_bit_flags_tb_IDEAL
Running: \unwrapped\fuse.exe -incremental -o cla_add_n_bit_tb_flags_isim_beh.exe -
prj cla_add_n_bit_flags_tb.prj -top cla_add_n_bit_flags_tb_IDEAL
ISim P.20131013 ( signature 0x7708f090 )
Number of CPUs detected in this system: 8
Turning on mult-threading, number of parallel sub-compilation jobs: 16
Determining compilation order of HDL files
Parsing VHDL file "cla_gp.vhd" into library work
Parsing VHDL file "cla_add_n_bit.vhd" into library work
Parsing VHDL file "cla_add_n_bit_flags_tb_IDEAL.vhd" into library work
Starting static elaboration
Completed static elaboration
Compiling package standard
Compiling package std_logic_1164
Compiling package textio
```



```

Compiling package std_logic_textio
Compiling package numeric_std
Compiling package attributes
Compiling package std_logic_misc
Compiling architecture ndv of entity cla_add_n_bit [\cla_add_n_bit( 8 )\]
Compiling architecture a1 of entity cla_add_n_bit_flags_tb_ideal
Time Resolution for simulation is 1ps.
Waiting for 1 sub-compilation( s ) to finish...
Compiled 10 VHDL Units
Built simulation executable cla_add_n_bit_tb_flags_isim_beh.exe
Fuse Memory Usage: 37496 KB
Fuse CPU Usage: 874 ms

64000225>cla_add_n_bit_tb_flags_isim_beh.exe -tclbatch isim.tcl -wdb
cla_add_n_bit_flags_tb.wdb
ISim P.20131013 ( signature 0x7708f090 )
WARNING: A WEBPACK license was found.
WARNING: Please use Xilinx License Configuration Manager to check out a full ISim
license.
WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for
more information on the differences between the Lite and the Full version.
This is a Lite version of ISim.
Time resolution is 1 ps
Simulator is doing circuit initialization process.
Finished circuit initialization process.

64000225>rem ***** test alu operations

64000225>xst -ifn alu_cla.xst
Release 14.7 - xst P.20131013 ( nt64 )
Copyright ( c ) 1995-2013 Xilinx, Inc. All rights reserved.
-- > Parameter TMPDIR set to xst/projnav.tmp

Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.24 secs

-- > Parameter xsthdpdir set to xst

Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.24 secs

-- >
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8.4.2 ) Asynchronous Control Signals Information

```

- 8.4.3) Timing Summary
- 8.4.4) Timing Details
- 8.4.5) Cross Clock Domains [Report](#)

```
=====
* Synthesis Options Summary *
=====
--      -- Source Parameters
Input File Name : "alu_cla.prj"
Ignore Synthesis Constraint File : NO

--      -- Target Parameters
Output File Name : "alu_cla"
Output Format : NGC
Target Device : xc6slx4-3-tqg144

--      -- Source Options
Top Module Name : alu_cla
Automatic FSM Extraction : YES
FSM Encoding Algorithm : Auto
Safe Implementation : No
FSM Style : LUT
RAM Extraction : Yes
RAM Style : Auto
ROM Extraction : Yes
Shift Register Extraction : YES
ROM Style : Auto
Resource Sharing : YES
Asynchronous To Synchronous : NO
Shift Register Minimum Size : 2
Use DSP Block : Auto
Automatic Register Balancing : No

--      -- Target Options
LUT Combining : Auto
Reduce Control Sets : Auto
Add IO Buffers : YES
Global Maximum Fanout : 100000
Add Generic Clock Buffer( BUFG ) : 16
Register Duplication : YES
Optimize Instantiated Primitives : NO
Use Clock Enable : Auto
Use Synchronous Set : Auto
Use Synchronous Reset : Auto
Pack IO Registers into IOBs : Auto
Equivalent register Removal : YES

--      -- General Options
Optimization Goal : Speed
Optimization Effort : 1
Power Reduction : NO
Keep Hierarchy : No
Netlist Hierarchy : As_Optimized
RTL Output : Yes
Global Optimization : AllClockNets
Read Cores : YES
Write Timing Constraints : NO
Cross Clock Analysis : NO
Hierarchy Separator : /
```

Bus Delimiter : <>
Case Specifier : Maintain
Slice Utilization Ratio : 100
BRAM Utilization Ratio : 100
DSP48 Utilization Ratio : 100
Auto BRAM Packing : NO
Slice Utilization Ratio Delta : 5

=====

* HDL Parsing *

=====

Parsing VHDL file "64000225\cla_gp.vhd" into library work
Parsing entity <cla_gp>.
Parsing architecture <ideal> of entity <cla_gp>.
Parsing VHDL file "64000225\cla_add_n_bit.vhd" into library work
Parsing entity <cla_add_n_bit>.
Parsing architecture <NDV> of entity <cla_add_n_bit>.
Parsing VHDL file "64000225\alu_cla.vhd" into library work
Parsing entity <alu_cla>.
Parsing architecture <NDV> of entity <alu_cla>.

=====

* HDL Elaboration *

=====

Elaborating entity <alu_cla> (architecture <NDV>) with generics from library <work>.

Elaborating entity <cla_add_n_bit> (architecture <NDV>) with generics from library <work>.

=====

* HDL Synthesis *

=====

Synthesizing Unit <alu_cla>.
Related source file is "64000225\alu_cla.vhd".
n = 8
Found 8-bit 12-to-1 multiplexer for signal <S> created at line 61.
Summary:
inferred 19 Multiplexer(s).
Unit <alu_cla> synthesized.

Synthesizing Unit <cla_add_n_bit>.
Related source file is "64000225\cla_add_n_bit.vhd".
n = 8
Summary:
Unit <cla_add_n_bit> synthesized.

=====

HDL Synthesis Report

Macro Statistics

Multiplexers : 19
1-bit 2-to-1 multiplexer : 12
8-bit 12-to-1 multiplexer : 1
8-bit 2-to-1 multiplexer : 6

```
# Xors : 17
 1-bit xor2 : 16
 8-bit xor2 : 1
```

=====

=====

```
* Advanced HDL Synthesis *
```

=====

=====

Advanced HDL Synthesis Report

Macro Statistics

```
# Multiplexers : 19
 1-bit 2-to-1 multiplexer : 12
 8-bit 12-to-1 multiplexer : 1
 8-bit 2-to-1 multiplexer : 6
# Xors : 17
 1-bit xor2 : 16
 8-bit xor2 : 1
```

=====

=====

```
* Low Level Synthesis *
```

=====

Optimizing unit <alu_cla> ...

Optimizing unit <cla_add_n_bit> ...

Mapping all equations...

Building and optimizing final netlist ...

Found area constraint ratio of 100 (+ 5) on block alu_cla, actual ratio is 3.

Final Macro Processing ...

=====

Final Register Report

Found no macro

=====

=====

```
* Partition Report *
```

=====

Partition Implementation Status

```
--      --      --      --      --      --      --      --      --      --      --      --
--      --      --      --      --      --      --      --      --      --      --      --
```

No Partitions were found in this design.

```
--      --      --      --      --      --      --      --      --      --      --      --
--      --      --      --      --      --      --      --      --      --      --      --
```

=====

```
* Design Summary *
```

=====

Top Level Output File Name : alu_cla.ngc

Primitive and Black Box Usage:

```
--      --      --      --      --      --      --      --      --      --      --      --
--      --      --
# BELS : 60
# LUT3 : 4
# LUT5 : 14
# LUT6 : 41
# MUXF7 : 1
# IO Buffers : 34
# IBUF : 20
# OBUF : 14
```

Device utilization summary:

```
--      --      --      --      --      --      --      --      --      --      --      --
-
```

Selected Device : 6slx4tqg144-3

Slice Logic Utilization:

Number of Slice LUTs: 59 out of 2400 2%
Number used as Logic: 59 out of 2400 2%

Slice Logic Distribution:

Number of LUT Flip Flop pairs used: 59
Number with an unused Flip Flop: 59 out of 59 100%
Number with an unused LUT: 0 out of 59 0%
Number of fully used LUT-FF pairs: 0 out of 59 0%
Number of unique control sets: 0

IO Utilization:

Number of IOs: 34
Number of bonded IOBs: 34 out of 102 33%

Specific Feature Utilization:

```
--      --      --      --      --      --      --      --      --      --      --      --
-
```

Partition Resource Summary:

```
--      --      --      --      --      --      --      --      --      --      --      --
-
```

No Partitions were found in this design.

```
--      --      --      --      --      --      --      --      --      --      --      --
-
```

=====

Timing Report

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.

FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT
GENERATED AFTER PLACE-and-ROUTE.

Clock Information:

```
--      --      --      --      --      --      --      --
```

No clock signals found in this design

Asynchronous Control Signals Information:

```
-- -- -- -- -- -- -- -- -- -- -- -- -- --
-- -- -- -- -- -- -- -- -- -- -- -- -- --
```

No asynchronous control signals found in this design

Timing Summary:

```
-- -- -- -- -- -- -- -- -- -- -- -- -- --
Speed Grade: -3
```

Minimum period: No path found

Minimum input arrival time before clock: No path found

Maximum output required time after clock: No path found

Maximum combinational path delay: 11.168ns

Timing Details:

```
-- -- -- -- -- -- -- -- -- -- -- -- -- --
All values displayed in nanoseconds ( ns )
```

=====
Timing constraint: Default path analysis

Total number of paths / destination ports: 1146 / 14

```
-- -- -- -- -- -- -- -- -- -- -- -- -- --
-- -- -- -- -- -- -- -- -- -- -- -- -- --
-- -- -- -- -- -- -- -- -- -- -- -- -- --
```

Delay: 11.168ns (Levels of Logic = 8)

Source: F<2> (PAD)

Destination: Negative (PAD)

Data Path: F<2> to Negative

Gate Net

Cell: in->out fanout Delay Delay Logical Name (Net Name)

```
-- -- -- -- -- -- -- -- -- -- -- -- -- --
-- -- -- -- -- -- -- -- -- -- -- -- -- --
-- -- -- -- -- -- -- -- -- -- -- -- -- --
```

IBUF:I->0 35 1.222 1.679 F_2_IBUF (F_2_IBUF)

LUT6:I1->0 6 0.203 0.973 Mmux_Y_sig31 (Y_sig<1>)

LUT5:I2->0 4 0.205 1.028 U1/C<3>2 (U1/C<3>)

LUT6:I1->0 1 0.203 0.000 U1/C<6>_G (N16)

MUXF7:I1->0 5 0.140 0.943 U1/C<6> (U1/C<6>)

LUT5:I2->0 3 0.205 1.015 U1/Mxor_S_sig<7>_xo<0>1 (S_sig<7>)

LUT6:I0->0 1 0.203 0.579 Mmux_Negative1 (Negative_OBUF)

OBUF:I->0 2.571 Negative_OBUF (Negative)

```
-- -- -- -- -- -- -- -- -- -- -- -- -- --
-- -- -- -- -- -- -- -- -- -- -- -- -- --
```

Total 11.168ns (4.952ns logic, 6.216ns route)

(44.3% logic, 55.7% route)

===== Cross Clock Domains Report:

```
-- -- -- -- -- -- -- -- -- -- -- -- -- --
```

=====
Total REAL time to Xst completion: 8.00 secs

Total CPU time to Xst completion: 8.88 secs

-- >

Total memory usage is 4487500 kilobytes

Number of errors : 0 (0 filtered)

Number of warnings : 0 (0 filtered)

Number of infos : 0 (0 filtered)

64000225>fuse -incremental -o alu_cla_tb_isim_beh.exe -prj alu_cla_tb.prj -top alu_cla_tb

Running: \unwrapped\fuse.exe -incremental -o alu_cla_tb_isim_beh.exe -prj alu_cla_tb.prj -top alu_cla_tb

ISim P.20131013 (signature 0x7708f090)

Number of CPUs detected in this system: 8

Turning on mult-threading, number of parallel sub-compilation jobs: 16

Determining compilation order of HDL files

Parsing VHDL file "cla_gp.vhd" into library work

Parsing VHDL file "cla_add_n_bit.vhd" into library work

Parsing VHDL file "alu_cla.vhd" into library work

Parsing VHDL file "alu_cla_tb_IDEAL.vhd" into library work

Starting static elaboration

Completed static elaboration

Compiling package standard

Compiling package std_logic_1164

Compiling package textio

Compiling package std_logic_textio

Compiling package numeric_std

Compiling package attributes

Compiling package std_logic_misc

Compiling architecture ndv of entity cla_add_n_bit [\cla_add_n_bit(8)\]

Compiling architecture ndv of entity alu_cla [\alu_cla(8)\]

Compiling architecture testbench_arch of entity alu_cla_tb

Time Resolution for simulation is 1ps.

Waiting for 1 sub-compilation(s) to finish...

Compiled 12 VHDL Units

Built simulation executable alu_cla_tb_isim_beh.exe

Fuse Memory Usage: 37752 KB

Fuse CPU Usage: 921 ms

64000225>alu_cla_tb_isim_beh.exe -tclbatch isim.tcl -wdb alu_cla_tb_isim_beh.wdb

ISim P.20131013 (signature 0x7708f090)

WARNING: A WEBPACK license was found.

WARNING: Please use Xilinx License Configuration Manager to check out a full ISim license.

WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for more information on the differences between the Lite and the Full version.

This is a Lite version of ISim.

Time resolution is 1 ps

Simulator is doing circuit initialization process.

Finished circuit initialization process.

at 7864320 ns, Instance /alu_cla_tb/ : Warning: NUMERIC_STD.TO_UNSIGNED: vector truncated

at 8847360 ns, Instance /alu_cla_tb/ : Warning: NUMERIC_STD.TO_UNSIGNED: vector truncated

at 9830400 ns, Instance /alu_cla_tb/ : Warning: NUMERIC_STD.TO_UNSIGNED: vector truncated

at 10813440 ns, Instance /alu_cla_tb/ : Warning: NUMERIC_STD.TO_UNSIGNED: vector truncated

at 11796480 ns, Instance /alu_cla_tb/ : Warning: NUMERIC_STD.TO_UNSIGNED: vector truncated
at 12779520 ns, Instance /alu_cla_tb/ : Warning: NUMERIC_STD.TO_UNSIGNED: vector truncated
at 13762560 ns, Instance /alu_cla_tb/ : Warning: NUMERIC_STD.TO_UNSIGNED: vector truncated
at 14745600 ns, Instance /alu_cla_tb/ : Warning: NUMERIC_STD.TO_UNSIGNED: vector truncated

64000225>rem ***** test alu flags

64000225>xst -ifn alu_cla_flags.xst
Release 14.7 - xst P.20131013 (nt64)
Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.
-- > Parameter TMPDIR set to xst/projnav.tmp

Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.23 secs

-- > Parameter xsthdmdir set to xst

Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.23 secs

-- >

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=====
* Synthesis Options Summary *

=====

-- -- Source Parameters

Input File Name : "alu_cla_flags_tb.prj"
Ignore Synthesis Constraint File : NO

-- -- Target Parameters

Output File Name : "alu_cla_flags_tb"
Output Format : NGC
Target Device : xc6slx4-3-tqg144

-- -- Source Options

Top Module Name : alu_cla_flags_tb
Automatic FSM Extraction : YES
FSM Encoding Algorithm : Auto
Safe Implementation : No
FSM Style : LUT
RAM Extraction : Yes
RAM Style : Auto
ROM Extraction : Yes
Shift Register Extraction : YES
ROM Style : Auto
Resource Sharing : YES
Asynchronous To Synchronous : NO
Shift Register Minimum Size : 2
Use DSP Block : Auto
Automatic Register Balancing : No

-- -- Target Options

LUT Combining : Auto
Reduce Control Sets : Auto
Add IO Buffers : YES
Global Maximum Fanout : 100000
Add Generic Clock Buffer(BUFG) : 16
Register Duplication : YES
Optimize Instantiated Primitives : NO
Use Clock Enable : Auto
Use Synchronous Set : Auto
Use Synchronous Reset : Auto
Pack IO Registers into IOBs : Auto
Equivalent register Removal : YES

-- -- General Options

Optimization Goal : Speed
Optimization Effort : 1
Power Reduction : NO
Keep Hierarchy : No
Netlist Hierarchy : As_Optimized
RTL Output : Yes
Global Optimization : AllClockNets
Read Cores : YES
Write Timing Constraints : NO
Cross Clock Analysis : NO
Hierarchy Separator : /
Bus Delimiter : <>
Case Specifier : Maintain
Slice Utilization Ratio : 100
BRAM Utilization Ratio : 100
DSP48 Utilization Ratio : 100
Auto BRAM Packing : NO
Slice Utilization Ratio Delta : 5

=====

=====

* HDL Parsing *

=====

Parsing VHDL file "64000225\cla_gp.vhd" into library work
Parsing entity <cla_gp>.
Parsing architecture <ideal> of entity <cla_gp>.
Parsing VHDL file "64000225\cla_add_n_bit.vhd" into library work

```

Parsing entity <cla_add_n_bit>.
Parsing architecture <NDV> of entity <cla_add_n_bit>.
Parsing VHDL file "64000225\alu_cla.vhd" into library work
Parsing entity <alu_cla>.
Parsing architecture <NDV> of entity <alu_cla>.
Parsing VHDL file "64000225\alu_cla_tb_FLAGS_IDEAL.vhd" into library work
Parsing entity <alu_cla_flags_tb>.
Parsing architecture <test_alu_flags> of entity <alu_cla_flags_tb>.

=====
* HDL Elaboration *
=====

Elaborating entity <alu_cla_flags_tb> ( architecture <test_alu_flags> ) with
generics from library <work>.

Elaborating entity <alu_cla> ( architecture <NDV> ) with generics from library
<work>.

Elaborating entity <cla_add_n_bit> ( architecture <NDV> ) with generics from
library <work>.
ERROR:HDLCompiler:890 - "64000225\alu_cla_tb_FLAGS_IDEAL.vhd" Line 144: wait
statement without UNTIL clause not supported for synthesis
Netlist alu_cla_flags_tb( 8 )( test_alu_flags ) remains a blackbox, due to errors
in its contents
-- >

Total memory usage is 4466680 kilobytes

Number of errors : 1 ( 0 filtered )
Number of warnings : 0 ( 0 filtered )
Number of infos : 0 ( 0 filtered )

64000225>fuse -incremental -o alu_cla_flags_tb_isim_beh.exe -prj
alu_cla_flags_tb.prj -top alu_cla_flags_tb
Running: \unwrapped\fuse.exe -incremental -o alu_cla_flags_tb_isim_beh.exe -prj
alu_cla_flags_tb.prj -top alu_cla_flags_tb
ISim P.20131013 ( signature 0x7708f090 )
Number of CPUs detected in this system: 8
Turning on mult-threading, number of parallel sub-compilation jobs: 16
Determining compilation order of HDL files
Parsing VHDL file "cla_gp.vhd" into library work
Parsing VHDL file "cla_add_n_bit.vhd" into library work
Parsing VHDL file "alu_cla.vhd" into library work
Parsing VHDL file "alu_cla_tb_FLAGS_IDEAL.vhd" into library work
Starting static elaboration
Completed static elaboration
Compiling package standard
Compiling package std_logic_1164
Compiling package textio
Compiling package std_logic_textio
Compiling package numeric_std
Compiling package attributes
Compiling package std_logic_misc
Compiling architecture ndv of entity cla_add_n_bit [\cla_add_n_bit( 8 )\]
Compiling architecture ndv of entity alu_cla [\alu_cla( 8 )\]
Compiling architecture test_alu_flags of entity alu_cla_flags_tb
Time Resolution for simulation is 1ps.
Waiting for 1 sub-compilation( s ) to finish...

```

Compiled 12 VHDL Units
Built simulation executable alu_cla_flags_tb_isim_beh.exe
Fuse Memory Usage: 37604 KB
Fuse CPU Usage: 1014 ms

```
64000225>alu_cla_flags_tb_isim_beh.exe -tclbatch isim.tcl -wdb
alu_cla_flags_tb_isim_beh.wdb
ISim P.20131013 ( signature 0x7708f090 )
WARNING: A WEBPACK license was found.
WARNING: Please use Xilinx License Configuration Manager to check out a full ISim
license.
WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for
more information on the differences between the Lite and the Full version.
This is a Lite version of ISim.
Time resolution is 1 ps
Simulator is doing circuit initialization process.
Finished circuit initialization process.
```

```
-- *****
-- **** STUDENT: 64190088
-- *****
-- KOMENTARJI K OCENI NALOGE
-- Matej Možek: Ni pripomb
-- *****
```

```
64190088>rem ***** test cla adder
```

```
64190088>if not exist "xst" mkdir xst
```

```
64190088>cd XST
```

```
64190088\xst>if not exist "projnav.tmp" mkdir "projnav.tmp"
```

```
64190088\xst>cd ..
```

```
64190088>rem ***** test cla operations
```

```
64190088>xst -ifn cla_add_n_bit.xst
Release 14.7 - xst P.20131013 ( nt64 )
Copyright ( c ) 1995-2013 Xilinx, Inc. All rights reserved.
-- > Parameter TMPDIR set to xst/projnav.tmp
```

```
Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.24 secs
```

```
-- > Parameter xsthdpdir set to xst
```

```
Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.24 secs
```

```
-- >
```

```
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- 8.4.5) Cross Clock Domains Report

```
=====
* Synthesis Options Summary *
```

```
=====
-- -- Source Parameters
```

```
Input File Name : "cla_add_n_bit.prj"
```

Ignore Synthesis Constraint File : NO

-- -- Target Parameters

Output File Name : "cla_add_n_bit"

Output Format : NGC

Target Device : xc6slx4-3-tqg144

-- -- Source Options

Top Module Name : cla_add_n_bit

Automatic FSM Extraction : YES

FSM Encoding Algorithm : Auto

Safe Implementation : No

FSM Style : LUT

RAM Extraction : Yes

RAM Style : Auto

ROM Extraction : Yes

Shift Register Extraction : YES

ROM Style : Auto

Resource Sharing : YES

Asynchronous To Synchronous : NO

Shift Register Minimum Size : 2

Use DSP Block : Auto

Automatic Register Balancing : No

-- -- Target Options

LUT Combining : Auto

Reduce Control Sets : Auto

Add IO Buffers : YES

Global Maximum Fanout : 100000

Add Generic Clock Buffer(BUFG) : 16

Register Duplication : YES

Optimize Instantiated Primitives : NO

Use Clock Enable : Auto

Use Synchronous Set : Auto

Use Synchronous Reset : Auto

Pack IO Registers into IOBs : Auto

Equivalent register Removal : YES

-- -- General Options

Optimization Goal : Speed

Optimization Effort : 1

Power Reduction : NO

Keep Hierarchy : No

Netlist Hierarchy : As_Optimized

RTL Output : Yes

Global Optimization : AllClockNets

Read Cores : YES

Write Timing Constraints : NO

Cross Clock Analysis : NO

Hierarchy Separator : /

Bus Delimiter : <>

Case Specifier : Maintain

Slice Utilization Ratio : 100

BRAM Utilization Ratio : 100

DSP48 Utilization Ratio : 100

Auto BRAM Packing : NO

Slice Utilization Ratio Delta : 5

=====

```

=====
* HDL Parsing *
=====
Parsing VHDL file "64190088\cla_gp.vhd" into library work
Parsing entity <cla_gp>.
Parsing architecture <ideal> of entity <cla_gp>.
Parsing VHDL file "64190088\cla_add_n_bit.vhd" into library work
Parsing entity <cla_add_n_bit>.
Parsing architecture <NDV> of entity <cla_add_n_bit>.

=====
* HDL Elaboration *
=====

Elaborating entity <cla_add_n_bit> ( architecture <NDV> ) with generics from
library <work>.

=====
* HDL Synthesis *
=====

Synthesizing Unit <cla_add_n_bit>.
Related source file is "64190088\cla_add_n_bit.vhd".
  n = 8
  Summary:
Unit <cla_add_n_bit> synthesized.

=====
HDL Synthesis Report

Macro Statistics
# Xors : 16
  1-bit xor2 : 16

=====

=====
* Advanced HDL Synthesis *
=====

=====
Advanced HDL Synthesis Report

Macro Statistics
# Xors : 16
  1-bit xor2 : 16

=====

=====
* Low Level Synthesis *
=====

Optimizing unit <cla_add_n_bit> ...

Mapping all equations...
Building and optimizing final netlist ...

```

Found area constraint ratio of 100 (+ 5) on block cla_add_n_bit, actual ratio is 1.

Final Macro Processing ...

=====
Final Register Report

Found no macro

=====
* Partition Report *
=====

Partition Implementation Status

-- -- -- -- -- -- -- -- -- -- -- -- -- --
-- -- -

No Partitions were found in this design.

-- -- -- -- -- -- -- -- -- -- -- -- -- --
-- -- -

=====
* Design Summary *
=====

Top Level Output File Name : cla_add_n_bit.ngc

Primitive and Black Box Usage:

-- -- -- -- -- -- -- -- -- -- -- -- -- --
-- --

BELS : 24
LUT2 : 6
LUT3 : 3
LUT5 : 6
LUT6 : 9
IO Buffers : 28
IBUF : 17
OBUF : 11

Device utilization summary:

-- -- -- -- -- -- -- -- -- -- -- -- -- --
-

Selected Device : 6slx4tqg144-3

Slice Logic Utilization:

Number of Slice LUTs: 24 out of 2400 1%
Number used as Logic: 24 out of 2400 1%

Slice Logic Distribution:

Number of LUT Flip Flop pairs used: 24
Number with an unused Flip Flop: 24 out of 24 100%
Number with an unused LUT: 0 out of 24 0%
Number of fully used LUT-FF pairs: 0 out of 24 0%
Number of unique control sets: 0

IO Utilization:

Number of IOs: 28

Number of bonded IOBs: 28 out of 102 27%

Specific Feature Utilization:

```
-- -- -- -- -- -- -- -- -- -- -- -- -- --  
-
```

Partition Resource Summary:

```
-- -- -- -- -- -- -- -- -- -- -- -- -- --  
-
```

No Partitions were found in this design.

```
-- -- -- -- -- -- -- -- -- -- -- -- -- --  
-
```

=====
Timing Report

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.

FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT
GENERATED AFTER PLACE-and-ROUTE.

Clock Information:

```
-- -- -- -- -- -- -- -- -- -- -- -- -- --  
No clock signals found in this design
```

Asynchronous Control Signals Information:

```
-- -- -- -- -- -- -- -- -- -- -- -- -- --  
-- -- -- -- -- -- -- -- -- -- -- -- -- --
```

No asynchronous control signals found in this design

Timing Summary:

```
-- -- -- -- -- -- -- -- -- -- -- -- -- --
```

Speed Grade: -3

Minimum period: No path found

Minimum input arrival time before clock: No path found

Maximum output required time after clock: No path found

Maximum combinational path delay: 9.101ns

Timing Details:

```
-- -- -- -- -- -- -- -- -- -- -- -- -- --
```

All values displayed in nanoseconds (ns)

=====
Timing constraint: Default path analysis

Total number of paths / destination ports: 131 / 11

```
-- -- -- -- -- -- -- -- -- -- -- -- -- --  
-- -- -- -- -- -- -- -- -- -- -- -- -- --  
-- -- -- -- -- -- -- -- -- -- -- -- -- --
```

Delay: 9.101ns (Levels of Logic = 7)

Source: Y<0> (PAD)

Destination: S<7> (PAD)

Data Path: Y<0> to S<7>

Gate Net

Cell:in->out fanout Delay Delay Logical Name (Net Name)


```

--      --      --      --      --      --      --      --      --      --      --
--      --      --      --      --      --      --      --      --      --      --
--      --
IBUF:I->0 6 1.222 0.973 Y_0_IBUF ( Y_0_IBUF )
LUT3:I0->0 2 0.205 0.617 C<3>_SW0 ( N2 )
LUT5:I4->0 3 0.205 0.651 C<3> ( C<3> )
LUT3:I2->0 2 0.205 0.617 C<6>_SW0 ( N4 )
LUT5:I4->0 2 0.205 0.845 C<6> ( C<6> )
LUT5:I2->0 1 0.205 0.579 Mxor_S_sig<7>_xo<0>1 ( S_7_OBUF )
OBUF:I->0 2.571 S_7_OBUF ( S<7> )
--      --      --      --      --      --      --      --      --      --      --
--      --      --      --      --      --      --      --      --      --      --
Total 9.101ns ( 4.818ns logic, 4.283ns route )
( 52.9% logic, 47.1% route )

```

Cross Clock Domains Report:

```

Total REAL time to Xst completion: 7.00 secs
Total CPU time to Xst completion: 7.92 secs

```

```
-- >
```

Total memory usage is 4487500 kilobytes

Number of errors : 0 (0 filtered)

Number of warnings : 0 (0 filtered)

Number of infos : 0 (0 filtered)

```

64190088>fuse -incremental -o cla_add_n_bit_tb_isim_beh.exe -prj
cla_add_n_bit_tb.prj -top cla_add_n_bit_tb
Running: \unwrapped\fuse.exe -incremental -o cla_add_n_bit_tb_isim_beh.exe -prj
cla_add_n_bit_tb.prj -top cla_add_n_bit_tb
ISim P.20131013 ( signature 0x7708f090 )
Number of CPUs detected in this system: 8
Turning on mult-threading, number of parallel sub-compilation jobs: 16
Determining compilation order of HDL files
Parsing VHDL file "cla_gp.vhd" into library work
Parsing VHDL file "cla_add_n_bit.vhd" into library work
Parsing VHDL file "cla_add_n_bit_tb_IDEAL.vhd" into library work
Starting static elaboration
Completed static elaboration
Compiling package standard
Compiling package std_logic_1164
Compiling package textio
Compiling package std_logic_textio
Compiling package numeric_std
Compiling package attributes
Compiling package std_logic_misc
Compiling architecture ndv of entity cla_add_n_bit [\cla_add_n_bit( 8 )\]
Compiling architecture testbench_arch of entity cla_add_n_bit_tb
Time Resolution for simulation is 1ps.
Waiting for 1 sub-compilation( s ) to finish...
Compiled 10 VHDL Units
Built simulation executable cla_add_n_bit_tb_isim_beh.exe

```

Fuse Memory Usage: 37380 KB
Fuse CPU Usage: 905 ms

```
64190088>cla_add_n_bit_tb_isim_beh.exe -tclbatch isim.tcl -wdb
cla_add_n_bit_tb_isim_beh.wdb
ISim P.20131013 ( signature 0x7708f090 )
WARNING: A WEBPACK license was found.
WARNING: Please use Xilinx License Configuration Manager to check out a full ISim
license.
WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for
more information on the differences between the Lite and the Full version.
This is a Lite version of ISim.
Time resolution is 1 ps
Simulator is doing circuit initialization process.
Finished circuit initialization process.
```

```
64190088>rem ***** test cla flags
```

```
64190088>xst -ifn cla_add_n_bit_flags.xst
Release 14.7 - xst P.20131013 ( nt64 )
Copyright ( c ) 1995-2013 Xilinx, Inc. All rights reserved.
-- > Parameter TMPDIR set to xst/projnav.tmp
```

Total REAL time to Xst completion: 1.00 secs
Total CPU time to Xst completion: 0.25 secs

```
-- > Parameter xsthdpdir set to xst
```

Total REAL time to Xst completion: 1.00 secs
Total CPU time to Xst completion: 0.25 secs

```
-- > ERROR:Xst:438 - Can not open file : cla_add_n_bit_flags.prj
```

Total REAL time to Xst completion: 1.00 secs
Total CPU time to Xst completion: 0.28 secs

```
-- >
```

Total memory usage is 4422880 kilobytes

Number of errors : 1 (0 filtered)
Number of warnings : 0 (0 filtered)
Number of infos : 0 (0 filtered)

```
64190088>fuse -incremental -o cla_add_n_bit_tb_flags_isim_beh.exe -prj
cla_add_n_bit_flags_tb.prj -top cla_add_n_bit_flags_tb_IDEAL
Running: \unwrapped\fuse.exe -incremental -o cla_add_n_bit_tb_flags_isim_beh.exe -
prj cla_add_n_bit_flags_tb.prj -top cla_add_n_bit_flags_tb_IDEAL
ISim P.20131013 ( signature 0x7708f090 )
Number of CPUs detected in this system: 8
Turning on mult-threading, number of parallel sub-compilation jobs: 16
Determining compilation order of HDL files
Parsing VHDL file "cla_gp.vhd" into library work
Parsing VHDL file "cla_add_n_bit.vhd" into library work
Parsing VHDL file "cla_add_n_bit_flags_tb_IDEAL.vhd" into library work
Starting static elaboration
Completed static elaboration
Compiling package standard
Compiling package std_logic_1164
```

```

Compiling package textio
Compiling package std_logic_textio
Compiling package numeric_std
Compiling package attributes
Compiling package std_logic_misc
Compiling architecture ndv of entity cla_add_n_bit [\cla_add_n_bit( 8 )\]
Compiling architecture a1 of entity cla_add_n_bit_flags_tb_ideal
Time Resolution for simulation is 1ps.
Waiting for 1 sub-compilation( s ) to finish...
Compiled 10 VHDL Units
Built simulation executable cla_add_n_bit_tb_flags_isim_beh.exe
Fuse Memory Usage: 37524 KB
Fuse CPU Usage: 968 ms

64190088>cla_add_n_bit_tb_flags_isim_beh.exe -tclbatch isim.tcl -wdb
cla_add_n_bit_flags_tb.wdb
ISim P.20131013 ( signature 0x7708f090 )
WARNING: A WEBPACK license was found.
WARNING: Please use Xilinx License Configuration Manager to check out a full ISim
license.
WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for
more information on the differences between the Lite and the Full version.
This is a Lite version of ISim.
Time resolution is 1 ps
Simulator is doing circuit initialization process.
Finished circuit initialization process.

64190088>rem ***** test alu operations

64190088>xst -ifn alu_cla.xst
Release 14.7 - xst P.20131013 ( nt64 )
Copyright ( c ) 1995-2013 Xilinx, Inc. All rights reserved.
-- > Parameter TMPDIR set to xst/projnav.tmp

Total REAL time to Xst completion: 1.00 secs
Total CPU time to Xst completion: 0.24 secs

-- > Parameter xsthdmdir set to xst

Total REAL time to Xst completion: 1.00 secs
Total CPU time to Xst completion: 0.24 secs

-- >
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```

- 8.4.2) Asynchronous Control Signals Information
- 8.4.3) Timing Summary
- 8.4.4) Timing Details
- 8.4.5) Cross Clock Domains [Report](#)

```
=====
* Synthesis Options Summary *
=====
--      -- Source Parameters
Input File Name : "alu_cla.prj"
Ignore Synthesis Constraint File : NO

--      -- Target Parameters
Output File Name : "alu_cla"
Output Format : NGC
Target Device : xc6slx4-3-tqg144

--      -- Source Options
Top Module Name : alu_cla
Automatic FSM Extraction : YES
FSM Encoding Algorithm : Auto
Safe Implementation : No
FSM Style : LUT
RAM Extraction : Yes
RAM Style : Auto
ROM Extraction : Yes
Shift Register Extraction : YES
ROM Style : Auto
Resource Sharing : YES
Asynchronous To Synchronous : NO
Shift Register Minimum Size : 2
Use DSP Block : Auto
Automatic Register Balancing : No

--      -- Target Options
LUT Combining : Auto
Reduce Control Sets : Auto
Add IO Buffers : YES
Global Maximum Fanout : 100000
Add Generic Clock Buffer( BUFG ) : 16
Register Duplication : YES
Optimize Instantiated Primitives : NO
Use Clock Enable : Auto
Use Synchronous Set : Auto
Use Synchronous Reset : Auto
Pack IO Registers into IOBs : Auto
Equivalent register Removal : YES

--      -- General Options
Optimization Goal : Speed
Optimization Effort : 1
Power Reduction : NO
Keep Hierarchy : No
Netlist Hierarchy : As_Optimized
RTL Output : Yes
Global Optimization : AllClockNets
Read Cores : YES
Write Timing Constraints : NO
Cross Clock Analysis : NO
```

Hierarchy Separator : /
Bus Delimiter : <>
Case Specifier : Maintain
Slice Utilization Ratio : 100
BRAM Utilization Ratio : 100
DSP48 Utilization Ratio : 100
Auto BRAM Packing : NO
Slice Utilization Ratio Delta : 5

=====

=====

* HDL Parsing *

=====

Parsing VHDL file "64190088\cla_gp.vhd" into library work
Parsing entity <cla_gp>.
Parsing architecture <ideal> of entity <cla_gp>.
Parsing VHDL file "64190088\cla_add_n_bit.vhd" into library work
Parsing entity <cla_add_n_bit>.
Parsing architecture <NDV> of entity <cla_add_n_bit>.
Parsing VHDL file "64190088\alu_cla.vhd" into library work
Parsing entity <alu_cla>.
Parsing architecture <NDV> of entity <alu_cla>.

=====

* HDL Elaboration *

=====

Elaborating entity <alu_cla> (architecture <NDV>) with generics from library <work>.

Elaborating entity <cla_add_n_bit> (architecture <NDV>) with generics from library <work>.

=====

* HDL Synthesis *

=====

Synthesizing Unit <alu_cla>.
Related source file is "64190088\alu_cla.vhd".
n = 8
Found 8-bit 12-to-1 multiplexer for signal <S> created at line 58.
Summary:
inferred 7 Multiplexer(s).
Unit <alu_cla> synthesized.

Synthesizing Unit <cla_add_n_bit>.
Related source file is "64190088\cla_add_n_bit.vhd".
n = 8
Summary:
Unit <cla_add_n_bit> synthesized.

=====

HDL Synthesis Report

Macro Statistics

Multiplexers : 7
8-bit 12-to-1 multiplexer : 1
8-bit 2-to-1 multiplexer : 6

```
# Xors : 17
1-bit xor2 : 16
8-bit xor2 : 1
```

=====

=====

```
* Advanced HDL Synthesis *
```

=====

=====

Advanced HDL Synthesis Report

Macro Statistics

```
# Multiplexers : 7
8-bit 12-to-1 multiplexer : 1
8-bit 2-to-1 multiplexer : 6
# Xors : 17
1-bit xor2 : 16
8-bit xor2 : 1
```

=====

=====

```
* Low Level Synthesis *
```

=====

Optimizing unit <alu_cla> ...

Optimizing unit <cla_add_n_bit> ...

Mapping all equations...

Building and optimizing final netlist ...

Found area constraint ratio of 100 (+ 5) on block alu_cla, actual ratio is 3.

Final Macro Processing ...

=====

Final Register Report

Found no macro

=====

=====

```
* Partition Report *
```

=====

Partition Implementation Status

```
--      --      --      --      --      --      --      --      --      --      --      --
--      --      --      --      --      --      --      --      --      --      --      --
```

No Partitions were found in this design.

```
--      --      --      --      --      --      --      --      --      --      --      --
--      --      --      --      --      --      --      --      --      --      --      --
```

=====

```
* Design Summary *
```

=====

Primitive and Black Box Usage:

— — — — —

— — — — —

```
# BELS : 52
# LUT3 : 2
# LUT5 : 14
# LUT6 : 35
# MUXF7 : 1
# IO Buffers : 34
# IBUF : 20
# OBUF : 14
```

Device utilization summary:

— — — — —

Selected Device : 6s1x4tqg144-3

Slice Logic Utilization:

Number of Slice LUTs: 51 out of 2400 2%
Number used as Logic: 51 out of 2400 2%

Slice Logic Distribution:

```

Number of LUT Flip Flop pairs used: 51
Number with an unused Flip Flop: 51 out of 51 100%
Number with an unused LUT: 0 out of 51 0%
Number of fully used LUT-FF pairs: 0 out of 51 0%
Number of unique control sets: 0

```

IO Utilization:

Number of IOs: 34
Number of bonded IOBs: 34 out of 102 33%

Specific Feature Utilization:

Partition Resource Summary:

No Partitions were found in this design.

.....

.....

Timing Report

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.
FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT
GENERATED AFTER PLACE-and-ROUTE.

Clock Information:

[illegible]

Asynchronous Control Signals Information:

```
-- -- -- -- -- -- -- -- -- -- -- -- -- --
-- -- -- -- -- -- -- -- -- -- -- -- -- --
```

No asynchronous control signals found in this design

Timing Summary:

```
-- -- -- -- -- -- -- -- -- -- -- -- -- --
```

Speed Grade: -3

Minimum period: No path found

Minimum input arrival time before clock: No path found

Maximum output required time after clock: No path found

Maximum combinational path delay: 11.074ns

Timing Details:

```
-- -- -- -- -- -- -- -- -- -- -- -- -- --
```

All values displayed in nanoseconds (ns)

=====
Timing constraint: Default path analysis

Total number of paths / destination ports: 1119 / 14

```
-- -- -- -- -- -- -- -- -- -- -- -- -- --
-- -- -- -- -- -- -- -- -- -- -- -- -- --
-- -- -- -- -- -- -- -- -- -- -- -- -- --
```

Delay: 11.074ns (Levels of Logic = 8)

Source: F<2> (PAD)

Destination: S<7> (PAD)

Data Path: F<2> to S<7>

Gate Net

Cell:in->out fanout Delay Delay Logical Name (Net Name)

```
-- -- -- -- -- -- -- -- -- -- -- -- -- --
-- -- -- -- -- -- -- -- -- -- -- -- -- --
-- -- -- -- -- -- -- -- -- -- -- -- -- --
```

IBUF:I->0 32 1.222 1.636 F_2_IBUF (F_2_IBUF)

LUT6:I1->0 6 0.203 0.973 Mmux_Y_sig31 (Y_sig<1>)

LUT5:I2->0 4 0.205 1.028 U1/C<3>2 (U1/C<3>)

LUT6:I1->0 1 0.203 0.000 U1/C<6>_G (N14)

MUXF7:I1->0 4 0.140 0.912 U1/C<6> (U1/C<6>)

LUT5:I2->0 3 0.205 0.995 U1/Mxor_S_sig<7>_xo<0>1 (Negative_OBUF)

LUT6:I1->0 1 0.203 0.579 Zero (Zero_OBUF)

OBUF:I->0 2.571 Zero_OBUF (Zero)

```
-- -- -- -- -- -- -- -- -- -- -- -- -- --
-- -- -- -- -- -- -- -- -- -- -- -- -- --
```

Total 11.074ns (4.952ns logic, 6.122ns route)

(44.7% logic, 55.3% route)

=====
Cross Clock Domains Report:

```
-- -- -- -- -- -- -- -- -- -- -- -- -- --
```

=====
Total REAL time to Xst completion: 9.00 secs

Total CPU time to Xst completion: 8.72 secs

-- >

Total memory usage is 4487500 kilobytes

Number of errors : 0 (0 filtered)

Number of warnings : 0 (0 filtered)

Number of infos : 0 (0 filtered)

```
64190088>fuse -incremental -o alu_cla_tb_isim_beh.exe -prj alu_cla_tb.prj -top
alu_cla_tb
```

```
Running: \unwrapped\fuse.exe -incremental -o alu_cla_tb_isim_beh.exe -prj
alu_cla_tb.prj -top alu_cla_tb
```

```
ISim P.20131013 ( signature 0x7708f090 )
```

```
Number of CPUs detected in this system: 8
```

```
Turning on mult-threading, number of parallel sub-compilation jobs: 16
```

```
Determining compilation order of HDL files
```

```
Parsing VHDL file "cla_gp.vhd" into library work
```

```
Parsing VHDL file "cla_add_n_bit.vhd" into library work
```

```
Parsing VHDL file "alu_cla.vhd" into library work
```

```
Parsing VHDL file "alu_cla_tb_IDEAL.vhd" into library work
```

```
Starting static elaboration
```

```
Completed static elaboration
```

```
Compiling package standard
```

```
Compiling package std_logic_1164
```

```
Compiling package textio
```

```
Compiling package std_logic_textio
```

```
Compiling package numeric_std
```

```
Compiling package attributes
```

```
Compiling package std_logic_misc
```

```
Compiling architecture ndv of entity cla_add_n_bit [\cla_add_n_bit( 8 )\]
```

```
Compiling architecture ndv of entity alu_cla [\alu_cla( 8 )\]
```

```
Compiling architecture testbench_arch of entity alu_cla_tb
```

```
Time Resolution for simulation is 1ps.
```

```
Waiting for 1 sub-compilation( s ) to finish...
```

```
Compiled 12 VHDL Units
```

```
Built simulation executable alu_cla_tb_isim_beh.exe
```

```
Fuse Memory Usage: 37744 KB
```

```
Fuse CPU Usage: 983 ms
```

```
64190088>alu_cla_tb_isim_beh.exe -tclbatch isim.tcl -wdb alu_cla_tb_isim_beh.wdb
```

```
ISim P.20131013 ( signature 0x7708f090 )
```

```
WARNING: A WEBPACK license was found.
```

```
WARNING: Please use Xilinx License Configuration Manager to check out a full ISim
license.
```

```
WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for
more information on the differences between the Lite and the Full version.
```

```
This is a Lite version of ISim.
```

```
Time resolution is 1 ps
```

```
Simulator is doing circuit initialization process.
```

```
Finished circuit initialization process.
```

```
at 7864320 ns, Instance /alu_cla_tb/ : Warning: NUMERIC_STD.TO_UNSIGNED: vector
truncated
```

```
at 8847360 ns, Instance /alu_cla_tb/ : Warning: NUMERIC_STD.TO_UNSIGNED: vector
truncated
```

```
at 9830400 ns, Instance /alu_cla_tb/ : Warning: NUMERIC_STD.TO_UNSIGNED: vector
truncated
```

```
at 10813440 ns, Instance /alu_cla_tb/ : Warning: NUMERIC_STD.TO_UNSIGNED: vector
truncated
```

```
at 11796480 ns, Instance /alu_cla_tb/ : Warning: NUMERIC_STD.TO_UNSIGNED: vector
truncated
```

at 12779520 ns, Instance /alu_cla_tb/ : Warning: NUMERIC_STD.TO_UNSIGNED: vector truncated
at 13762560 ns, Instance /alu_cla_tb/ : Warning: NUMERIC_STD.TO_UNSIGNED: vector truncated
at 14745600 ns, Instance /alu_cla_tb/ : Warning: NUMERIC_STD.TO_UNSIGNED: vector truncated

64190088>rem ***** test alu flags

64190088>xst -ifn alu_cla_flags.xst
Release 14.7 - xst P.20131013 (nt64)
Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.
-- > Parameter TMPDIR set to xst/projnav.tmp

Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.24 secs

-- > Parameter xsthdpdir set to xst

Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.24 secs

-- >

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=====
* Synthesis Options Summary *

-- -- Source Parameters

Input File Name : "alu_cla_flags_tb.prj"
Ignore Synthesis Constraint File : NO

-- -- Target Parameters

Output File Name : "alu_cla_flags_tb"
Output Format : NGC
Target Device : xc6slx4-3-tqg144

-- -- Source Options

Top Module Name : alu_cla_flags_tb
Automatic FSM Extraction : YES

FSM Encoding Algorithm : Auto
Safe Implementation : No
FSM Style : LUT
RAM Extraction : Yes
RAM Style : Auto
ROM Extraction : Yes
Shift Register Extraction : YES
ROM Style : Auto
Resource Sharing : YES
Asynchronous To Synchronous : NO
Shift Register Minimum Size : 2
Use DSP Block : Auto
Automatic Register Balancing : No

-- -- Target Options

LUT Combining : Auto
Reduce Control Sets : Auto
Add IO Buffers : YES
Global Maximum Fanout : 100000
Add Generic Clock Buffer(BUFG) : 16
Register Duplication : YES
Optimize Instantiated Primitives : NO
Use Clock Enable : Auto
Use Synchronous Set : Auto
Use Synchronous Reset : Auto
Pack IO Registers into IOBs : Auto
Equivalent register Removal : YES

-- -- General Options

Optimization Goal : Speed
Optimization Effort : 1
Power Reduction : NO
Keep Hierarchy : No
Netlist Hierarchy : As_Optimized
RTL Output : Yes
Global Optimization : AllClockNets
Read Cores : YES
Write Timing Constraints : NO
Cross Clock Analysis : NO
Hierarchy Separator : /
Bus Delimiter : <>
Case Specifier : Maintain
Slice Utilization Ratio : 100
BRAM Utilization Ratio : 100
DSP48 Utilization Ratio : 100
Auto BRAM Packing : NO
Slice Utilization Ratio Delta : 5

=====

=====

* HDL Parsing *

=====

Parsing VHDL file "64190088\cla_gp.vhd" into library work
Parsing entity <cla_gp>.
Parsing architecture <ideal> of entity <cla_gp>.
Parsing VHDL file "64190088\cla_add_n_bit.vhd" into library work
Parsing entity <cla_add_n_bit>.
Parsing architecture <NDV> of entity <cla_add_n_bit>.

```

Parsing VHDL file "64190088\alu_cla.vhd" into library work
Parsing entity <alu_cla>.
Parsing architecture <NDV> of entity <alu_cla>.
Parsing VHDL file "64190088\alu_cla_tb_FLAGS_IDEAL.vhd" into library work
Parsing entity <alu_cla_flags_tb>.
Parsing architecture <test_alu_flags> of entity <alu_cla_flags_tb>.

=====
* HDL Elaboration *
=====

Elaborating entity <alu_cla_flags_tb> ( architecture <test_alu_flags> ) with
generics from library <work>.

Elaborating entity <alu_cla> ( architecture <NDV> ) with generics from library
<work>.

Elaborating entity <cla_add_n_bit> ( architecture <NDV> ) with generics from
library <work>.
ERROR:HDLCompiler:890 - "64190088\alu_cla_tb_FLAGS_IDEAL.vhd" Line 144: wait
statement without UNTIL clause not supported for synthesis
Netlist alu_cla_flags_tb( 8 )( test_alu_flags ) remains a blackbox, due to errors
in its contents
-- >

Total memory usage is 4466680 kilobytes

Number of errors : 1 ( 0 filtered )
Number of warnings : 0 ( 0 filtered )
Number of infos : 0 ( 0 filtered )

64190088>fuse -incremental -o alu_cla_flags_tb_isim_beh.exe -prj
alu_cla_flags_tb.prj -top alu_cla_flags_tb
Running: \unwrapped\fuse.exe -incremental -o alu_cla_flags_tb_isim_beh.exe -prj
alu_cla_flags_tb.prj -top alu_cla_flags_tb
ISim P.20131013 ( signature 0x7708f090 )
Number of CPUs detected in this system: 8
Turning on mult-threading, number of parallel sub-compilation jobs: 16
Determining compilation order of HDL files
Parsing VHDL file "cla_gp.vhd" into library work
Parsing VHDL file "cla_add_n_bit.vhd" into library work
Parsing VHDL file "alu_cla.vhd" into library work
Parsing VHDL file "alu_cla_tb_FLAGS_IDEAL.vhd" into library work
Starting static elaboration
Completed static elaboration
Compiling package standard
Compiling package std_logic_1164
Compiling package textio
Compiling package std_logic_textio
Compiling package numeric_std
Compiling package attributes
Compiling package std_logic_misc
Compiling architecture ndv of entity cla_add_n_bit [\cla_add_n_bit( 8 )\]
Compiling architecture ndv of entity alu_cla [\alu_cla( 8 )\]
Compiling architecture test_alu_flags of entity alu_cla_flags_tb
Time Resolution for simulation is 1ps.
Waiting for 1 sub-compilation( s ) to finish...
Compiled 12 VHDL Units
Built simulation executable alu_cla_flags_tb_isim_beh.exe

```

Fuse Memory Usage: 37640 KB
Fuse CPU Usage: 999 ms

```
64190088>alu_cla_flags_tb_isim_beh.exe -tclbatch isim.tcl -wdb
alu_cla_flags_tb_isim_beh.wdb
ISim P.20131013 ( signature 0x7708f090 )
WARNING: A WEBPACK license was found.
WARNING: Please use Xilinx License Configuration Manager to check out a full ISim
license.
WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for
more information on the differences between the Lite and the Full version.
This is a Lite version of ISim.
Time resolution is 1 ps
Simulator is doing circuit initialization process.
Finished circuit initialization process.
```

```
-- *****
-- **** STUDENT: 64200100
-- *****
-- KOMENTARJI K OCENI NALOGE
-- Matej Možek: Ni pripomb
-- *****
```

```
64200100>rem ***** test cla adder
```

```
64200100>if not exist "xst" mkdir xst
```

```
64200100>cd XST
```

```
64200100\xst>if not exist "projnav.tmp" mkdir "projnav.tmp"
```

```
64200100\xst>cd ..
```

```
64200100>rem ***** test cla operations
```

```
64200100>xst -ifn cla_add_n_bit.xst
Release 14.7 - xst P.20131013 ( nt64 )
Copyright ( c ) 1995-2013 Xilinx, Inc. All rights reserved.
-- > Parameter TMPDIR set to xst/projnav.tmp
```

```
Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.24 secs
```

```
-- > Parameter xsthdpdir set to xst
```

```
Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.24 secs
```

```
-- >
```

```
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```
=====
* Synthesis Options Summary *
```

```
-- -- Source Parameters
```

```
Input File Name : "cla_add_n_bit.prj"
```

Ignore Synthesis Constraint File : NO

-- -- Target Parameters

Output File Name : "cla_add_n_bit"

Output Format : NGC

Target Device : xc6slx4-3-tqg144

-- -- Source Options

Top Module Name : cla_add_n_bit

Automatic FSM Extraction : YES

FSM Encoding Algorithm : Auto

Safe Implementation : No

FSM Style : LUT

RAM Extraction : Yes

RAM Style : Auto

ROM Extraction : Yes

Shift Register Extraction : YES

ROM Style : Auto

Resource Sharing : YES

Asynchronous To Synchronous : NO

Shift Register Minimum Size : 2

Use DSP Block : Auto

Automatic Register Balancing : No

-- -- Target Options

LUT Combining : Auto

Reduce Control Sets : Auto

Add IO Buffers : YES

Global Maximum Fanout : 100000

Add Generic Clock Buffer(BUFG) : 16

Register Duplication : YES

Optimize Instantiated Primitives : NO

Use Clock Enable : Auto

Use Synchronous Set : Auto

Use Synchronous Reset : Auto

Pack IO Registers into IOBs : Auto

Equivalent register Removal : YES

-- -- General Options

Optimization Goal : Speed

Optimization Effort : 1

Power Reduction : NO

Keep Hierarchy : No

Netlist Hierarchy : As_Optimized

RTL Output : Yes

Global Optimization : AllClockNets

Read Cores : YES

Write Timing Constraints : NO

Cross Clock Analysis : NO

Hierarchy Separator : /

Bus Delimiter : <>

Case Specifier : Maintain

Slice Utilization Ratio : 100

BRAM Utilization Ratio : 100

DSP48 Utilization Ratio : 100

Auto BRAM Packing : NO

Slice Utilization Ratio Delta : 5

=====

```

=====
* HDL Parsing *
=====
Parsing VHDL file "64200100\cla_gp.vhd" into library work
Parsing entity <cla_gp>.
Parsing architecture <ideal> of entity <cla_gp>.
Parsing VHDL file "64200100\cla_add_n_bit.vhd" into library work
Parsing entity <cla_add_n_bit>.
Parsing architecture <NDV> of entity <cla_add_n_bit>.

=====
* HDL Elaboration *
=====

Elaborating entity <cla_add_n_bit> ( architecture <NDV> ) with generics from
library <work>.
WARNING:HDLCompiler:634 - "64200100\cla_add_n_bit.vhd" Line 23: Net <Gint[0]> does
not have a driver.

=====
* HDL Synthesis *
=====

Synthesizing Unit <cla_add_n_bit>.
  Related source file is "64200100\cla_add_n_bit.vhd".
  n = 8
WARNING:Xst:653 - Signal      <Gint<0>> is used but never assigned. This
sourceless signal          will be automatically connected to value GND.
  Summary:
Unit <cla_add_n_bit> synthesized.

=====
HDL Synthesis Report

Macro Statistics
# Xors : 16
  1-bit xor2 : 16

=====

=====
* Advanced HDL Synthesis *
=====

=====
Advanced HDL Synthesis Report

Macro Statistics
# Xors : 16
  1-bit xor2 : 16

=====

=====
* Low Level Synthesis *
=====

Optimizing unit <cla_add_n_bit> ...

```


Mapping all equations...
Building and optimizing final netlist ...
Found area constraint ratio of 100 (+ 5) on block cla_add_n_bit, actual ratio is 1.

Final Macro Processing ...

=====

Final Register Report

Found no macro

=====

=====

* Partition Report *

=====

Partition Implementation Status

```
--      --      --      --      --      --      --      --      --      --      --      --
--      --      --      --      --      --      --      --      --      --      --      --
```

No Partitions were found in this design.

```
--      --      --      --      --      --      --      --      --      --      --      --
--      --      --      --      --      --      --      --      --      --      --      --
```

=====

* Design Summary *

=====

Top Level Output File Name : cla_add_n_bit.ngc

Primitive and Black Box Usage:

```
--      --      --      --      --      --      --      --      --      --      --      --
--      --      --      --      --      --      --      --      --      --      --      --
```

BELS : 24
LUT2 : 6
LUT3 : 3
LUT5 : 6
LUT6 : 9
IO Buffers : 28
IBUF : 17
OBUF : 11

Device utilization summary:

```
--      --      --      --      --      --      --      --      --      --      --      --
--
```

Selected Device : 6slx4tqg144-3

Slice Logic Utilization:

Number of Slice LUTs: 24 out of 2400 1%
Number used as Logic: 24 out of 2400 1%

Slice Logic Distribution:

Number of LUT Flip Flop pairs used: 24
Number with an unused Flip Flop: 24 out of 24 100%
Number with an unused LUT: 0 out of 24 0%

Number of fully used LUT-FF pairs: 0 out of 24 0%
Number of unique control sets: 0

IO Utilization:

Number of IOs: 28
Number of bonded IOBs: 28 out of 102 27%

Specific Feature Utilization:

```
-- -- -- -- -- -- -- -- -- -- -- -- -- --  
-  
Partition Resource Summary:  
-- -- -- -- -- -- -- -- -- -- -- -- -- --  
-
```

No Partitions were found in this design.

```
-- -- -- -- -- -- -- -- -- -- -- -- -- --  
-
```

=====
Timing Report

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.
FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT
GENERATED AFTER PLACE-and-ROUTE.

Clock Information:

```
-- -- -- -- -- -- -- -- -- -- -- -- -- --  
No clock signals found in this design
```

Asynchronous Control Signals Information:

```
-- -- -- -- -- -- -- -- -- -- -- -- -- --  
-- -- -- -- -- -- -- -- -- -- -- -- -- --  
No asynchronous control signals found in this design
```

Timing Summary:

```
-- -- -- -- -- -- -- -- -- -- -- -- -- --  
Speed Grade: -3
```

Minimum period: No path found
Minimum input arrival time before clock: No path found
Maximum output required time after clock: No path found
Maximum combinational path delay: 9.101ns

Timing Details:

```
-- -- -- -- -- -- -- -- -- -- -- -- -- --  
All values displayed in nanoseconds ( ns )
```

=====
Timing constraint: Default path analysis

Total number of paths / destination ports: 131 / 11

```
-- -- -- -- -- -- -- -- -- -- -- -- -- --  
-- -- -- -- -- -- -- -- -- -- -- -- -- --  
-- -- -- -- -- -- -- -- -- -- -- -- -- --
```

Delay: 9.101ns (Levels of Logic = 7)

Source: Y<0> (PAD)

Destination: S<7> (PAD)

Data Path: Y<0> to S<7>

Gate Net

Cell:in->out fanout Delay Delay Logical Name (Net Name)

```
--      --      --      --      --      --      --      --      --      --      --
--      --      --      --      --      --      --      --      --      --      --
--      --
IBUF:I->0 6 1.222 0.973 Y_0_IBUF ( Y_0_IBUF )
LUT3:I0->0 2 0.205 0.617 C<3>_SW0 ( N2 )
LUT5:I4->0 3 0.205 0.651 C<3> ( C<3> )
LUT3:I2->0 2 0.205 0.617 C<6>_SW0 ( N4 )
LUT5:I4->0 2 0.205 0.845 C<6> ( C<6> )
LUT5:I2->0 1 0.205 0.579 Mxor_S_sig<7>_xo<0>1 ( S_7_OBUF )
OBUF:I->0 2.571 S_7_OBUF ( S<7> )
--      --      --      --      --      --      --      --      --      --      --
--      --      --      --      --      --      --      --      --      --      --
Total 9.101ns ( 4.818ns logic, 4.283ns route )
( 52.9% logic, 47.1% route )
```

=====

Cross Clock Domains Report:

```
--      --      --      --      --      --      --      --      --      --      --
--      --      --      --      --      --      --      --      --      --      --
=====
```

Total REAL time to Xst completion: 8.00 secs

Total CPU time to Xst completion: 8.13 secs

-- >

Total memory usage is 4487500 kilobytes

Number of errors : 0 (0 filtered)

Number of warnings : 2 (0 filtered)

Number of infos : 0 (0 filtered)

```
64200100>fuse -incremental -o cla_add_n_bit_tb_isim_beh.exe -prj
cla_add_n_bit_tb.prj -top cla_add_n_bit_tb
Running: \unwrapped\fuse.exe -incremental -o cla_add_n_bit_tb_isim_beh.exe -prj
cla_add_n_bit_tb.prj -top cla_add_n_bit_tb
ISim P.20131013 ( signature 0x7708f090 )
Number of CPUs detected in this system: 8
Turning on mult-threading, number of parallel sub-compilation jobs: 16
Determining compilation order of HDL files
Parsing VHDL file "cla_gp.vhd" into library work
Parsing VHDL file "cla_add_n_bit.vhd" into library work
Parsing VHDL file "cla_add_n_bit_tb_IDEAL.vhd" into library work
Starting static elaboration
Completed static elaboration
Compiling package standard
Compiling package std_logic_1164
Compiling package textio
Compiling package std_logic_textio
Compiling package numeric_std
Compiling package attributes
Compiling package std_logic_misc
Compiling architecture ndv of entity cla_add_n_bit [\cla_add_n_bit( 8 )\]
Compiling architecture testbench_arch of entity cla_add_n_bit_tb
Time Resolution for simulation is 1ps.
```

Waiting for 1 sub-compilation(s) to finish...

Compiled 10 VHDL Units

Built simulation executable cla_add_n_bit_tb_isim_beh.exe

Fuse Memory Usage: 37440 KB

Fuse CPU Usage: 858 ms

64200100>cla_add_n_bit_tb_isim_beh.exe -tclbatch isim.tcl -wdb

cla_add_n_bit_tb_isim_beh.wdb

ISim P.20131013 (signature 0x7708f090)

WARNING: A WEBPACK license was found.

WARNING: Please use Xilinx License Configuration Manager to check out a full ISim license.

WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for more information on the differences between the Lite and the Full version.

This is a Lite version of ISim.

Time resolution is 1 ps

Simulator is doing circuit initialization process.

Finished circuit initialization process.

64200100>rem ***** test cla flags

64200100>xst -ifn cla_add_n_bit_flags.xst

Release 14.7 - xst P.20131013 (nt64)

Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.

-- > Parameter TMPDIR set to xst/projnav.tmp

Total REAL time to Xst completion: 0.00 secs

Total CPU time to Xst completion: 0.22 secs

-- > Parameter xsthdmdir set to xst

Total REAL time to Xst completion: 0.00 secs

Total CPU time to Xst completion: 0.22 secs

-- > ERROR:Xst:438 - Can not open file : cla_add_n_bit_flags.prj

Total REAL time to Xst completion: 0.00 secs

Total CPU time to Xst completion: 0.25 secs

-- >

Total memory usage is 4422880 kilobytes

Number of errors : 1 (0 filtered)

Number of warnings : 0 (0 filtered)

Number of infos : 0 (0 filtered)

64200100>fuse -incremental -o cla_add_n_bit_tb_flags_isim_beh.exe -prj

cla_add_n_bit_flags_tb.prj -top cla_add_n_bit_flags_tb_IDEAL

Running: \unwrapped\fuse.exe -incremental -o cla_add_n_bit_tb_flags_isim_beh.exe -prj cla_add_n_bit_flags_tb.prj -top cla_add_n_bit_flags_tb_IDEAL

ISim P.20131013 (signature 0x7708f090)

Number of CPUs detected in this system: 8

Turning on mult-threading, number of parallel sub-compilation jobs: 16

Determining compilation order of HDL files

Parsing VHDL file "cla_gp.vhd" into library work

Parsing VHDL file "cla_add_n_bit.vhd" into library work

Parsing VHDL file "cla_add_n_bit_flags_tb_IDEAL.vhd" into library work

Starting static elaboration

```

Completed static elaboration
Compiling package standard
Compiling package std_logic_1164
Compiling package textio
Compiling package std_logic_textio
Compiling package numeric_std
Compiling package attributes
Compiling package std_logic_misc
Compiling architecture ndv of entity cla_add_n_bit [\cla_add_n_bit( 8 )\]
Compiling architecture a1 of entity cla_add_n_bit_flags_tb_ideal
Time Resolution for simulation is 1ps.
Waiting for 1 sub-compilation( s ) to finish...
Compiled 10 VHDL Units
Built simulation executable cla_add_n_bit_tb_flags_isim_beh.exe
Fuse Memory Usage: 37316 KB
Fuse CPU Usage: 889 ms

64200100>cla_add_n_bit_tb_flags_isim_beh.exe -tclbatch isim.tcl -wdb
cla_add_n_bit_flags_tb.wdb
ISim P.20131013 ( signature 0x7708f090 )
WARNING: A WEBPACK license was found.
WARNING: Please use Xilinx License Configuration Manager to check out a full ISim
license.
WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for
more information on the differences between the Lite and the Full version.
This is a Lite version of ISim.
Time resolution is 1 ps
Simulator is doing circuit initialization process.
Finished circuit initialization process.

64200100>rem ***** test alu operations

64200100>xst -ifn alu_cla.xst
Release 14.7 - xst P.20131013 ( nt64 )
Copyright ( c ) 1995-2013 Xilinx, Inc. All rights reserved.
-- > Parameter TMPDIR set to xst/projnav.tmp

Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.23 secs

-- > Parameter xsthdpdir set to xst

Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.23 secs

-- >
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```

8.3) Partition Resource Summary
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8.4.4) Timing Details
8.4.5) Cross Clock Domains Report

=====
* Synthesis Options Summary *
=====

-- -- Source Parameters

Input File Name : "alu_cla.prj"
Ignore Synthesis Constraint File : NO

-- -- Target Parameters

Output File Name : "alu_cla"
Output Format : NGC
Target Device : xc6slx4-3-tqg144

-- -- Source Options

Top Module Name : alu_cla
Automatic FSM Extraction : YES
FSM Encoding Algorithm : Auto
Safe Implementation : No
FSM Style : LUT
RAM Extraction : Yes
RAM Style : Auto
ROM Extraction : Yes
Shift Register Extraction : YES
ROM Style : Auto
Resource Sharing : YES
Asynchronous To Synchronous : NO
Shift Register Minimum Size : 2
Use DSP Block : Auto
Automatic Register Balancing : No

-- -- Target Options

LUT Combining : Auto
Reduce Control Sets : Auto
Add IO Buffers : YES
Global Maximum Fanout : 100000
Add Generic Clock Buffer(BUFG) : 16
Register Duplication : YES
Optimize Instantiated Primitives : NO
Use Clock Enable : Auto
Use Synchronous Set : Auto
Use Synchronous Reset : Auto
Pack IO Registers into IOBs : Auto
Equivalent register Removal : YES

-- -- General Options

Optimization Goal : Speed
Optimization Effort : 1
Power Reduction : NO
Keep Hierarchy : No
Netlist Hierarchy : As_Optimized
RTL Output : Yes
Global Optimization : AllClockNets

Read Cores : YES
Write Timing Constraints : NO
Cross Clock Analysis : NO
Hierarchy Separator : /
Bus Delimiter : <>
Case Specifier : Maintain
Slice Utilization Ratio : 100
BRAM Utilization Ratio : 100
DSP48 Utilization Ratio : 100
Auto BRAM Packing : NO
Slice Utilization Ratio Delta : 5

=====

=====

* HDL Parsing *

=====

Parsing VHDL file "64200100\cla_gp.vhd" into library work
Parsing entity <cla_gp>.
Parsing architecture <ideal> of entity <cla_gp>.
Parsing VHDL file "64200100\cla_add_n_bit.vhd" into library work
Parsing entity <cla_add_n_bit>.
Parsing architecture <NDV> of entity <cla_add_n_bit>.
Parsing VHDL file "64200100\alu_cla.vhd" into library work
Parsing entity <alu_cla>.
Parsing architecture <NDV> of entity <alu_cla>.

=====

* HDL Elaboration *

=====

Elaborating entity <alu_cla> (architecture <NDV>) with generics from library <work>.

Elaborating entity <cla_add_n_bit> (architecture <NDV>) with generics from library <work>.

WARNING:HDLCompiler:634 - "64200100\cla_add_n_bit.vhd" Line 23: Net <Gint[0]> does not have a driver.

=====

* HDL Synthesis *

=====

Synthesizing Unit <alu_cla>.

Related source file is "64200100\alu_cla.vhd".

n = 8

Found 8-bit 12-to-1 multiplexer for signal <S> created at line 50.

Summary:

inferred 19 Multiplexer(s).

Unit <alu_cla> synthesized.

Synthesizing Unit <cla_add_n_bit>.

Related source file is "64200100\cla_add_n_bit.vhd".

n = 8

WARNING:Xst:653 - Signal <Gint<0>> is used but never assigned. This sourceless signal will be automatically connected to value GND.

Summary:

Unit <cla_add_n_bit> synthesized.

```
=====
HDL Synthesis Report

Macro Statistics
# Multiplexers : 19
  1-bit 2-to-1 multiplexer : 12
  8-bit 12-to-1 multiplexer : 1
  8-bit 2-to-1 multiplexer : 6
# Xors : 17
  1-bit xor2 : 16
  8-bit xor2 : 1

=====
* Advanced HDL Synthesis *
=====

Advanced HDL Synthesis Report

Macro Statistics
# Multiplexers : 19
  1-bit 2-to-1 multiplexer : 12
  8-bit 12-to-1 multiplexer : 1
  8-bit 2-to-1 multiplexer : 6
# Xors : 17
  1-bit xor2 : 16
  8-bit xor2 : 1

=====
* Low Level Synthesis *
=====

Optimizing unit <alu_cla> ...
Optimizing unit <cla_add_n_bit> ...

Mapping all equations...
Building and optimizing final netlist ...
Found area constraint ratio of 100 ( + 5 ) on block alu_cla, actual ratio is 3.

Final Macro Processing ...

=====
Final Register Report

Found no macro

=====
* Partition Report *
=====

Partition Implementation Status
```


No Partitions were found in this design.

```
--      --      --      --      --      --      --      --      --      --      --      --
--      --      --
```

```
=====
* Design Summary *
=====
```

Top Level Output File Name : alu_cla.ngc

Primitive and Black Box Usage:

```
--      --      --      --      --      --      --      --      --      --      --      --
--      --      --
```

```
# BELS : 60
# LUT3 : 4
# LUT5 : 14
# LUT6 : 41
# MUXF7 : 1
# IO Buffers : 34
# IBUF : 20
# OBUF : 14
```

Device utilization summary:

```
--      --      --      --      --      --      --      --      --      --      --      --
-
```

Selected Device : 6slx4tqg144-3

Slice Logic Utilization:

Number of Slice LUTs: 59 out of 2400 2%
Number used as Logic: 59 out of 2400 2%

Slice Logic Distribution:

Number of LUT Flip Flop pairs used: 59
Number with an unused Flip Flop: 59 out of 59 100%
Number with an unused LUT: 0 out of 59 0%
Number of fully used LUT-FF pairs: 0 out of 59 0%
Number of unique control sets: 0

IO Utilization:

Number of IOs: 34
Number of bonded IOBs: 34 out of 102 33%

Specific Feature Utilization:

```
--      --      --      --      --      --      --      --      --      --      --      --
-
```

Partition Resource Summary:

```
--      --      --      --      --      --      --      --      --      --      --      --
-
```

No Partitions were found in this design.

```
--      --      --      --      --      --      --      --      --      --      --      --
-
```

```
=====
```

Timing Report

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.

FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT
GENERATED AFTER PLACE-and-ROUTE.

Clock Information:

-- -- -- -- --
No clock signals found in this design

Asynchronous Control Signals Information:

-- -- -- -- --
No asynchronous control signals found in this design

Timing Summary:

-- -- -- -- --
Speed Grade: -3

Minimum period: No path found

Minimum input arrival time before clock: No path found

Maximum output required time after clock: No path found

Maximum combinational path delay: 11.168ns

Timing Details:

-- -- -- -- --
All values displayed in nanoseconds (ns)

=====
Timing constraint: Default path analysis

Total number of paths / destination ports: 1146 / 14

-- -- -- -- --
-- -- -- -- --
-- -- -- -- --

Delay: 11.168ns (Levels of Logic = 8)

Source: F<2> (PAD)

Destination: Negative (PAD)

Data Path: F<2> to Negative

Gate Net

Cell: in->out fanout Delay Delay Logical Name (Net Name)

-- -- -- -- --
-- -- -- -- --
-- -- -- -- --

IBUF:I->0 35 1.222 1.679 F_2_IBUF (F_2_IBUF)

LUT6:I1->0 6 0.203 0.973 Mmux_Y_sig31 (Y_sig<1>)

LUT5:I2->0 4 0.205 1.028 U1/C<3>2 (U1/C<3>)

LUT6:I1->0 1 0.203 0.000 U1/C<6>_G (N16)

MUXF7:I1->0 5 0.140 0.943 U1/C<6> (U1/C<6>)

LUT5:I2->0 3 0.205 1.015 U1/Mxor_S_sig<7>_xo<0>1 (S_sig<7>)

LUT6:I0->0 1 0.203 0.579 Mmux_Negative1 (Negative_OBUF)

OBUF:I->0 2.571 Negative_OBUF (Negative)

-- -- -- -- --
-- -- -- -- --

Total 11.168ns (4.952ns logic, 6.216ns route)

(44.3% logic, 55.7% route)

=====

Cross Clock Domains Report:

-- -- -- -- -- -- -- -- -- -- -- -- -- --
=====

Total REAL time to Xst completion: 9.00 secs

Total CPU time to Xst completion: 8.92 secs

-- >

Total memory usage is 4487500 kilobytes

Number of errors : 0 (0 filtered)

Number of warnings : 2 (0 filtered)

Number of infos : 0 (0 filtered)

64200100>fuse -incremental -o alu_cla_tb_isim_beh.exe -prj alu_cla_tb.prj -top alu_cla_tb

Running: \unwrapped\fuse.exe -incremental -o alu_cla_tb_isim_beh.exe -prj alu_cla_tb.prj -top alu_cla_tb

ISim P.20131013 (signature 0x7708f090)

Number of CPUs detected in this system: 8

Turning on mult-threading, number of parallel sub-compilation jobs: 16

Determining compilation order of HDL files

Parsing VHDL file "cla_gp.vhd" into library work

Parsing VHDL file "cla_add_n_bit.vhd" into library work

Parsing VHDL file "alu_cla.vhd" into library work

Parsing VHDL file "alu_cla_tb_IDEAL.vhd" into library work

Starting static elaboration

Completed static elaboration

Compiling package standard

Compiling package std_logic_1164

Compiling package textio

Compiling package std_logic_textio

Compiling package numeric_std

Compiling package attributes

Compiling package std_logic_misc

Compiling architecture ndv of entity cla_add_n_bit [\cla_add_n_bit(8)\]

Compiling architecture ndv of entity alu_cla [\alu_cla(8)\]

Compiling architecture testbench_arch of entity alu_cla_tb

Time Resolution for simulation is 1ps.

Waiting for 1 sub-compilation(s) to finish...

Compiled 12 VHDL Units

Built simulation executable alu_cla_tb_isim_beh.exe

Fuse Memory Usage: 37680 KB

Fuse CPU Usage: 984 ms

64200100>alu_cla_tb_isim_beh.exe -tclbatch isim.tcl -wdb alu_cla_tb_isim_beh.wdb

ISim P.20131013 (signature 0x7708f090)

WARNING: A WEBPACK license was found.

WARNING: Please use Xilinx License Configuration Manager to check out a full ISim license.

WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for more information on the differences between the Lite and the Full version.

This is a Lite version of ISim.

Time resolution is 1 ps

Simulator is doing circuit initialization process.

Finished circuit initialization process.

at 7864320 ns, Instance /alu_cla_tb/ : Warning: NUMERIC_STD.TO_UNSIGNED: vector truncated
at 8847360 ns, Instance /alu_cla_tb/ : Warning: NUMERIC_STD.TO_UNSIGNED: vector truncated
at 9830400 ns, Instance /alu_cla_tb/ : Warning: NUMERIC_STD.TO_UNSIGNED: vector truncated
at 10813440 ns, Instance /alu_cla_tb/ : Warning: NUMERIC_STD.TO_UNSIGNED: vector truncated
at 11796480 ns, Instance /alu_cla_tb/ : Warning: NUMERIC_STD.TO_UNSIGNED: vector truncated
at 12779520 ns, Instance /alu_cla_tb/ : Warning: NUMERIC_STD.TO_UNSIGNED: vector truncated
at 13762560 ns, Instance /alu_cla_tb/ : Warning: NUMERIC_STD.TO_UNSIGNED: vector truncated
at 14745600 ns, Instance /alu_cla_tb/ : Warning: NUMERIC_STD.TO_UNSIGNED: vector truncated

64200100>rem ***** test alu flags

64200100>xst -ifn alu_cla_flags.xst
Release 14.7 - xst P.20131013 (nt64)
Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.
-- > Parameter TMPDIR set to xst/projnav.tmp

Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.25 secs

-- > Parameter xsthdpdir set to xst

Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.25 secs

-- >

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 - 8.4.5) Cross Clock Domains Report

=====

* Synthesis Options Summary *

=====

-- -- Source Parameters

Input File Name : "alu_cla_flags_tb.prj"

Ignore Synthesis Constraint File : NO

-- -- Target Parameters

Output File Name : "alu_cla_flags_tb"

Output Format : NGC

Target Device : xc6slx4-3-tqg144

-- -- Source Options

Top Module Name : alu_cla_flags_tb

Automatic FSM Extraction : YES

FSM Encoding Algorithm : Auto

Safe Implementation : No

FSM Style : LUT

RAM Extraction : Yes

RAM Style : Auto

ROM Extraction : Yes

Shift Register Extraction : YES

ROM Style : Auto

Resource Sharing : YES

Asynchronous To Synchronous : NO

Shift Register Minimum Size : 2

Use DSP Block : Auto

Automatic Register Balancing : No

-- -- Target Options

LUT Combining : Auto

Reduce Control Sets : Auto

Add IO Buffers : YES

Global Maximum Fanout : 100000

Add Generic Clock Buffer(BUFG) : 16

Register Duplication : YES

Optimize Instantiated Primitives : NO

Use Clock Enable : Auto

Use Synchronous Set : Auto

Use Synchronous Reset : Auto

Pack IO Registers into IOBs : Auto

Equivalent register Removal : YES

-- -- General Options

Optimization Goal : Speed

Optimization Effort : 1

Power Reduction : NO

Keep Hierarchy : No

Netlist Hierarchy : As_Optimized

RTL Output : Yes

Global Optimization : AllClockNets

Read Cores : YES

Write Timing Constraints : NO

Cross Clock Analysis : NO

Hierarchy Separator : /

Bus Delimiter : <>

Case Specifier : Maintain

Slice Utilization Ratio : 100

BRAM Utilization Ratio : 100

DSP48 Utilization Ratio : 100

Auto BRAM Packing : NO

Slice Utilization Ratio Delta : 5

=====

```

=====
* HDL Parsing *
=====
Parsing VHDL file "64200100\cla_gp.vhd" into library work
Parsing entity <cla_gp>.
Parsing architecture <ideal> of entity <cla_gp>.
Parsing VHDL file "64200100\cla_add_n_bit.vhd" into library work
Parsing entity <cla_add_n_bit>.
Parsing architecture <NDV> of entity <cla_add_n_bit>.
Parsing VHDL file "64200100\alu_cla.vhd" into library work
Parsing entity <alu_cla>.
Parsing architecture <NDV> of entity <alu_cla>.
Parsing VHDL file "64200100\alu_cla_tb_FLAGS_IDEAL.vhd" into library work
Parsing entity <alu_cla_flags_tb>.
Parsing architecture <test_alu_flags> of entity <alu_cla_flags_tb>.

=====
* HDL Elaboration *
=====

Elaborating entity <alu_cla_flags_tb> ( architecture <test_alu_flags> ) with
generics from library <work>.

Elaborating entity <alu_cla> ( architecture <NDV> ) with generics from library
<work>.

Elaborating entity <cla_add_n_bit> ( architecture <NDV> ) with generics from
library <work>.
WARNING:HDLCompiler:634 - "64200100\cla_add_n_bit.vhd" Line 23: Net <Gint[0]> does
not have a driver.
ERROR:HDLCompiler:890 - "64200100\alu_cla_tb_FLAGS_IDEAL.vhd" Line 144: wait
statement without UNTIL clause not supported for synthesis
Netlist alu_cla_flags_tb( 8 )( test_alu_flags ) remains a blackbox, due to errors
in its contents
-- >

Total memory usage is 4466680 kilobytes

Number of errors : 1 ( 0 filtered )
Number of warnings : 1 ( 0 filtered )
Number of infos : 0 ( 0 filtered )

64200100>fuse -incremental -o alu_cla_flags_tb_isim_beh.exe -prj
alu_cla_flags_tb.prj -top alu_cla_flags_tb
Running: \unwrapped\fuse.exe -incremental -o alu_cla_flags_tb_isim_beh.exe -prj
alu_cla_flags_tb.prj -top alu_cla_flags_tb
ISim P.20131013 ( signature 0x7708f090 )
Number of CPUs detected in this system: 8
Turning on mult-threading, number of parallel sub-compilation jobs: 16
Determining compilation order of HDL files
Parsing VHDL file "cla_gp.vhd" into library work
Parsing VHDL file "cla_add_n_bit.vhd" into library work
Parsing VHDL file "alu_cla.vhd" into library work
Parsing VHDL file "alu_cla_tb_FLAGS_IDEAL.vhd" into library work
Starting static elaboration
Completed static elaboration
Compiling package standard
Compiling package std_logic_1164

```

```
Compiling package textio
Compiling package std_logic_textio
Compiling package numeric_std
Compiling package attributes
Compiling package std_logic_misc
Compiling architecture ndv of entity cla_add_n_bit [\cla_add_n_bit( 8 )\]
Compiling architecture ndv of entity alu_cla [\alu_cla( 8 )\]
Compiling architecture test_alu_flags of entity alu_cla_flags_tb
Time Resolution for simulation is 1ps.
Waiting for 1 sub-compilation( s ) to finish...
Compiled 12 VHDL Units
Built simulation executable alu_cla_flags_tb_isim_beh.exe
Fuse Memory Usage: 37648 KB
Fuse CPU Usage: 983 ms

64200100>alu_cla_flags_tb_isim_beh.exe -tclbatch isim.tcl -wdb
alu_cla_flags_tb_isim_beh.wdb
ISim P.20131013 ( signature 0x7708f090 )
WARNING: A WEBPACK license was found.
WARNING: Please use Xilinx License Configuration Manager to check out a full ISim
license.
WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for
more information on the differences between the Lite and the Full version.
This is a Lite version of ISim.
Time resolution is 1 ps
Simulator is doing circuit initialization process.
Finished circuit initialization process.
```

```
-- *****
-- **** STUDENT: 64200112
-- *****
-- KOMENTARJI K OCENI NALOGE
-- Matej Možek: Ni pripomb
-- *****
```

```
64200112>rem ***** test cla adder
```

```
64200112>if not exist "xst" mkdir xst
```

```
64200112>cd XST
```

```
64200112\xst>if not exist "projnav.tmp" mkdir "projnav.tmp"
```

```
64200112\xst>cd ..
```

```
64200112>rem ***** test cla operations
```

```
64200112>xst -ifn cla_add_n_bit.xst
Release 14.7 - xst P.20131013 ( nt64 )
Copyright ( c ) 1995-2013 Xilinx, Inc. All rights reserved.
-- > Parameter TMPDIR set to xst/projnav.tmp
```

```
Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.23 secs
```

```
-- > Parameter xsthdpdir set to xst
```

```
Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.23 secs
```

```
-- >
```

```
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```
=====
* Synthesis Options Summary *
```

```
=====
-- -- Source Parameters
```

```
Input File Name : "cla_add_n_bit.prj"
```


Ignore Synthesis Constraint File : NO

-- -- Target Parameters

Output File Name : "cla_add_n_bit"

Output Format : NGC

Target Device : xc6slx4-3-tqg144

-- -- Source Options

Top Module Name : cla_add_n_bit

Automatic FSM Extraction : YES

FSM Encoding Algorithm : Auto

Safe Implementation : No

FSM Style : LUT

RAM Extraction : Yes

RAM Style : Auto

ROM Extraction : Yes

Shift Register Extraction : YES

ROM Style : Auto

Resource Sharing : YES

Asynchronous To Synchronous : NO

Shift Register Minimum Size : 2

Use DSP Block : Auto

Automatic Register Balancing : No

-- -- Target Options

LUT Combining : Auto

Reduce Control Sets : Auto

Add IO Buffers : YES

Global Maximum Fanout : 100000

Add Generic Clock Buffer(BUFG) : 16

Register Duplication : YES

Optimize Instantiated Primitives : NO

Use Clock Enable : Auto

Use Synchronous Set : Auto

Use Synchronous Reset : Auto

Pack IO Registers into IOBs : Auto

Equivalent register Removal : YES

-- -- General Options

Optimization Goal : Speed

Optimization Effort : 1

Power Reduction : NO

Keep Hierarchy : No

Netlist Hierarchy : As_Optimized

RTL Output : Yes

Global Optimization : AllClockNets

Read Cores : YES

Write Timing Constraints : NO

Cross Clock Analysis : NO

Hierarchy Separator : /

Bus Delimiter : <>

Case Specifier : Maintain

Slice Utilization Ratio : 100

BRAM Utilization Ratio : 100

DSP48 Utilization Ratio : 100

Auto BRAM Packing : NO

Slice Utilization Ratio Delta : 5

=====

```

=====
* HDL Parsing *
=====
Parsing VHDL file "64200112\cla_gp.vhd" into library work
Parsing entity <cla_gp>.
Parsing architecture <ideal> of entity <cla_gp>.
Parsing VHDL file "64200112\cla_add_n_bit.vhd" into library work
Parsing entity <cla_add_n_bit>.
Parsing architecture <NDV> of entity <cla_add_n_bit>.

=====
* HDL Elaboration *
=====

Elaborating entity <cla_add_n_bit> ( architecture <NDV> ) with generics from
library <work>.

Elaborating entity <cla_gp> ( architecture <ideal> ) from library <work>.

=====
* HDL Synthesis *
=====

Synthesizing Unit <cla_add_n_bit>.
  Related source file is "64200112\cla_add_n_bit.vhd".
  n = 8
  Summary:
    no macro.
Unit <cla_add_n_bit> synthesized.

Synthesizing Unit <cla_gp>.
  Related source file is "64200112\cla_gp.vhd".
  Summary:
Unit <cla_gp> synthesized.

=====
HDL Synthesis Report

Macro Statistics
# Xors : 16
  1-bit xor2 : 16

=====

=====
* Advanced HDL Synthesis *
=====

=====
Advanced HDL Synthesis Report

Macro Statistics
# Xors : 16
  1-bit xor2 : 16

=====
=====

```

* Low Level Synthesis *

=====

Optimizing unit <cla_add_n_bit> ...

Mapping all equations...

Building and optimizing final netlist ...

Found area constraint ratio of 100 (+ 5) on block cla_add_n_bit, actual ratio is 1.

Final Macro Processing ...

=====

Final Register Report

Found no macro

=====

=====

* Partition Report *

=====

Partition Implementation Status

-- -- -- -- -- -- -- -- -- -- -- -- -- --
-- -- --

No Partitions were found in this design.

-- -- -- -- -- -- -- -- -- -- -- -- -- --
-- -- --

=====

* Design Summary *

=====

Top Level Output File Name : cla_add_n_bit.ngc

Primitive and Black Box Usage:

-- -- -- -- -- -- -- -- -- -- -- -- -- --
-- -- --

BELS : 24
LUT2 : 6
LUT3 : 3
LUT5 : 6
LUT6 : 9
IO Buffers : 28
IBUF : 17
OBUF : 11

Device utilization summary:

-- -- -- -- -- -- -- -- -- -- -- -- -- --
-

Selected Device : 6slx4tqg144-3

Slice Logic Utilization:

Number of Slice LUTs: 24 out of 2400 1%
Number used as Logic: 24 out of 2400 1%

```
Number of LUT Flip Flop pairs used: 24
Number with an unused Flip Flop: 24 out of 24 100%
Number with an unused LUT: 0 out of 24 0%
Number of fully used LUT-FF pairs: 0 out of 24 0%
Number of unique control sets: 0
```

Number of IOs: 28
Number of bonded IOBs: 28 out of 102 27%

[illegible][illegible]

1. 2. 3. 4. 5. 6. 7. 8. 9. 10. 11. 12. 13. 14. 15. 16. 17. 18. 19. 20. 21. 22. 23. 24. 25. 26. 27. 28. 29. 30. 31. 32. 33. 34. 35. 36. 37. 38. 39. 40. 41. 42. 43. 44. 45. 46. 47. 48. 49. 50. 51. 52. 53. 54. 55. 56. 57. 58. 59. 60. 61. 62. 63. 64. 65. 66. 67. 68. 69. 70. 71. 72. 73. 74. 75. 76. 77. 78. 79. 80. 81. 82. 83. 84. 85. 86. 87. 88. 89. 90. 91. 92. 93. 94. 95. 96. 97. 98. 99. 100. 101. 102. 103. 104. 105. 106. 107. 108. 109. 110. 111. 112. 113. 114. 115. 116. 117. 118. 119. 120. 121. 122. 123. 124. 125. 126. 127. 128. 129. 130. 131. 132. 133. 134. 135. 136. 137. 138. 139. 140. 141. 142. 143. 144. 145. 146. 147. 148. 149. 150. 151. 152. 153. 154. 155. 156. 157. 158. 159. 160. 161. 162. 163. 164. 165. 166. 167. 168. 169. 170. 171. 172. 173. 174. 175. 176. 177. 178. 179. 180. 181. 182. 183. 184. 185. 186. 187. 188. 189. 190. 191. 192. 193. 194. 195. 196. 197. 198. 199. 200. 201. 202. 203. 204. 205. 206. 207. 208. 209. 210. 211. 212. 213. 214. 215. 216. 217. 218. 219. 220. 221. 222. 223. 224. 225. 226. 227. 228. 229. 230. 231. 232. 233. 234. 235. 236. 237. 238. 239. 240. 241. 242. 243. 244. 245. 246. 247. 248. 249. 250. 251. 252. 253. 254. 255. 256. 257. 258. 259. 260. 261. 262. 263. 264. 265. 266. 267. 268. 269. 270. 271. 272. 273. 274. 275. 276. 277. 278. 279. 280. 281. 282. 283. 284. 285. 286. 287. 288. 289. 290. 291. 292. 293. 294. 295. 296. 297. 298. 299. 300. 301. 302. 303. 304. 305. 306. 307. 308. 309. 310. 311. 312. 313. 314. 315. 316. 317. 318. 319. 320. 321. 322. 323. 324. 325. 326. 327. 328. 329. 330. 331. 332. 333. 334. 335. 336. 337. 338. 339. 340. 341. 342. 343. 344. 345. 346. 347. 348. 349. 350. 351. 352. 353. 354. 355. 356. 357. 358. 359. 360. 361. 362. 363. 364. 365. 366. 367. 368. 369. 370. 371. 372. 373. 374. 375. 376. 377. 378. 379. 380. 381. 382. 383. 384. 385. 386. 387. 388. 389. 390. 391. 392. 393. 394. 395. 396. 397. 398. 399. 400. 401. 402. 403. 404. 405. 406. 407. 408. 409. 410. 411. 412. 413. 414. 415. 416. 417. 418. 419. 420. 421. 422. 423. 424. 425. 426. 427. 428. 429. 430. 431. 432. 433. 434. 435. 436. 437. 438. 439. 440. 441. 442. 443. 444. 445. 446. 447. 448. 449. 450. 451. 452. 453. 454. 455. 456. 457. 458. 459. 460. 461. 462. 463. 464. 465. 466. 467. 468. 469. 470. 471. 472. 473. 474. 475. 476. 477. 478. 479. 480. 481. 482. 483. 484. 485. 486. 487. 488. 489. 490. 491. 492. 493. 494. 495. 496. 497. 498. 499. 500. 501. 502. 503. 504. 505. 506. 507. 508. 509. 510. 511. 512. 513. 514. 515. 516. 517. 518. 519. 520. 521. 522. 523. 524. 525. 526. 527. 528. 529. 530. 531. 532. 533. 534. 535. 536. 537. 538. 539. 540. 541. 542. 543. 544. 545. 546. 547. 548. 549. 550. 551. 552. 553. 554. 555. 556. 557. 558. 559. 560. 561. 562. 563. 564. 565. 566. 567. 568. 569. 570. 571. 572. 573. 574. 575. 576. 577. 578. 579. 580. 581. 582. 583. 584. 585. 586. 587. 588. 589. 590. 591. 592. 593. 594. 595. 596. 597. 598. 599. 600. 601. 602. 603. 604. 605. 606. 607. 608. 609. 610. 611. 612. 613. 614. 615. 616. 617. 618. 619. 620. 621. 622. 623. 624. 625. 626. 627. 628. 629. 630. 631. 632. 633. 634. 635. 636. 637. 638. 639. 640. 641. 642. 643. 644. 645. 646. 647. 648. 649. 650. 651. 652. 653. 654. 655. 656. 657. 658. 659. 660. 661. 662. 663. 664. 665. 666. 667. 668. 669. 670. 671. 672. 673. 674. 675. 676. 677. 678. 679. 680. 681. 682. 683. 684. 685. 686. 687. 688. 689. 690. 691. 692. 693. 694. 695. 696. 697. 698. 699. 700. 701. 702. 703. 704. 705. 706. 707. 708. 709. 710. 711. 712. 713. 714. 715. 716. 717. 718. 719. 720. 721. 722. 723. 724. 725. 726. 727. 728. 729. 730. 731. 732. 733. 734. 735. 736. 737. 738. 739. 740. 741. 742. 743. 744. 745. 746. 747. 748. 749. 750. 751. 752. 753. 754. 755. 756. 757. 758. 759. 760. 761. 762. 763. 764. 765. 766. 767. 768. 769. 770. 771. 772. 773. 774. 775. 776. 777. 778. 779. 780. 781. 782. 783. 784. 785. 786. 787. 788. 789. 790. 791. 792. 793. 794. 795. 796. 797. 798. 799. 800. 801. 802. 803. 804. 805. 806. 807. 808. 809. 810. 811. 812. 813. 814. 815. 816. 817. 818. 819. 820. 821. 822. 823. 824. 825. 826. 827. 828. 829. 830. 831. 832. 833. 834. 835. 836. 837. 838. 839. 840.

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.
FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT
GENERATED AFTER PLACE-and-ROUTE.

[illegible]

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|-----|
| 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 | 26 | 27 | 28 | 29 | 30 | 31 | 32 | 33 | 34 | 35 | 36 | 37 | 38 | 39 | 40 | 41 | 42 | 43 | 44 | 45 | 46 | 47 | 48 | 49 | 50 | 51 | 52 | 53 | 54 | 55 | 56 | 57 | 58 | 59 | 60 | 61 | 62 | 63 | 64 | 65 | 66 | 67 | 68 | 69 | 70 | 71 | 72 | 73 | 74 | 75 | 76 | 77 | 78 | 79 | 80 | 81 | 82 | 83 | 84 | 85 | 86 | 87 | 88 | 89 | 90 | 91 | 92 | 93 | 94 | 95 | 96 | 97 | 98 | 99 | 100 |
| 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 | 26 | 27 | 28 | 29 | 30 | 31 | 32 | 33 | 34 | 35 | 36 | 37 | 38 | 39 | 40 | 41 | 42 | 43 | 44 | 45 | 46 | 47 | 48 | 49 | 50 | 51 | 52 | 53 | 54 | 55 | 56 | 57 | 58 | 59 | 60 | 61 | 62 | 63 | 64 | 65 | 66 | 67 | 68 | 69 | 70 | 71 | 72 | 73 | 74 | 75 | 76 | 77 | 78 | 79 | 80 | 81 | 82 | 83 | 84 | 85 | 86 | 87 | 88 | 89 | 90 | 91 | 92 | 93 | 94 | 95 | 96 | 97 | 98 | 99 | 100 |

Speed Grade: -3

```
-- -- -- -- --
All values displayed in nanoseconds ( ns )
```

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|-----|
| 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 | 26 | 27 | 28 | 29 | 30 | 31 | 32 | 33 | 34 | 35 | 36 | 37 | 38 | 39 | 40 | 41 | 42 | 43 | 44 | 45 | 46 | 47 | 48 | 49 | 50 | 51 | 52 | 53 | 54 | 55 | 56 | 57 | 58 | 59 | 60 | 61 | 62 | 63 | 64 | 65 | 66 | 67 | 68 | 69 | 70 | 71 | 72 | 73 | 74 | 75 | 76 | 77 | 78 | 79 | 80 | 81 | 82 | 83 | 84 | 85 | 86 | 87 | 88 | 89 | 90 | 91 | 92 | 93 | 94 | 95 | 96 | 97 | 98 | 99 | 100 |
| 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 | 26 | 27 | 28 | 29 | 30 | 31 | 32 | 33 | 34 | 35 | 36 | 37 | 38 | 39 | 40 | 41 | 42 | 43 | 44 | 45 | 46 | 47 | 48 | 49 | 50 | 51 | 52 | 53 | 54 | 55 | 56 | 57 | 58 | 59 | 60 | 61 | 62 | 63 | 64 | 65 | 66 | 67 | 68 | 69 | 70 | 71 | 72 | 73 | 74 | 75 | 76 | 77 | 78 | 79 | 80 | 81 | 82 | 83 | 84 | 85 | 86 | 87 | 88 | 89 | 90 | 91 | 92 | 93 | 94 | 95 | 96 | 97 | 98 | 99 | 100 |
| 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 | 26 | 27 | 28 | 29 | 30 | 31 | 32 | 33 | 34 | 35 | 36 | 37 | 38 | 39 | 40 | 41 | 42 | 43 | 44 | 45 | 46 | 47 | 48 | 49 | 50 | 51 | 52 | 53 | 54 | 55 | 56 | 57 | 58 | 59 | 60 | 61 | 62 | 63 | 64 | 65 | 66 | 67 | 68 | 69 | 70 | 71 | 72 | 73 | 74 | 75 | 76 | 77 | 78 | 79 | 80 | 81 | 82 | 83 | 84 | 85 | 86 | 87 | 88 | 89 | 90 | 91 | 92 | 93 | 94 | 95 | 96 | 97 | 98 | 99 | 100 |

Delay: 9.101ns (Levels of Logic = 7)
Source: Y<0> (PAD)
Destination: S<7> (PAD)

Data Path: Y<0> to S<7>

Gate Net

Cell:in->out fanout Delay Delay Logical Name (Net Name)

```
-- -- -- -- -- -- -- -- -- -- -- -- -- --
-- -- -- -- -- -- -- -- -- -- -- -- -- --
-- -- -- -- -- -- -- -- -- -- -- -- -- --
```

IBUF:I->0 6 1.222 0.973 Y_0_IBUF (Y_0_IBUF)
LUT3:I0->0 2 0.205 0.617 stages[2].cla_stage/Cout_SW0 (N2)
LUT5:I4->0 3 0.205 0.651 stages[2].cla_stage/Cout (C<3>)
LUT3:I2->0 2 0.205 0.617 stages[5].cla_stage/Cout_SW0 (N4)
LUT5:I4->0 2 0.205 0.845 stages[5].cla_stage/Cout (C<6>)
LUT5:I2->0 1 0.205 0.579 stages[7].cla_stage/Mxor_S_xo<0>1 (S_7_OBUF)
OBUF:I->0 2.571 S_7_OBUF (S<7>)

```
-- -- -- -- -- -- -- -- -- -- -- -- -- --
-- -- -- -- -- -- -- -- -- -- -- -- -- --
```

Total 9.101ns (4.818ns logic, 4.283ns route)
(52.9% logic, 47.1% route)

=====
Cross Clock Domains Report:

```
-- -- -- -- -- -- -- -- -- -- -- -- -- --
```

=====
Total REAL time to Xst completion: 8.00 secs
Total CPU time to Xst completion: 8.05 secs

-- >

Total memory usage is 4487500 kilobytes

Number of errors : 0 (0 filtered)

Number of warnings : 0 (0 filtered)

Number of infos : 0 (0 filtered)

64200112>fuse -incremental -o cla_add_n_bit_tb_isim_beh.exe -prj
cla_add_n_bit_tb.prj -top cla_add_n_bit_tb
Running: \unwrapped\fuse.exe -incremental -o cla_add_n_bit_tb_isim_beh.exe -prj
cla_add_n_bit_tb.prj -top cla_add_n_bit_tb
ISim P.20131013 (signature 0x7708f090)
Number of CPUs detected in this system: 8
Turning on mult-threading, number of parallel sub-compilation jobs: 16
Determining compilation order of HDL files
Parsing VHDL file "cla_gp.vhd" into library work
Parsing VHDL file "cla_add_n_bit.vhd" into library work
Parsing VHDL file "cla_add_n_bit_tb_IDEAL.vhd" into library work
Starting static elaboration
Completed static elaboration
Compiling package standard
Compiling package std_logic_1164
Compiling package textio
Compiling package std_logic_textio
Compiling package numeric_std
Compiling package attributes

```

Compiling package std_logic_misc
Compiling architecture ideal of entity cla_gp [cla_gp_default]
Compiling architecture ndv of entity cla_add_n_bit [\cla_add_n_bit( 8 )\]
Compiling architecture testbench_arch of entity cla_add_n_bit_tb
Time Resolution for simulation is 1ps.
Waiting for 1 sub-compilation( s ) to finish...
Compiled 12 VHDL Units
Built simulation executable cla_add_n_bit_tb_isim_beh.exe
Fuse Memory Usage: 37424 KB
Fuse CPU Usage: 983 ms

64200112>cla_add_n_bit_tb_isim_beh.exe -tclbatch isim.tcl -wdb
cla_add_n_bit_tb_isim_beh.wdb
ISim P.20131013 ( signature 0x7708f090 )
WARNING: A WEBPACK license was found.
WARNING: Please use Xilinx License Configuration Manager to check out a full ISim
license.
WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for
more information on the differences between the Lite and the Full version.
This is a Lite version of ISim.
Time resolution is 1 ps
Simulator is doing circuit initialization process.
Finished circuit initialization process.

64200112>rem ***** test cla flags

64200112>xst -ifn cla_add_n_bit_flags.xst
Release 14.7 - xst P.20131013 ( nt64 )
Copyright ( c ) 1995-2013 Xilinx, Inc. All rights reserved.
-- > Parameter TMPDIR set to xst/projnav.tmp

Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.34 secs

-- > Parameter xsthdpdir set to xst

Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.36 secs

-- > ERROR:Xst:438 - Can not open file : cla_add_n_bit_flags.prj

Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.38 secs

-- >

Total memory usage is 4422880 kilobytes

Number of errors : 1 ( 0 filtered )
Number of warnings : 0 ( 0 filtered )
Number of infos : 0 ( 0 filtered )

64200112>fuse -incremental -o cla_add_n_bit_tb_flags_isim_beh.exe -prj
cla_add_n_bit_flags_tb.prj -top cla_add_n_bit_flags_tb_IDEAL
Running: \unwrapped\fuse.exe -incremental -o cla_add_n_bit_tb_flags_isim_beh.exe -
prj cla_add_n_bit_flags_tb.prj -top cla_add_n_bit_flags_tb_IDEAL
ISim P.20131013 ( signature 0x7708f090 )
Number of CPUs detected in this system: 8
Turning on mult-threading, number of parallel sub-compilation jobs: 16

```

```

Determining compilation order of HDL files
Parsing VHDL file "cla_gp.vhd" into library work
Parsing VHDL file "cla_add_n_bit.vhd" into library work
Parsing VHDL file "cla_add_n_bit_flags_tb_IDEAL.vhd" into library work
Starting static elaboration
Completed static elaboration
Compiling package standard
Compiling package std_logic_1164
Compiling package textio
Compiling package std_logic_textio
Compiling package numeric_std
Compiling package attributes
Compiling package std_logic_misc
Compiling architecture ideal of entity cla_gp [cla_gp_default]
Compiling architecture ndv of entity cla_add_n_bit [\cla_add_n_bit( 8 )\]
Compiling architecture a1 of entity cla_add_n_bit_flags_tb_ideal
Time Resolution for simulation is 1ps.
Waiting for 1 sub-compilation( s ) to finish...
Compiled 12 VHDL Units
Built simulation executable cla_add_n_bit_tb_flags_isim_beh.exe
Fuse Memory Usage: 37504 KB
Fuse CPU Usage: 874 ms

64200112>cla_add_n_bit_tb_flags_isim_beh.exe -tclbatch isim.tcl -wdb
cla_add_n_bit_flags_tb.wdb
ISim P.20131013 ( signature 0x7708f090 )
WARNING: A WEBPACK license was found.
WARNING: Please use Xilinx License Configuration Manager to check out a full ISim
license.
WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for
more information on the differences between the Lite and the Full version.
This is a Lite version of ISim.
Time resolution is 1 ps
Simulator is doing circuit initialization process.
Finished circuit initialization process.

64200112>rem ***** test alu operations

64200112>xst -ifn alu_cla.xst
Release 14.7 - xst P.20131013 ( nt64 )
Copyright ( c ) 1995-2013 Xilinx, Inc. All rights reserved.
-- > Parameter TMPDIR set to xst/projnav.tmp

Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.22 secs

-- > Parameter xsthdpdir set to xst

Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.22 secs

-- >
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3 ) HDL Elaboration
4 ) HDL Synthesis
4.1 ) HDL Synthesis Report
5 ) Advanced HDL Synthesis

```

- 5.1) Advanced HDL Synthesis Report
- 6) Low Level Synthesis
- 7) Partition Report
- 8) Design Summary
 - 8.1) Primitive and Black Box Usage
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 - 8.4.1) Clock Information
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 - 8.4.3) Timing Summary
 - 8.4.4) Timing Details
 - 8.4.5) Cross Clock Domains Report

=====

* Synthesis Options Summary *

=====

-- -- Source Parameters

Input File Name : "alu_cla.prj"
Ignore Synthesis Constraint File : NO

-- -- Target Parameters

Output File Name : "alu_cla"
Output Format : NGC
Target Device : xc6slx4-3-tqg144

-- -- Source Options

Top Module Name : alu_cla
Automatic FSM Extraction : YES
FSM Encoding Algorithm : Auto
Safe Implementation : No
FSM Style : LUT
RAM Extraction : Yes
RAM Style : Auto
ROM Extraction : Yes
Shift Register Extraction : YES
ROM Style : Auto
Resource Sharing : YES
Asynchronous To Synchronous : NO
Shift Register Minimum Size : 2
Use DSP Block : Auto
Automatic Register Balancing : No

-- -- Target Options

LUT Combining : Auto
Reduce Control Sets : Auto
Add IO Buffers : YES
Global Maximum Fanout : 100000
Add Generic Clock Buffer(BUFG) : 16
Register Duplication : YES
Optimize Instantiated Primitives : NO
Use Clock Enable : Auto
Use Synchronous Set : Auto
Use Synchronous Reset : Auto
Pack IO Registers into IOBs : Auto
Equivalent register Removal : YES

-- -- General Options

Optimization Goal : Speed

Optimization Effort : 1
Power Reduction : NO
Keep Hierarchy : No
Netlist Hierarchy : As_Optimized
RTL Output : Yes
Global Optimization : AllClockNets
Read Cores : YES
Write Timing Constraints : NO
Cross Clock Analysis : NO
Hierarchy Separator : /
Bus Delimiter : <>
Case Specifier : Maintain
Slice Utilization Ratio : 100
BRAM Utilization Ratio : 100
DSP48 Utilization Ratio : 100
Auto BRAM Packing : NO
Slice Utilization Ratio Delta : 5

=====

=====

* HDL Parsing *

=====

Parsing VHDL file "64200112\cla_gp.vhd" into library work
Parsing entity <cla_gp>.
Parsing architecture <ideal> of entity <cla_gp>.
Parsing VHDL file "64200112\cla_add_n_bit.vhd" into library work
Parsing entity <cla_add_n_bit>.
Parsing architecture <NDV> of entity <cla_add_n_bit>.
Parsing VHDL file "64200112\alu_cla.vhd" into library work
Parsing entity <alu_cla>.
Parsing architecture <NDV> of entity <alu_cla>.

=====

* HDL Elaboration *

=====

Elaborating entity <alu_cla> (architecture <NDV>) with generics from library <work>.

Elaborating entity <cla_add_n_bit> (architecture <NDV>) with generics from library <work>.

Elaborating entity <cla_gp> (architecture <ideal>) from library <work>.

=====

* HDL Synthesis *

=====

Synthesizing Unit <alu_cla>.
Related source file is "64200112\alu_cla.vhd".
n = 8
Found 8-bit 12-to-1 multiplexer for signal <S> created at line 53.
Summary:
inferred 7 Multiplexer(s).
Unit <alu_cla> synthesized.

Synthesizing Unit <cla_add_n_bit>.
Related source file is "64200112\cla_add_n_bit.vhd".

```
n = 8
Summary:
    no macro.
Unit <cla_add_n_bit> synthesized.

Synthesizing Unit <cla_gp>.
Related source file is "64200112\cla_gp.vhd".
Summary:
Unit <cla_gp> synthesized.
```

```
=====
HDL Synthesis Report
```

```
Macro Statistics
# Multiplexers : 7
  8-bit 12-to-1 multiplexer : 1
  8-bit 2-to-1 multiplexer : 6
# Xors : 17
  1-bit xor2 : 16
  8-bit xor2 : 1
```

```
=====
* Advanced HDL Synthesis *
=====
```

```
=====
Advanced HDL Synthesis Report
```

```
Macro Statistics
# Multiplexers : 7
  8-bit 12-to-1 multiplexer : 1
  8-bit 2-to-1 multiplexer : 6
# Xors : 17
  1-bit xor2 : 16
  8-bit xor2 : 1
```

```
=====
* Low Level Synthesis *
=====
```

```
Optimizing unit <alu_cla> ...
```

```
Optimizing unit <cla_add_n_bit> ...
```

```
Mapping all equations...
```

```
Building and optimizing final netlist ...
```

```
Found area constraint ratio of 100 ( + 5 ) on block alu_cla, actual ratio is 3.
```

```
Final Macro Processing ...
```

```
=====
Final Register Report
```

```
Found no macro
=====
```

```
=====
* Partition Report *
=====
```

Partition Implementation Status

```
--      --      --      --      --      --      --      --      --      --      --      --
--      --      --
```

No Partitions were found in this design.

```
--      --      --      --      --      --      --      --      --      --      --      --
--      --      --
```

```
=====
* Design Summary *
=====
```

Top Level Output File Name : alu_cla.ngc

Primitive and Black Box Usage:

```
--      --      --      --      --      --      --      --      --      --      --      --
--      --      --
```

```
# BELS : 49
# LUT3 : 3
# LUT5 : 14
# LUT6 : 30
# MUXF7 : 2
# IO Buffers : 34
# IBUF : 20
# OBUF : 14
```

Device utilization summary:

```
--      --      --      --      --      --      --      --      --      --      --      --
-
```

Selected Device : 6slx4tqg144-3

Slice Logic Utilization:

Number of Slice LUTs: 47 out of 2400 1%
Number used as Logic: 47 out of 2400 1%

Slice Logic Distribution:

Number of LUT Flip Flop pairs used: 47
Number with an unused Flip Flop: 47 out of 47 100%
Number with an unused LUT: 0 out of 47 0%
Number of fully used LUT-FF pairs: 0 out of 47 0%
Number of unique control sets: 0

IO Utilization:

Number of IOs: 34
Number of bonded IOBs: 34 out of 102 33%

Specific Feature Utilization:

```
--      --      --      --      --      --      --      --      --      --      --      --
-
```

Partition Resource Summary:

```
--      --      --      --      --      --      --      --      --      --      --      --      --
-
```

No Partitions were found in this design.

```
--      --      --      --      --      --      --      --      --      --      --      --      --
-
```

Timing Report

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.
FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT
GENERATED AFTER PLACE-and-ROUTE.

Clock Information:

```
--      --      --      --      --      --      --      --      --      --      --      --      --
-
```

No clock signals found in this design

Asynchronous Control Signals Information:

```
--      --      --      --      --      --      --      --      --      --      --      --      --
--      --      --      --      --      --      --      --      --      --      --      --      --
```

No asynchronous control signals found in this design

Timing Summary:

```
--      --      --      --      --      --      --      --      --      --      --      --      --
-
```

Speed Grade: -3

Minimum period: No path found
Minimum input arrival time before clock: No path found
Maximum output required time after clock: No path found
Maximum combinational path delay: 12.446ns

Timing Details:

```
--      --      --      --      --      --      --      --      --      --      --      --      --
-
```

All values displayed in nanoseconds (ns)

Timing constraint: Default path analysis

Total number of paths / destination ports: 918 / 14

```
--      --      --      --      --      --      --      --      --      --      --      --      --
--      --      --      --      --      --      --      --      --      --      --      --      --
--      --      --      --      --      --      --      --      --      --      --      --      --
```

Delay: 12.446ns (Levels of Logic = 9)

Source: F<2> (PAD)

Destination: Zero (PAD)

Data Path: F<2> to Zero

Gate Net

Cell: in->out fanout Delay Delay Logical Name (Net Name)

```
--      --      --      --      --      --      --      --      --      --      --      --      --
--      --      --      --      --      --      --      --      --      --      --      --      --
--      --      --      --      --      --      --      --      --      --      --      --      --
```

IBUF:I->0 30 1.222 1.608 F_2_IBUF (F_2_IBUF)
LUT6:I1->0 5 0.203 0.943 Mmux_Y_sig31 (Y_sig<1>)
LUT5:I2->0 4 0.205 0.684 U1/stages[2].cla_stage/Cout2 (U1/C<3>)
LUT3:I2->0 1 0.205 0.580 U1/stages[5].cla_stage/Cout_SW2 (N11)
LUT5:I4->0 3 0.205 0.879 U1/stages[5].cla_stage/Cout (U1/C<6>)
LUT5:I2->0 1 0.205 0.924 U1/stages[7].cla_stage/Mxor_S_xo<0>1 (S_sig<7>)

```

LUT6:I1->O 4 0.203 1.028 Mmux_S22 ( Negative_OBUF )
LUT6:I1->O 1 0.203 0.579 Zero ( Zero_OBUF )
OBUF:I->O 2.571 Zero_OBUF ( Zero )
-- -- -- -- -- -- -- -- -- -- --
-- -- -- -- -- -- -- -- -- -- --
Total 12.446ns ( 5.222ns logic, 7.224ns route )
( 42.0% logic, 58.0% route )

```

=====
Cross Clock Domains Report:

```

-- -- -- -- -- -- -- -- -- -- --
=====  

Total REAL time to Xst completion: 9.00 secs
Total CPU time to Xst completion: 9.26 secs

```

-- >

Total memory usage is 4487500 kilobytes

Number of errors : 0 (0 filtered)

Number of warnings : 0 (0 filtered)

Number of infos : 0 (0 filtered)

64200112>fuse -incremental -o alu_cla_tb_isim_beh.exe -prj alu_cla_tb.prj -top alu_cla_tb

Running: \unwrapped\fuse.exe -incremental -o alu_cla_tb_isim_beh.exe -prj alu_cla_tb.prj -top alu_cla_tb

ISim P.20131013 (signature 0x7708f090)

Number of CPUs detected in this system: 8

Turning on mult-threading, number of parallel sub-compilation jobs: 16

Determining compilation order of HDL files

Parsing VHDL file "cla_gp.vhd" into library work

Parsing VHDL file "cla_add_n_bit.vhd" into library work

Parsing VHDL file "alu_cla.vhd" into library work

Parsing VHDL file "alu_cla_tb_IDEAL.vhd" into library work

Starting static elaboration

Completed static elaboration

Compiling package standard

Compiling package std_logic_1164

Compiling package textio

Compiling package std_logic_textio

Compiling package numeric_std

Compiling package attributes

Compiling package std_logic_misc

Compiling architecture ideal of entity cla_gp [cla_gp_default]

Compiling architecture ndv of entity cla_add_n_bit [\cla_add_n_bit(8)\]

Compiling architecture ndv of entity alu_cla [\alu_cla(8)\]

Compiling architecture testbench_arch of entity alu_cla_tb

Time Resolution for simulation is 1ps.

Waiting for 1 sub-compilation(s) to finish...

Compiled 14 VHDL Units

Built simulation executable alu_cla_tb_isim_beh.exe

Fuse Memory Usage: 37664 KB

Fuse CPU Usage: 1030 ms

64200112>alu_cla_tb_isim_beh.exe -tclbatch isim.tcl -wdb alu_cla_tb_isim_beh.wdb

ISim P.20131013 (signature 0x7708f090)
WARNING: A WEBPACK license was found.
WARNING: Please use Xilinx License Configuration Manager to check out a full ISim license.

WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for more information on the differences between the Lite and the Full version.

This is a Lite version of ISim.

Time resolution is 1 ps

Simulator is doing circuit initialization process.

Finished circuit initialization process.

at 7864320 ns, Instance /alu_cla_tb/ : Warning: NUMERIC_STD.TO_UNSIGNED: vector truncated

at 8847360 ns, Instance /alu_cla_tb/ : Warning: NUMERIC_STD.TO_UNSIGNED: vector truncated

at 9830400 ns, Instance /alu_cla_tb/ : Warning: NUMERIC_STD.TO_UNSIGNED: vector truncated

at 10813440 ns, Instance /alu_cla_tb/ : Warning: NUMERIC_STD.TO_UNSIGNED: vector truncated

at 11796480 ns, Instance /alu_cla_tb/ : Warning: NUMERIC_STD.TO_UNSIGNED: vector truncated

at 12779520 ns, Instance /alu_cla_tb/ : Warning: NUMERIC_STD.TO_UNSIGNED: vector truncated

at 13762560 ns, Instance /alu_cla_tb/ : Warning: NUMERIC_STD.TO_UNSIGNED: vector truncated

at 14745600 ns, Instance /alu_cla_tb/ : Warning: NUMERIC_STD.TO_UNSIGNED: vector truncated

64200112>rem ***** test alu flags

64200112>xst -ifn alu_cla_flags.xst

Release 14.7 - xst P.20131013 (nt64)

Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.

-- > Parameter TMPDIR set to xst/projnav.tmp

Total REAL time to Xst completion: 0.00 secs

Total CPU time to Xst completion: 0.23 secs

-- > Parameter xsthdpdir set to xst

Total REAL time to Xst completion: 0.00 secs

Total CPU time to Xst completion: 0.23 secs

-- >

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- 8.4.5) Cross Clock Domains [Report](#)

```

=====
* Synthesis Options Summary *
=====
--      -- Source Parameters
Input File Name : "alu_cla_flags_tb.prj"
Ignore Synthesis Constraint File : NO

--      -- Target Parameters
Output File Name : "alu_cla_flags_tb"
Output Format : NGC
Target Device : xc6slx4-3-tqg144

--      -- Source Options
Top Module Name : alu_cla_flags_tb
Automatic FSM Extraction : YES
FSM Encoding Algorithm : Auto
Safe Implementation : No
FSM Style : LUT
RAM Extraction : Yes
RAM Style : Auto
ROM Extraction : Yes
Shift Register Extraction : YES
ROM Style : Auto
Resource Sharing : YES
Asynchronous To Synchronous : NO
Shift Register Minimum Size : 2
Use DSP Block : Auto
Automatic Register Balancing : No

--      -- Target Options
LUT Combining : Auto
Reduce Control Sets : Auto
Add IO Buffers : YES
Global Maximum Fanout : 100000
Add Generic Clock Buffer( BUFG ) : 16
Register Duplication : YES
Optimize Instantiated Primitives : NO
Use Clock Enable : Auto
Use Synchronous Set : Auto
Use Synchronous Reset : Auto
Pack IO Registers into IOBs : Auto
Equivalent register Removal : YES

--      -- General Options
Optimization Goal : Speed
Optimization Effort : 1
Power Reduction : NO
Keep Hierarchy : No
Netlist Hierarchy : As_Optimized
RTL Output : Yes
Global Optimization : AllClockNets
Read Cores : YES
Write Timing Constraints : NO
Cross Clock Analysis : NO

```

Hierarchy Separator : /
Bus Delimiter : <>
Case Specifier : Maintain
Slice Utilization Ratio : 100
BRAM Utilization Ratio : 100
DSP48 Utilization Ratio : 100
Auto BRAM Packing : NO
Slice Utilization Ratio Delta : 5

=====

=====

* HDL Parsing *

=====

Parsing VHDL file "64200112\cla_gp.vhd" into library work
Parsing entity <cla_gp>.
Parsing architecture <ideal> of entity <cla_gp>.
Parsing VHDL file "64200112\cla_add_n_bit.vhd" into library work
Parsing entity <cla_add_n_bit>.
Parsing architecture <NDV> of entity <cla_add_n_bit>.
Parsing VHDL file "64200112\alu_cla.vhd" into library work
Parsing entity <alu_cla>.
Parsing architecture <NDV> of entity <alu_cla>.
Parsing VHDL file "64200112\alu_cla_tb_FLAGS_IDEAL.vhd" into library work
Parsing entity <alu_cla_flags_tb>.
Parsing architecture <test_alu_flags> of entity <alu_cla_flags_tb>.

=====

* HDL Elaboration *

=====

Elaborating entity <alu_cla_flags_tb> (architecture <test_alu_flags>) with
generics from library <work>.

Elaborating entity <alu_cla> (architecture <NDV>) with generics from library
<work>.

Elaborating entity <cla_add_n_bit> (architecture <NDV>) with generics from
library <work>.

Elaborating entity <cla_gp> (architecture <ideal>) from library <work>.
ERROR:HDLCompiler:890 - "64200112\alu_cla_tb_FLAGS_IDEAL.vhd" Line 144: wait
statement without UNTIL clause not supported for synthesis
Netlist alu_cla_flags_tb(8)(test_alu_flags) remains a blackbox, due to errors
in its contents

-- >

Total memory usage is 4466680 kilobytes

Number of errors : 1 (0 filtered)

Number of warnings : 0 (0 filtered)

Number of infos : 0 (0 filtered)

64200112>fuse -incremental -o alu_cla_flags_tb_isim_beh.exe -prj
alu_cla_flags_tb.prj -top alu_cla_flags_tb
Running: \unwrapped\fuse.exe -incremental -o alu_cla_flags_tb_isim_beh.exe -prj
alu_cla_flags_tb.prj -top alu_cla_flags_tb
ISim P.20131013 (signature 0x7708f090)
Number of CPUs detected in this system: 8

Turning on mult-threading, number of parallel sub-compilation jobs: 16
Determining compilation order of HDL files
Parsing VHDL file "cla_gp.vhd" into library work
Parsing VHDL file "cla_add_n_bit.vhd" into library work
Parsing VHDL file "alu_cla.vhd" into library work
Parsing VHDL file "alu_cla_tb_FLAGS_IDEAL.vhd" into library work
Starting static elaboration
Completed static elaboration
Compiling package standard
Compiling package std_logic_1164
Compiling package textio
Compiling package std_logic_textio
Compiling package numeric_std
Compiling package attributes
Compiling package std_logic_misc
Compiling architecture ideal of entity cla_gp [cla_gp_default]
Compiling architecture ndv of entity cla_add_n_bit [\cla_add_n_bit(8)\]
Compiling architecture ndv of entity alu_cla [\alu_cla(8)\]
Compiling architecture test_alu_flags of entity alu_cla_flags_tb
Time Resolution for simulation is 1ps.
Waiting for 1 sub-compilation(s) to finish...
Compiled 14 VHDL Units
Built simulation executable alu_cla_flags_tb_isim_beh.exe
Fuse Memory Usage: 37560 KB
Fuse CPU Usage: 1092 ms

64200112>alu_cla_flags_tb_isim_beh.exe -tclbatch isim.tcl -wdb
alu_cla_flags_tb_isim_beh.wdb
ISim P.20131013 (signature 0x7708f090)
WARNING: A WEBPACK license was found.
WARNING: Please use Xilinx License Configuration Manager to check out a full ISim license.
WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for more information on the differences between the Lite and the Full version.
This is a Lite version of ISim.
Time resolution is 1 ps
Simulator is doing circuit initialization process.
Finished circuit initialization process.

```
-- *****
-- **** STUDENT: 64200163
-- *****
-- KOMENTARJI K OCENI NALOGE
-- Matej Možek: Ni pripomb
-- *****
```

```
64200163>rem ***** test cla adder
```

```
64200163>if not exist "xst" mkdir xst
```

```
64200163>cd XST
```

```
64200163\xst>if not exist "projnav.tmp" mkdir "projnav.tmp"
```

```
64200163\xst>cd ..
```

```
64200163>rem ***** test cla operations
```

```
64200163>xst -ifn cla_add_n_bit.xst
Release 14.7 - xst P.20131013 ( nt64 )
Copyright ( c ) 1995-2013 Xilinx, Inc. All rights reserved.
-- > Parameter TMPDIR set to xst/projnav.tmp
```

```
Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.25 secs
```

```
-- > Parameter xsthdpdir set to xst
```

```
Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.25 secs
```

```
-- >
```

```
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```
=====
* Synthesis Options Summary *
```

```
-- -- Source Parameters
```

```
Input File Name : "cla_add_n_bit.prj"
```

Ignore Synthesis Constraint File : NO

-- -- Target Parameters

Output File Name : "cla_add_n_bit"

Output Format : NGC

Target Device : xc6slx4-3-tqg144

-- -- Source Options

Top Module Name : cla_add_n_bit

Automatic FSM Extraction : YES

FSM Encoding Algorithm : Auto

Safe Implementation : No

FSM Style : LUT

RAM Extraction : Yes

RAM Style : Auto

ROM Extraction : Yes

Shift Register Extraction : YES

ROM Style : Auto

Resource Sharing : YES

Asynchronous To Synchronous : NO

Shift Register Minimum Size : 2

Use DSP Block : Auto

Automatic Register Balancing : No

-- -- Target Options

LUT Combining : Auto

Reduce Control Sets : Auto

Add IO Buffers : YES

Global Maximum Fanout : 100000

Add Generic Clock Buffer(BUFG) : 16

Register Duplication : YES

Optimize Instantiated Primitives : NO

Use Clock Enable : Auto

Use Synchronous Set : Auto

Use Synchronous Reset : Auto

Pack IO Registers into IOBs : Auto

Equivalent register Removal : YES

-- -- General Options

Optimization Goal : Speed

Optimization Effort : 1

Power Reduction : NO

Keep Hierarchy : No

Netlist Hierarchy : As_Optimized

RTL Output : Yes

Global Optimization : AllClockNets

Read Cores : YES

Write Timing Constraints : NO

Cross Clock Analysis : NO

Hierarchy Separator : /

Bus Delimiter : <>

Case Specifier : Maintain

Slice Utilization Ratio : 100

BRAM Utilization Ratio : 100

DSP48 Utilization Ratio : 100

Auto BRAM Packing : NO

Slice Utilization Ratio Delta : 5

=====

```

=====
* HDL Parsing *
=====
Parsing VHDL file "64200163\cla_gp.vhd" into library work
Parsing entity <cla_gp>.
Parsing architecture <ideal> of entity <cla_gp>.
Parsing VHDL file "64200163\cla_add_n_bit.vhd" into library work
Parsing entity <cla_add_n_bit>.
Parsing architecture <arch> of entity <cla_add_n_bit>.

=====
* HDL Elaboration *
=====

Elaborating entity <cla_add_n_bit> ( architecture <arch> ) with generics from
library <work>.

=====
* HDL Synthesis *
=====

Synthesizing Unit <cla_add_n_bit>.
Related source file is "64200163\cla_add_n_bit.vhd".
  n = 8
  Summary:
Unit <cla_add_n_bit> synthesized.

=====
HDL Synthesis Report

Macro Statistics
# Xors : 16
  1-bit xor2 : 16

=====

=====
* Advanced HDL Synthesis *
=====

=====
Advanced HDL Synthesis Report

Macro Statistics
# Xors : 16
  1-bit xor2 : 16

=====

=====
* Low Level Synthesis *
=====

Optimizing unit <cla_add_n_bit> ...

Mapping all equations...
Building and optimizing final netlist ...

```

Found area constraint ratio of 100 (+ 5) on block cla_add_n_bit, actual ratio is 1.

Final Macro Processing ...

=====
Final Register Report

Found no macro

=====
* Partition Report *
=====

Partition Implementation Status

-- -- -- -- -- -- -- -- -- -- -- -- -- --
-- -- -

No Partitions were found in this design.

-- -- -- -- -- -- -- -- -- -- -- -- -- --
-- -- -

=====
* Design Summary *
=====

Top Level Output File Name : cla_add_n_bit.ngc

Primitive and Black Box Usage:

-- -- -- -- -- -- -- -- -- -- -- -- -- --
-- -- -

BELS : 24
LUT2 : 6
LUT3 : 3
LUT5 : 6
LUT6 : 9
IO Buffers : 28
IBUF : 17
OBUF : 11

Device utilization summary:

-- -- -- -- -- -- -- -- -- -- -- -- -- --
-

Selected Device : 6slx4tqg144-3

Slice Logic Utilization:

Number of Slice LUTs: 24 out of 2400 1%
Number used as Logic: 24 out of 2400 1%

Slice Logic Distribution:

Number of LUT Flip Flop pairs used: 24
Number with an unused Flip Flop: 24 out of 24 100%
Number with an unused LUT: 0 out of 24 0%
Number of fully used LUT-FF pairs: 0 out of 24 0%
Number of unique control sets: 0

IO Utilization:

Number of IOs: 28

Number of bonded IOBs: 28 out of 102 27%

Specific Feature Utilization:

```
-- -- -- -- -- -- -- -- -- -- -- -- -- --
-
```

Partition Resource Summary:

```
-- -- -- -- -- -- -- -- -- -- -- -- -- --
-
```

No Partitions were found in this design.

```
-- -- -- -- -- -- -- -- -- -- -- -- -- --
-
```

=====
Timing Report

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.

FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT
GENERATED AFTER PLACE-and-ROUTE.

Clock Information:

```
-- -- -- -- -- -- -- -- -- -- -- -- -- --
```

No clock signals found in this design

Asynchronous Control Signals Information:

```
-- -- -- -- -- -- -- -- -- -- -- -- -- --
-- -- -- -- -- -- -- -- -- -- -- -- -- --
```

No asynchronous control signals found in this design

Timing Summary:

```
-- -- -- -- -- -- -- -- -- -- -- -- -- --
```

Speed Grade: -3

Minimum period: No path found

Minimum input arrival time before clock: No path found

Maximum output required time after clock: No path found

Maximum combinational path delay: 9.101ns

Timing Details:

```
-- -- -- -- -- -- -- -- -- -- -- -- -- --
```

All values displayed in nanoseconds (ns)

=====
Timing constraint: Default path analysis

Total number of paths / destination ports: 131 / 11

```
-- -- -- -- -- -- -- -- -- -- -- -- -- --
-- -- -- -- -- -- -- -- -- -- -- -- -- --
-- -- -- -- -- -- -- -- -- -- -- -- -- --
```

Delay: 9.101ns (Levels of Logic = 7)

Source: y<0> (PAD)

Destination: S<7> (PAD)

Data Path: y<0> to S<7>

Gate Net

Cell:in->out fanout Delay Delay Logical Name (Net Name)

```

--      --      --      --      --      --      --      --      --      --      --
--      --      --      --      --      --      --      --      --      --      --
--      --
IBUF:I->0 6 1.222 0.973 y_0_IBUF ( y_0_IBUF )
LUT3:I0->0 2 0.205 0.617 C<3>_SW0 ( N2 )
LUT5:I4->0 3 0.205 0.651 C<3> ( C<3> )
LUT3:I2->0 2 0.205 0.617 C<6>_SW0 ( N4 )
LUT5:I4->0 2 0.205 0.845 C<6> ( C<6> )
LUT5:I2->0 1 0.205 0.579 Mxor_S_sig<7>_xo<0>1 ( S_7_OBUF )
OBUF:I->0 2.571 S_7_OBUF ( S<7> )
--      --      --      --      --      --      --      --      --      --      --
--      --      --      --      --      --      --      --      --      --      --
Total 9.101ns ( 4.818ns logic, 4.283ns route )
( 52.9% logic, 47.1% route )

```

Cross Clock Domains Report:

```

Total REAL time to Xst completion: 9.00 secs
Total CPU time to Xst completion: 8.89 secs

```

```
-- >
```

Total memory usage is 4487500 kilobytes

Number of errors : 0 (0 filtered)

Number of warnings : 0 (0 filtered)

Number of infos : 0 (0 filtered)

```

64200163>fuse -incremental -o cla_add_n_bit_tb_isim_beh.exe -prj
cla_add_n_bit_tb.prj -top cla_add_n_bit_tb
Running: \unwrapped\fuse.exe -incremental -o cla_add_n_bit_tb_isim_beh.exe -prj
cla_add_n_bit_tb.prj -top cla_add_n_bit_tb
ISim P.20131013 ( signature 0x7708f090 )
Number of CPUs detected in this system: 8
Turning on mult-threading, number of parallel sub-compilation jobs: 16
Determining compilation order of HDL files
Parsing VHDL file "cla_gp.vhd" into library work
Parsing VHDL file "cla_add_n_bit.vhd" into library work
Parsing VHDL file "cla_add_n_bit_tb_IDEAL.vhd" into library work
Starting static elaboration
Completed static elaboration
Compiling package standard
Compiling package std_logic_1164
Compiling package textio
Compiling package std_logic_textio
Compiling package numeric_std
Compiling package attributes
Compiling package std_logic_misc
Compiling architecture arch of entity cla_add_n_bit [ \cla_add_n_bit( 8 ) \ ]
Compiling architecture testbench_arch of entity cla_add_n_bit_tb
Time Resolution for simulation is 1ps.
Waiting for 1 sub-compilation( s ) to finish...
Compiled 10 VHDL Units
Built simulation executable cla_add_n_bit_tb_isim_beh.exe

```

Fuse Memory Usage: 37428 KB
Fuse CPU Usage: 921 ms

```
64200163>cla_add_n_bit_tb_isim_beh.exe -tclbatch isim.tcl -wdb
cla_add_n_bit_tb_isim_beh.wdb
ISim P.20131013 ( signature 0x7708f090 )
WARNING: A WEBPACK license was found.
WARNING: Please use Xilinx License Configuration Manager to check out a full ISim
license.
WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for
more information on the differences between the Lite and the Full version.
This is a Lite version of ISim.
Time resolution is 1 ps
Simulator is doing circuit initialization process.
Finished circuit initialization process.
```

```
64200163>rem ***** test cla flags
```

```
64200163>xst -ifn cla_add_n_bit_flags.xst
Release 14.7 - xst P.20131013 ( nt64 )
Copyright ( c ) 1995-2013 Xilinx, Inc. All rights reserved.
-- > Parameter TMPDIR set to xst/projnav.tmp
```

Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.23 secs

```
-- > Parameter xsthdpdir set to xst
```

Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.23 secs

```
-- > ERROR:Xst:438 - Can not open file : cla_add_n_bit_flags.prj
```

Total REAL time to Xst completion: 1.00 secs
Total CPU time to Xst completion: 0.26 secs

```
-- >
```

Total memory usage is 4422880 kilobytes

Number of errors : 1 (0 filtered)
Number of warnings : 0 (0 filtered)
Number of infos : 0 (0 filtered)

```
64200163>fuse -incremental -o cla_add_n_bit_tb_flags_isim_beh.exe -prj
cla_add_n_bit_flags_tb.prj -top cla_add_n_bit_flags_tb_IDEAL
Running: \unwrapped\fuse.exe -incremental -o cla_add_n_bit_tb_flags_isim_beh.exe -
prj cla_add_n_bit_flags_tb.prj -top cla_add_n_bit_flags_tb_IDEAL
ISim P.20131013 ( signature 0x7708f090 )
Number of CPUs detected in this system: 8
Turning on mult-threading, number of parallel sub-compilation jobs: 16
Determining compilation order of HDL files
Parsing VHDL file "cla_gp.vhd" into library work
Parsing VHDL file "cla_add_n_bit.vhd" into library work
Parsing VHDL file "cla_add_n_bit_flags_tb_IDEAL.vhd" into library work
Starting static elaboration
Completed static elaboration
Compiling package standard
Compiling package std_logic_1164
```



```

Compiling package textio
Compiling package std_logic_textio
Compiling package numeric_std
Compiling package attributes
Compiling package std_logic_misc
Compiling architecture arch of entity cla_add_n_bit [\cla_add_n_bit( 8 )\]
Compiling architecture a1 of entity cla_add_n_bit_flags_tb_ideal
Time Resolution for simulation is 1ps.
Waiting for 1 sub-compilation( s ) to finish...
Compiled 10 VHDL Units
Built simulation executable cla_add_n_bit_tb_flags_isim_beh.exe
Fuse Memory Usage: 37320 KB
Fuse CPU Usage: 890 ms

64200163>cla_add_n_bit_tb_flags_isim_beh.exe -tclbatch isim.tcl -wdb
cla_add_n_bit_flags_tb.wdb
ISim P.20131013 ( signature 0x7708f090 )
WARNING: A WEBPACK license was found.
WARNING: Please use Xilinx License Configuration Manager to check out a full ISim
license.
WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for
more information on the differences between the Lite and the Full version.
This is a Lite version of ISim.
Time resolution is 1 ps
Simulator is doing circuit initialization process.
Finished circuit initialization process.

64200163>rem ***** test alu operations

64200163>xst -ifn alu_cla.xst
Release 14.7 - xst P.20131013 ( nt64 )
Copyright ( c ) 1995-2013 Xilinx, Inc. All rights reserved.
-- > Parameter TMPDIR set to xst/projnav.tmp

Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.25 secs

-- > Parameter xsthdmdir set to xst

Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.25 secs

-- >
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```

- 8.4.2) Asynchronous Control Signals Information
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- 8.4.5) Cross Clock Domains [Report](#)

```
=====
* Synthesis Options Summary *
=====
--      -- Source Parameters
Input File Name : "alu_cla.prj"
Ignore Synthesis Constraint File : NO

--      -- Target Parameters
Output File Name : "alu_cla"
Output Format : NGC
Target Device : xc6slx4-3-tqg144

--      -- Source Options
Top Module Name : alu_cla
Automatic FSM Extraction : YES
FSM Encoding Algorithm : Auto
Safe Implementation : No
FSM Style : LUT
RAM Extraction : Yes
RAM Style : Auto
ROM Extraction : Yes
Shift Register Extraction : YES
ROM Style : Auto
Resource Sharing : YES
Asynchronous To Synchronous : NO
Shift Register Minimum Size : 2
Use DSP Block : Auto
Automatic Register Balancing : No

--      -- Target Options
LUT Combining : Auto
Reduce Control Sets : Auto
Add IO Buffers : YES
Global Maximum Fanout : 100000
Add Generic Clock Buffer( BUFG ) : 16
Register Duplication : YES
Optimize Instantiated Primitives : NO
Use Clock Enable : Auto
Use Synchronous Set : Auto
Use Synchronous Reset : Auto
Pack IO Registers into IOBs : Auto
Equivalent register Removal : YES

--      -- General Options
Optimization Goal : Speed
Optimization Effort : 1
Power Reduction : NO
Keep Hierarchy : No
Netlist Hierarchy : As_Optimized
RTL Output : Yes
Global Optimization : AllClockNets
Read Cores : YES
Write Timing Constraints : NO
Cross Clock Analysis : NO
```

Hierarchy Separator : /
Bus Delimiter : <>
Case Specifier : Maintain
Slice Utilization Ratio : 100
BRAM Utilization Ratio : 100
DSP48 Utilization Ratio : 100
Auto BRAM Packing : NO
Slice Utilization Ratio Delta : 5

=====

=====

* HDL Parsing *

=====

Parsing VHDL file "64200163\cla_gp.vhd" into library work
Parsing entity <cla_gp>.
Parsing architecture <ideal> of entity <cla_gp>.
Parsing VHDL file "64200163\cla_add_n_bit.vhd" into library work
Parsing entity <cla_add_n_bit>.
Parsing architecture <arch> of entity <cla_add_n_bit>.
Parsing VHDL file "64200163\alu_cla.vhd" into library work
Parsing entity <alu_cla>.
Parsing architecture <NDV> of entity <alu_cla>.

=====

* HDL Elaboration *

=====

Elaborating entity <alu_cla> (architecture <NDV>) with generics from library <work>.

Elaborating entity <cla_add_n_bit> (architecture <arch>) with generics from library <work>.

=====

* HDL Synthesis *

=====

Synthesizing Unit <alu_cla>.
Related source file is "64200163\alu_cla.vhd".
n = 8
Found 8-bit 12-to-1 multiplexer for signal <S> created at line 45.
Summary:
inferred 7 Multiplexer(s).
Unit <alu_cla> synthesized.

Synthesizing Unit <cla_add_n_bit>.
Related source file is "64200163\cla_add_n_bit.vhd".
n = 8
Summary:
Unit <cla_add_n_bit> synthesized.

=====

HDL Synthesis Report

Macro Statistics

Multiplexers : 7
8-bit 12-to-1 multiplexer : 1
8-bit 2-to-1 multiplexer : 6

```
# Xors : 17
1-bit xor2 : 16
8-bit xor2 : 1
```

=====

=====

```
* Advanced HDL Synthesis *
```

=====

=====

Advanced HDL Synthesis Report

Macro Statistics

```
# Multiplexers : 7
8-bit 12-to-1 multiplexer : 1
8-bit 2-to-1 multiplexer : 6
# Xors : 17
1-bit xor2 : 16
8-bit xor2 : 1
```

=====

=====

```
* Low Level Synthesis *
```

=====

Optimizing unit <alu_cla> ...

Optimizing unit <cla_add_n_bit> ...

Mapping all equations...

Building and optimizing final netlist ...

Found area constraint ratio of 100 (+ 5) on block alu_cla, actual ratio is 3.

Final Macro Processing ...

=====

Final Register Report

Found no macro

=====

=====

```
* Partition Report *
```

=====

Partition Implementation Status

```
--      --      --      --      --      --      --      --      --      --      --      --
--      --      --      --      --      --      --      --      --      --      --      --
```

No Partitions were found in this design.

```
--      --      --      --      --      --      --      --      --      --      --      --
--      --      --      --      --      --      --      --      --      --      --      --
```

=====

```
* Design Summary *
```

=====

Primitive and Black Box Usage:

-- -- -- -- -- -- -- -- -- -- -- -- -- --
 -- -- -- -- -- -- -- -- -- -- -- -- -- --

```
# BELS : 49
# LUT3 : 3
# LUT5 : 14
# LUT6 : 30
# MUXF7 : 2
# IO Buffers : 34
# IBUF : 20
# OBUF : 14
```

Device utilization summary:

— — — — —

Selected Device : 6s1x4tqg144-3

Slice Logic Utilization:

Number of Slice LUTs: 47 out of 2400 1%
Number used as Logic: 47 out of 2400 1%

Slice Logic Distribution:

```

Number of LUT Flip Flop pairs used: 47
Number with an unused Flip Flop: 47 out of 47 100%
Number with an unused LUT: 0 out of 47 0%
Number of fully used LUT-FF pairs: 0 out of 47 0%
Number of unique control sets: 0

```

IO Utilization:

Number of IOs: 34
Number of bonded IOBs: 34 out of 102 33%

Specific Feature Utilization:

Partition Resource Summary:

No Partitions were found in this design.

1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53 54 55 56 57 58 59 60 61 62 63 64 65 66 67 68 69 70 71 72 73 74 75 76 77 78 79 80 81 82 83 84 85 86 87 88 89 90 91 92 93 94 95 96 97 98 99 100

Timing Report

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.
FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT
GENERATED AFTER PLACE-and-ROUTE.

Clock Information:

[illegible]

Asynchronous Control Signals Information:

```
-- -- -- -- -- -- -- -- -- -- -- -- -- --
-- -- -- -- -- -- -- -- -- -- -- -- -- --
```

No asynchronous control signals found in this design

Timing Summary:

```
-- -- -- -- -- -- -- -- -- -- -- -- -- --
```

Speed Grade: -3

Minimum period: No path found

Minimum input arrival time before clock: No path found

Maximum output required time after clock: No path found

Maximum combinational path delay: 12.446ns

Timing Details:

```
-- -- -- -- -- -- -- -- -- -- -- -- -- --
```

All values displayed in nanoseconds (ns)

=====
Timing constraint: Default path analysis

Total number of paths / destination ports: 918 / 14

```
-- -- -- -- -- -- -- -- -- -- -- -- -- --
-- -- -- -- -- -- -- -- -- -- -- -- -- --
-- -- -- -- -- -- -- -- -- -- -- -- -- --
```

Delay: 12.446ns (Levels of Logic = 9)

Source: F<2> (PAD)

Destination: Zero (PAD)

Data Path: F<2> to Zero

Gate Net

Cell:in->out fanout Delay Delay Logical Name (Net Name)

```
-- -- -- -- -- -- -- -- -- -- -- -- -- --
-- -- -- -- -- -- -- -- -- -- -- -- -- --
-- -- -- -- -- -- -- -- -- -- -- -- -- --
```

IBUF:I->0 30 1.222 1.608 F_2_IBUF (F_2_IBUF)

LUT6:I1->0 5 0.203 0.943 Mmux_Y_sig31 (Y_sig<1>)

LUT5:I2->0 4 0.205 0.684 U1/C<3>2 (U1/C<3>)

LUT3:I2->0 1 0.205 0.580 U1/C<6>_SW2 (N11)

LUT5:I4->0 3 0.205 0.879 U1/C<6> (U1/C<6>)

LUT5:I2->0 1 0.205 0.924 U1/Mxor_S_sig<7>_xo<0>1 (S_sig<7>)

LUT6:I1->0 4 0.203 1.028 Mmux_S22 (Negative_OBUF)

LUT6:I1->0 1 0.203 0.579 Zero (Zero_OBUF)

OBUF:I->0 2.571 Zero_OBUF (Zero)

```
-- -- -- -- -- -- -- -- -- -- -- -- -- --
-- -- -- -- -- -- -- -- -- -- -- -- -- --
```

Total 12.446ns (5.222ns logic, 7.224ns route)

(42.0% logic, 58.0% route)

=====
Cross Clock Domains Report:

```
-- -- -- -- -- -- -- -- -- -- -- -- -- --
```

=====
Total REAL time to Xst completion: 9.00 secs

Total CPU time to Xst completion: 9.31 secs

-- >

Total memory usage is 4488092 kilobytes

Number of errors : 0 (0 filtered)

Number of warnings : 0 (0 filtered)

Number of infos : 0 (0 filtered)

64200163>fuse -incremental -o alu_cla_tb_isim_beh.exe -prj alu_cla_tb.prj -top alu_cla_tb

Running: \unwrapped\fuse.exe -incremental -o alu_cla_tb_isim_beh.exe -prj alu_cla_tb.prj -top alu_cla_tb

ISim P.20131013 (signature 0x7708f090)

Number of CPUs detected in this system: 8

Turning on mult-threading, number of parallel sub-compilation jobs: 16

Determining compilation order of HDL files

Parsing VHDL file "cla_gp.vhd" into library work

Parsing VHDL file "cla_add_n_bit.vhd" into library work

Parsing VHDL file "alu_cla.vhd" into library work

Parsing VHDL file "alu_cla_tb_IDEAL.vhd" into library work

Starting static elaboration

Completed static elaboration

Compiling package standard

Compiling package std_logic_1164

Compiling package textio

Compiling package std_logic_textio

Compiling package numeric_std

Compiling package attributes

Compiling package std_logic_misc

Compiling architecture arch of entity cla_add_n_bit [\cla_add_n_bit(8)\]

Compiling architecture ndv of entity alu_cla [\alu_cla(8)\]

Compiling architecture testbench_arch of entity alu_cla_tb

Time Resolution for simulation is 1ps.

Waiting for 1 sub-compilation(s) to finish...

Compiled 12 VHDL Units

Built simulation executable alu_cla_tb_isim_beh.exe

Fuse Memory Usage: 37748 KB

Fuse CPU Usage: 952 ms

64200163>alu_cla_tb_isim_beh.exe -tclbatch isim.tcl -wdb alu_cla_tb_isim_beh.wdb

ISim P.20131013 (signature 0x7708f090)

WARNING: A WEBPACK license was found.

WARNING: Please use Xilinx License Configuration Manager to check out a full ISim license.

WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for more information on the differences between the Lite and the Full version.

This is a Lite version of ISim.

Time resolution is 1 ps

Simulator is doing circuit initialization process.

Finished circuit initialization process.

at 7864320 ns, Instance /alu_cla_tb/ : Warning: NUMERIC_STD.TO_UNSIGNED: vector truncated

at 8847360 ns, Instance /alu_cla_tb/ : Warning: NUMERIC_STD.TO_UNSIGNED: vector truncated

at 9830400 ns, Instance /alu_cla_tb/ : Warning: NUMERIC_STD.TO_UNSIGNED: vector truncated

at 10813440 ns, Instance /alu_cla_tb/ : Warning: NUMERIC_STD.TO_UNSIGNED: vector truncated

at 11796480 ns, Instance /alu_cla_tb/ : Warning: NUMERIC_STD.TO_UNSIGNED: vector truncated
at 12779520 ns, Instance /alu_cla_tb/ : Warning: NUMERIC_STD.TO_UNSIGNED: vector truncated
at 13762560 ns, Instance /alu_cla_tb/ : Warning: NUMERIC_STD.TO_UNSIGNED: vector truncated
at 14745600 ns, Instance /alu_cla_tb/ : Warning: NUMERIC_STD.TO_UNSIGNED: vector truncated

64200163>rem ***** test alu flags

64200163>xst -ifn alu_cla_flags.xst
Release 14.7 - xst P.20131013 (nt64)
Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.
-- > Parameter TMPDIR set to xst/projnav.tmp

Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.26 secs

-- > Parameter xsthdpdir set to xst

Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.26 secs

-- >

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 - 8.4.5) Cross Clock Domains Report

=====
* Synthesis Options Summary *

=====

-- -- Source Parameters

Input File Name : "alu_cla_flags_tb.prj"
Ignore Synthesis Constraint File : NO

-- -- Target Parameters

Output File Name : "alu_cla_flags_tb"
Output Format : NGC
Target Device : xc6slx4-3-tqg144

-- -- Source Options

Top Module Name : alu_cla_flags_tb
Automatic FSM Extraction : YES
FSM Encoding Algorithm : Auto
Safe Implementation : No
FSM Style : LUT
RAM Extraction : Yes
RAM Style : Auto
ROM Extraction : Yes
Shift Register Extraction : YES
ROM Style : Auto
Resource Sharing : YES
Asynchronous To Synchronous : NO
Shift Register Minimum Size : 2
Use DSP Block : Auto
Automatic Register Balancing : No

-- -- Target Options

LUT Combining : Auto
Reduce Control Sets : Auto
Add IO Buffers : YES
Global Maximum Fanout : 100000
Add Generic Clock Buffer(BUFG) : 16
Register Duplication : YES
Optimize Instantiated Primitives : NO
Use Clock Enable : Auto
Use Synchronous Set : Auto
Use Synchronous Reset : Auto
Pack IO Registers into IOBs : Auto
Equivalent register Removal : YES

-- -- General Options

Optimization Goal : Speed
Optimization Effort : 1
Power Reduction : NO
Keep Hierarchy : No
Netlist Hierarchy : As_Optimized
RTL Output : Yes
Global Optimization : AllClockNets
Read Cores : YES
Write Timing Constraints : NO
Cross Clock Analysis : NO
Hierarchy Separator : /
Bus Delimiter : <>
Case Specifier : Maintain
Slice Utilization Ratio : 100
BRAM Utilization Ratio : 100
DSP48 Utilization Ratio : 100
Auto BRAM Packing : NO
Slice Utilization Ratio Delta : 5

=====

=====

* HDL Parsing *

=====

Parsing VHDL file "64200163\cla_gp.vhd" into library work
Parsing entity <cla_gp>.
Parsing architecture <ideal> of entity <cla_gp>.
Parsing VHDL file "64200163\cla_add_n_bit.vhd" into library work

```

Parsing entity <cla_add_n_bit>.
Parsing architecture <arch> of entity <cla_add_n_bit>.
Parsing VHDL file "64200163\alu_cla.vhd" into library work
Parsing entity <alu_cla>.
Parsing architecture <NDV> of entity <alu_cla>.
Parsing VHDL file "64200163\alu_cla_tb_FLAGS_IDEAL.vhd" into library work
Parsing entity <alu_cla_flags_tb>.
Parsing architecture <test_alu_flags> of entity <alu_cla_flags_tb>.

=====
* HDL Elaboration *
=====

Elaborating entity <alu_cla_flags_tb> ( architecture <test_alu_flags> ) with
generics from library <work>.

Elaborating entity <alu_cla> ( architecture <NDV> ) with generics from library
<work>.

Elaborating entity <cla_add_n_bit> ( architecture <arch> ) with generics from
library <work>.
ERROR:HDLCompiler:890 - "64200163\alu_cla_tb_FLAGS_IDEAL.vhd" Line 144: wait
statement without UNTIL clause not supported for synthesis
Netlist alu_cla_flags_tb( 8 )( test_alu_flags ) remains a blackbox, due to errors
in its contents
-- >

Total memory usage is 4466680 kilobytes

Number of errors : 1 ( 0 filtered )
Number of warnings : 0 ( 0 filtered )
Number of infos : 0 ( 0 filtered )

64200163>fuse -incremental -o alu_cla_flags_tb_isim_beh.exe -prj
alu_cla_flags_tb.prj -top alu_cla_flags_tb
Running: \unwrapped\fuse.exe -incremental -o alu_cla_flags_tb_isim_beh.exe -prj
alu_cla_flags_tb.prj -top alu_cla_flags_tb
ISim P.20131013 ( signature 0x7708f090 )
Number of CPUs detected in this system: 8
Turning on mult-threading, number of parallel sub-compilation jobs: 16
Determining compilation order of HDL files
Parsing VHDL file "cla_gp.vhd" into library work
Parsing VHDL file "cla_add_n_bit.vhd" into library work
Parsing VHDL file "alu_cla.vhd" into library work
Parsing VHDL file "alu_cla_tb_FLAGS_IDEAL.vhd" into library work
Starting static elaboration
Completed static elaboration
Compiling package standard
Compiling package std_logic_1164
Compiling package textio
Compiling package std_logic_textio
Compiling package numeric_std
Compiling package attributes
Compiling package std_logic_misc
Compiling architecture arch of entity cla_add_n_bit [\cla_add_n_bit( 8 )\]
Compiling architecture ndv of entity alu_cla [\alu_cla( 8 )\]
Compiling architecture test_alu_flags of entity alu_cla_flags_tb
Time Resolution for simulation is 1ps.
Waiting for 1 sub-compilation( s ) to finish...

```

Compiled 12 VHDL Units
Built simulation executable alu_cla_flags_tb_isim_beh.exe
Fuse Memory Usage: 37596 KB
Fuse CPU Usage: 983 ms

```
64200163>alu_cla_flags_tb_isim_beh.exe -tclbatch isim.tcl -wdb
alu_cla_flags_tb_isim_beh.wdb
ISim P.20131013 ( signature 0x7708f090 )
WARNING: A WEBPACK license was found.
WARNING: Please use Xilinx License Configuration Manager to check out a full ISim
license.
WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for
more information on the differences between the Lite and the Full version.
This is a Lite version of ISim.
Time resolution is 1 ps
Simulator is doing circuit initialization process.
Finished circuit initialization process.
```

```
-- *****
-- **** STUDENT: 64200238
-- *****
-- KOMENTARJI K OCENI NALOGE
-- Matej Možek: Ni pripomb
-- *****
```

```
64200238>rem ***** test cla adder
```

```
64200238>if not exist "xst" mkdir xst
```

```
64200238>cd XST
```

```
64200238\xst>if not exist "projnav.tmp" mkdir "projnav.tmp"
```

```
64200238\xst>cd ..
```

```
64200238>rem ***** test cla operations
```

```
64200238>xst -ifn cla_add_n_bit.xst
Release 14.7 - xst P.20131013 ( nt64 )
Copyright ( c ) 1995-2013 Xilinx, Inc. All rights reserved.
-- > Parameter TMPDIR set to xst/projnav.tmp
```

```
Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.23 secs
```

```
-- > Parameter xsthdpdir set to xst
```

```
Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.24 secs
```

```
-- >
```

```
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 - 8.4.5) Cross Clock Domains Report

```
=====
* Synthesis Options Summary *
```

```
=====
-- -- Source Parameters
```

```
Input File Name : "cla_add_n_bit.prj"
```

Ignore Synthesis Constraint File : NO

-- -- Target Parameters

Output File Name : "cla_add_n_bit"

Output Format : NGC

Target Device : xc6slx4-3-tqg144

-- -- Source Options

Top Module Name : cla_add_n_bit

Automatic FSM Extraction : YES

FSM Encoding Algorithm : Auto

Safe Implementation : No

FSM Style : LUT

RAM Extraction : Yes

RAM Style : Auto

ROM Extraction : Yes

Shift Register Extraction : YES

ROM Style : Auto

Resource Sharing : YES

Asynchronous To Synchronous : NO

Shift Register Minimum Size : 2

Use DSP Block : Auto

Automatic Register Balancing : No

-- -- Target Options

LUT Combining : Auto

Reduce Control Sets : Auto

Add IO Buffers : YES

Global Maximum Fanout : 100000

Add Generic Clock Buffer(BUFG) : 16

Register Duplication : YES

Optimize Instantiated Primitives : NO

Use Clock Enable : Auto

Use Synchronous Set : Auto

Use Synchronous Reset : Auto

Pack IO Registers into IOBs : Auto

Equivalent register Removal : YES

-- -- General Options

Optimization Goal : Speed

Optimization Effort : 1

Power Reduction : NO

Keep Hierarchy : No

Netlist Hierarchy : As_Optimized

RTL Output : Yes

Global Optimization : AllClockNets

Read Cores : YES

Write Timing Constraints : NO

Cross Clock Analysis : NO

Hierarchy Separator : /

Bus Delimiter : <>

Case Specifier : Maintain

Slice Utilization Ratio : 100

BRAM Utilization Ratio : 100

DSP48 Utilization Ratio : 100

Auto BRAM Packing : NO

Slice Utilization Ratio Delta : 5

=====

```

=====
* HDL Parsing *
=====
Parsing VHDL file "64200238\cla_gp.vhd" into library work
Parsing entity <cla_gp>.
Parsing architecture <ideal> of entity <cla_gp>.
Parsing VHDL file "64200238\cla_add_n_bit.vhd" into library work
Parsing entity <cla_add_n_bit>.
Parsing architecture <NDV> of entity <cla_add_n_bit>.

=====
* HDL Elaboration *
=====

Elaborating entity <cla_add_n_bit> ( architecture <NDV> ) with generics from
library <work>.

=====
* HDL Synthesis *
=====

Synthesizing Unit <cla_add_n_bit>.
Related source file is "64200238\cla_add_n_bit.vhd".
  n = 8
  Summary:
Unit <cla_add_n_bit> synthesized.

=====
HDL Synthesis Report

Macro Statistics
# Xors : 16
  1-bit xor2 : 16

=====

=====
* Advanced HDL Synthesis *
=====

=====
Advanced HDL Synthesis Report

Macro Statistics
# Xors : 16
  1-bit xor2 : 16

=====

=====
* Low Level Synthesis *
=====

Optimizing unit <cla_add_n_bit> ...

Mapping all equations...
Building and optimizing final netlist ...

```

Found area constraint ratio of 100 (+ 5) on block cla_add_n_bit, actual ratio is 1.

Final Macro Processing ...

=====
Final Register Report

Found no macro

=====
* Partition Report *
=====

Partition Implementation Status

-- -- -- -- -- -- -- -- -- -- -- -- -- --
-- -- -

No Partitions were found in this design.

-- -- -- -- -- -- -- -- -- -- -- -- -- --
-- -- -

=====
* Design Summary *
=====

Top Level Output File Name : cla_add_n_bit.ngc

Primitive and Black Box Usage:

-- -- -- -- -- -- -- -- -- -- -- -- -- --
-- -- -

BELS : 24
LUT2 : 6
LUT3 : 3
LUT5 : 6
LUT6 : 9
IO Buffers : 28
IBUF : 17
OBUF : 11

Device utilization summary:

-- -- -- -- -- -- -- -- -- -- -- -- -- --
-

Selected Device : 6slx4tqg144-3

Slice Logic Utilization:

Number of Slice LUTs: 24 out of 2400 1%
Number used as Logic: 24 out of 2400 1%

Slice Logic Distribution:

Number of LUT Flip Flop pairs used: 24
Number with an unused Flip Flop: 24 out of 24 100%
Number with an unused LUT: 0 out of 24 0%
Number of fully used LUT-FF pairs: 0 out of 24 0%
Number of unique control sets: 0

IO Utilization:

Number of IOs: 28

Number of bonded IOBs: 28 out of 102 27%

Specific Feature Utilization:

```
-- -- -- -- -- -- -- -- -- -- -- -- -- --  
-
```

Partition Resource Summary:

```
-- -- -- -- -- -- -- -- -- -- -- -- -- --  
-
```

No Partitions were found in this design.

```
-- -- -- -- -- -- -- -- -- -- -- -- -- --  
-
```

=====
Timing Report

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.

FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT
GENERATED AFTER PLACE-and-ROUTE.

Clock Information:

```
-- -- -- -- -- -- -- -- -- -- -- -- -- --  
No clock signals found in this design
```

Asynchronous Control Signals Information:

```
-- -- -- -- -- -- -- -- -- -- -- -- -- --  
-- -- -- -- -- -- -- -- -- -- -- -- -- --
```

No asynchronous control signals found in this design

Timing Summary:

```
-- -- -- -- -- -- -- -- -- -- -- -- -- --
```

Speed Grade: -3

Minimum period: No path found

Minimum input arrival time before clock: No path found

Maximum output required time after clock: No path found

Maximum combinational path delay: 9.101ns

Timing Details:

```
-- -- -- -- -- -- -- -- -- -- -- -- -- --
```

All values displayed in nanoseconds (ns)

=====
Timing constraint: Default path analysis

Total number of paths / destination ports: 131 / 11

```
-- -- -- -- -- -- -- -- -- -- -- -- -- --  
-- -- -- -- -- -- -- -- -- -- -- -- -- --  
-- -- -- -- -- -- -- -- -- -- -- -- -- --
```

Delay: 9.101ns (Levels of Logic = 7)

Source: Y<0> (PAD)

Destination: S<7> (PAD)

Data Path: Y<0> to S<7>

Gate Net

Cell:in->out fanout Delay Delay Logical Name (Net Name)


```

--      --      --      --      --      --      --      --      --      --      --
--      --      --      --      --      --      --      --      --      --      --
--      --
IBUF:I->0 6 1.222 0.973 Y_0_IBUF ( Y_0_IBUF )
LUT3:I0->0 2 0.205 0.617 C<3>_SW0 ( N2 )
LUT5:I4->0 3 0.205 0.651 C<3> ( C<3> )
LUT3:I2->0 2 0.205 0.617 C<6>_SW0 ( N4 )
LUT5:I4->0 2 0.205 0.845 C<6> ( C<6> )
LUT5:I2->0 1 0.205 0.579 Mxor_S_sig<7>_xo<0>1 ( S_7_OBUF )
OBUF:I->0 2.571 S_7_OBUF ( S<7> )
--      --      --      --      --      --      --      --      --      --      --
--      --      --      --      --      --      --      --      --      --      --
Total 9.101ns ( 4.818ns logic, 4.283ns route )
( 52.9% logic, 47.1% route )

```

Cross Clock Domains Report:

```

Total REAL time to Xst completion: 9.00 secs
Total CPU time to Xst completion: 8.63 secs

```

```
-- >
```

Total memory usage is 4487500 kilobytes

Number of errors : 0 (0 filtered)

Number of warnings : 0 (0 filtered)

Number of infos : 0 (0 filtered)

```

64200238>fuse -incremental -o cla_add_n_bit_tb_isim_beh.exe -prj
cla_add_n_bit_tb.prj -top cla_add_n_bit_tb
Running: \unwrapped\fuse.exe -incremental -o cla_add_n_bit_tb_isim_beh.exe -prj
cla_add_n_bit_tb.prj -top cla_add_n_bit_tb
ISim P.20131013 ( signature 0x7708f090 )
Number of CPUs detected in this system: 8
Turning on mult-threading, number of parallel sub-compilation jobs: 16
Determining compilation order of HDL files
Parsing VHDL file "cla_gp.vhd" into library work
Parsing VHDL file "cla_add_n_bit.vhd" into library work
Parsing VHDL file "cla_add_n_bit_tb_IDEAL.vhd" into library work
Starting static elaboration
Completed static elaboration
Compiling package standard
Compiling package std_logic_1164
Compiling package textio
Compiling package std_logic_textio
Compiling package numeric_std
Compiling package attributes
Compiling package std_logic_misc
Compiling architecture ndv of entity cla_add_n_bit [\cla_add_n_bit( 8 )\]
Compiling architecture testbench_arch of entity cla_add_n_bit_tb
Time Resolution for simulation is 1ps.
Waiting for 1 sub-compilation( s ) to finish...
Compiled 10 VHDL Units
Built simulation executable cla_add_n_bit_tb_isim_beh.exe

```

Fuse Memory Usage: 36812 KB
Fuse CPU Usage: 890 ms

```
64200238>cla_add_n_bit_tb_isim_beh.exe -tclbatch isim.tcl -wdb
cla_add_n_bit_tb_isim_beh.wdb
ISim P.20131013 ( signature 0x7708f090 )
WARNING: A WEBPACK license was found.
WARNING: Please use Xilinx License Configuration Manager to check out a full ISim
license.
WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for
more information on the differences between the Lite and the Full version.
This is a Lite version of ISim.
Time resolution is 1 ps
Simulator is doing circuit initialization process.
Finished circuit initialization process.
```

```
64200238>rem ***** test cla flags
```

```
64200238>xst -ifn cla_add_n_bit_flags.xst
Release 14.7 - xst P.20131013 ( nt64 )
Copyright ( c ) 1995-2013 Xilinx, Inc. All rights reserved.
-- > Parameter TMPDIR set to xst/projnav.tmp
```

Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.23 secs

```
-- > Parameter xsthdpdir set to xst
```

Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.24 secs

```
-- > ERROR:Xst:438 - Can not open file : cla_add_n_bit_flags.prj
```

Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.26 secs

```
-- >
```

Total memory usage is 4422880 kilobytes

Number of errors : 1 (0 filtered)
Number of warnings : 0 (0 filtered)
Number of infos : 0 (0 filtered)

```
64200238>fuse -incremental -o cla_add_n_bit_tb_flags_isim_beh.exe -prj
cla_add_n_bit_flags_tb.prj -top cla_add_n_bit_flags_tb_IDEAL
Running: \unwrapped\fuse.exe -incremental -o cla_add_n_bit_tb_flags_isim_beh.exe -
prj cla_add_n_bit_flags_tb.prj -top cla_add_n_bit_flags_tb_IDEAL
ISim P.20131013 ( signature 0x7708f090 )
Number of CPUs detected in this system: 8
Turning on mult-threading, number of parallel sub-compilation jobs: 16
Determining compilation order of HDL files
Parsing VHDL file "cla_gp.vhd" into library work
Parsing VHDL file "cla_add_n_bit.vhd" into library work
Parsing VHDL file "cla_add_n_bit_flags_tb_IDEAL.vhd" into library work
Starting static elaboration
Completed static elaboration
Compiling package standard
Compiling package std_logic_1164
```

```

Compiling package textio
Compiling package std_logic_textio
Compiling package numeric_std
Compiling package attributes
Compiling package std_logic_misc
Compiling architecture ndv of entity cla_add_n_bit [\cla_add_n_bit( 8 )\]
Compiling architecture a1 of entity cla_add_n_bit_flags_tb_ideal
Time Resolution for simulation is 1ps.
Waiting for 1 sub-compilation( s ) to finish...
Compiled 10 VHDL Units
Built simulation executable cla_add_n_bit_tb_flags_isim_beh.exe
Fuse Memory Usage: 38140 KB
Fuse CPU Usage: 937 ms

64200238>cla_add_n_bit_tb_flags_isim_beh.exe -tclbatch isim.tcl -wdb
cla_add_n_bit_flags_tb.wdb
ISim P.20131013 ( signature 0x7708f090 )
WARNING: A WEBPACK license was found.
WARNING: Please use Xilinx License Configuration Manager to check out a full ISim
license.
WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for
more information on the differences between the Lite and the Full version.
This is a Lite version of ISim.
Time resolution is 1 ps
Simulator is doing circuit initialization process.
Finished circuit initialization process.

64200238>rem ***** test alu operations

64200238>xst -ifn alu_cla.xst
Release 14.7 - xst P.20131013 ( nt64 )
Copyright ( c ) 1995-2013 Xilinx, Inc. All rights reserved.
-- > Parameter TMPDIR set to xst/projnav.tmp

Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.23 secs

-- > Parameter xsthdpdir set to xst

Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.23 secs

-- >
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8.4.1 ) Clock Information

```

- 8.4.2) Asynchronous Control Signals Information
- 8.4.3) Timing Summary
- 8.4.4) Timing Details
- 8.4.5) Cross Clock Domains [Report](#)

```
=====
* Synthesis Options Summary *
=====
--      -- Source Parameters
Input File Name : "alu_cla.prj"
Ignore Synthesis Constraint File : NO

--      -- Target Parameters
Output File Name : "alu_cla"
Output Format : NGC
Target Device : xc6slx4-3-tqg144

--      -- Source Options
Top Module Name : alu_cla
Automatic FSM Extraction : YES
FSM Encoding Algorithm : Auto
Safe Implementation : No
FSM Style : LUT
RAM Extraction : Yes
RAM Style : Auto
ROM Extraction : Yes
Shift Register Extraction : YES
ROM Style : Auto
Resource Sharing : YES
Asynchronous To Synchronous : NO
Shift Register Minimum Size : 2
Use DSP Block : Auto
Automatic Register Balancing : No

--      -- Target Options
LUT Combining : Auto
Reduce Control Sets : Auto
Add IO Buffers : YES
Global Maximum Fanout : 100000
Add Generic Clock Buffer( BUFG ) : 16
Register Duplication : YES
Optimize Instantiated Primitives : NO
Use Clock Enable : Auto
Use Synchronous Set : Auto
Use Synchronous Reset : Auto
Pack IO Registers into IOBs : Auto
Equivalent register Removal : YES

--      -- General Options
Optimization Goal : Speed
Optimization Effort : 1
Power Reduction : NO
Keep Hierarchy : No
Netlist Hierarchy : As_Optimized
RTL Output : Yes
Global Optimization : AllClockNets
Read Cores : YES
Write Timing Constraints : NO
Cross Clock Analysis : NO
```

Hierarchy Separator : /
Bus Delimiter : <>
Case Specifier : Maintain
Slice Utilization Ratio : 100
BRAM Utilization Ratio : 100
DSP48 Utilization Ratio : 100
Auto BRAM Packing : NO
Slice Utilization Ratio Delta : 5

=====

=====

* HDL Parsing *

=====

Parsing VHDL file "64200238\cla_gp.vhd" into library work
Parsing entity <cla_gp>.
Parsing architecture <ideal> of entity <cla_gp>.
Parsing VHDL file "64200238\cla_add_n_bit.vhd" into library work
Parsing entity <cla_add_n_bit>.
Parsing architecture <NDV> of entity <cla_add_n_bit>.
Parsing VHDL file "64200238\alu_cla.vhd" into library work
Parsing entity <alu_cla>.
Parsing architecture <NDV> of entity <alu_cla>.

=====

* HDL Elaboration *

=====

Elaborating entity <alu_cla> (architecture <NDV>) with generics from library <work>.

Elaborating entity <cla_add_n_bit> (architecture <NDV>) with generics from library <work>.

=====

* HDL Synthesis *

=====

Synthesizing Unit <alu_cla>.
Related source file is "64200238\alu_cla.vhd".
n = 8
Found 8-bit 12-to-1 multiplexer for signal <S> created at line 67.
Summary:
inferred 17 Multiplexer(s).
Unit <alu_cla> synthesized.

Synthesizing Unit <cla_add_n_bit>.
Related source file is "64200238\cla_add_n_bit.vhd".
n = 8
Summary:
Unit <cla_add_n_bit> synthesized.

=====

HDL Synthesis Report

Macro Statistics

Multiplexers : 17
1-bit 2-to-1 multiplexer : 10
8-bit 12-to-1 multiplexer : 1

```
8-bit 2-to-1 multiplexer : 6
# Xors : 17
1-bit xor2 : 16
8-bit xor2 : 1
```

=====

=====

* Advanced HDL Synthesis *

=====

=====

Advanced HDL Synthesis Report

Macro Statistics

```
# Multiplexers : 17
1-bit 2-to-1 multiplexer : 10
8-bit 12-to-1 multiplexer : 1
8-bit 2-to-1 multiplexer : 6
# Xors : 17
1-bit xor2 : 16
8-bit xor2 : 1
```

=====

=====

* Low Level Synthesis *

=====

Optimizing unit <alu_cla> ...

Optimizing unit <cla_add_n_bit> ...

Mapping all equations...

Building and optimizing final netlist ...

Found area constraint ratio of 100 (+ 5) on block alu_cla, actual ratio is 3.

Final Macro Processing ...

=====

Final Register Report

Found no macro

=====

=====

* Partition Report *

=====

Partition Implementation Status

```
--      --      --      --      --      --      --      --      --      --      --      --
--      --      --      --      --      --      --      --      --      --      --      --
```

No Partitions were found in this design.

```
--      --      --      --      --      --      --      --      --      --      --      --
--      --      --      --      --      --      --      --      --      --      --      --
```

=====

* Design Summary *

=====

Top Level Output File Name : alu_cla.ngc

Primitive and Black Box Usage:

```
--      --      --      --      --      --      --      --      --      --      --      --
--      --      --
# BELS : 60
# LUT3 : 4
# LUT5 : 14
# LUT6 : 41
# MUXF7 : 1
# IO Buffers : 34
# IBUF : 20
# OBUF : 14
```

Device utilization summary:

```
--      --      --      --      --      --      --      --      --      --      --      --
-
```

Selected Device : 6slx4tqg144-3

Slice Logic Utilization:

Number of Slice LUTs: 59 out of 2400 2%
Number used as Logic: 59 out of 2400 2%

Slice Logic Distribution:

Number of LUT Flip Flop pairs used: 59
Number with an unused Flip Flop: 59 out of 59 100%
Number with an unused LUT: 0 out of 59 0%
Number of fully used LUT-FF pairs: 0 out of 59 0%
Number of unique control sets: 0

IO Utilization:

Number of IOs: 34
Number of bonded IOBs: 34 out of 102 33%

Specific Feature Utilization:

```
--      --      --      --      --      --      --      --      --      --      --      --
-
```

Partition Resource Summary:

```
--      --      --      --      --      --      --      --      --      --      --      --
-
```

No Partitions were found in this design.

```
--      --      --      --      --      --      --      --      --      --      --      --
-
```

=====

Timing Report

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.
FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT
GENERATED AFTER PLACE-and-ROUTE.

Clock Information:

```

--      --      --      --      --      --      --      --      --
No clock signals found in this design

Asynchronous Control Signals Information:
--      --      --      --      --      --      --      --      --
--      --      --      --      --      --      --      --      --
No asynchronous control signals found in this design

Timing Summary:
--      --      --      --      --      --      --      --
Speed Grade: -3

Minimum period: No path found
Minimum input arrival time before clock: No path found
Maximum output required time after clock: No path found
Maximum combinational path delay: 11.168ns

Timing Details:
--      --      --      --      --      --      --      --
All values displayed in nanoseconds ( ns )

=====
Timing constraint: Default path analysis
Total number of paths / destination ports: 1146 / 14
--      --      --      --      --      --      --      --      --
--      --      --      --      --      --      --      --      --
--      --      --      --      --      --      --      --      --
Delay: 11.168ns ( Levels of Logic = 8 )
Source: F<2> ( PAD )
Destination: Negative ( PAD )

Data Path: F<2> to Negative
Gate Net
Cell:in->out fanout Delay Delay Logical Name ( Net Name )
--      --      --      --      --      --      --      --      --
--      --      --      --      --      --      --      --      --
--      --      --      --      --      --      --      --      --
IBUF:I->O 35 1.222 1.679 F_2_IBUF ( F_2_IBUF )
LUT6:I1->O 6 0.203 0.973 Mmux_Y_sig31 ( Y_sig<1> )
LUT5:I2->O 4 0.205 1.028 U1/C<3>2 ( U1/C<3> )
LUT6:I1->O 1 0.203 0.000 U1/C<6>_G ( N16 )
MUXF7:I1->O 5 0.140 0.943 U1/C<6> ( U1/C<6> )
LUT5:I2->O 3 0.205 1.015 U1/Mxor_S_sig<7>_xo<0>1 ( S_temp<7> )
LUT6:I0->O 1 0.203 0.579 Mmux_Negative1 ( Negative_OBUF )
OBUF:I->O 2.571 Negative_OBUF ( Negative )
--      --      --      --      --      --      --      --      --
--      --      --      --      --      --      --      --      --
Total 11.168ns ( 4.952ns logic, 6.216ns route )
( 44.3% logic, 55.7% route )

=====

Cross Clock Domains Report:
--      --      --      --      --      --      --      --      --
--      --      --      --      --      --      --      --      --
=====

Total REAL time to Xst completion: 9.00 secs
Total CPU time to Xst completion: 9.53 secs

```


-- >

Total memory usage is 4487500 kilobytes

Number of errors : 0 (0 filtered)

Number of warnings : 0 (0 filtered)

Number of infos : 0 (0 filtered)

64200238>fuse -incremental -o alu_cla_tb_isim_beh.exe -prj alu_cla_tb.prj -top alu_cla_tb

Running: \unwrapped\fuse.exe -incremental -o alu_cla_tb_isim_beh.exe -prj alu_cla_tb.prj -top alu_cla_tb

ISim P.20131013 (signature 0x7708f090)

Number of CPUs detected in this system: 8

Turning on mult-threading, number of parallel sub-compilation jobs: 16

Determining compilation order of HDL files

Parsing VHDL file "cla_gp.vhd" into library work

Parsing VHDL file "cla_add_n_bit.vhd" into library work

Parsing VHDL file "alu_cla.vhd" into library work

Parsing VHDL file "alu_cla_tb_IDEAL.vhd" into library work

Starting static elaboration

Completed static elaboration

Compiling package standard

Compiling package std_logic_1164

Compiling package textio

Compiling package std_logic_textio

Compiling package numeric_std

Compiling package attributes

Compiling package std_logic_misc

Compiling architecture ndv of entity cla_add_n_bit [\cla_add_n_bit(8)\]

Compiling architecture ndv of entity alu_cla [\alu_cla(8)\]

Compiling architecture testbench_arch of entity alu_cla_tb

Time Resolution for simulation is 1ps.

Compiled 12 VHDL Units

Built simulation executable alu_cla_tb_isim_beh.exe

Fuse Memory Usage: 37136 KB

Fuse CPU Usage: 984 ms

64200238>alu_cla_tb_isim_beh.exe -tclbatch isim.tcl -wdb alu_cla_tb_isim_beh.wdb

ISim P.20131013 (signature 0x7708f090)

WARNING: A WEBPACK license was found.

WARNING: Please use Xilinx License Configuration Manager to check out a full ISim license.

WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for more information on the differences between the Lite and the Full version.

This is a Lite version of ISim.

Time resolution is 1 ps

Simulator is doing circuit initialization process.

Finished circuit initialization process.

at 7864320 ns, Instance /alu_cla_tb/ : Warning: NUMERIC_STD.TO_UNSIGNED: vector truncated

at 8847360 ns, Instance /alu_cla_tb/ : Warning: NUMERIC_STD.TO_UNSIGNED: vector truncated

at 9830400 ns, Instance /alu_cla_tb/ : Warning: NUMERIC_STD.TO_UNSIGNED: vector truncated

at 10813440 ns, Instance /alu_cla_tb/ : Warning: NUMERIC_STD.TO_UNSIGNED: vector truncated

at 11796480 ns, Instance /alu_cla_tb/ : Warning: NUMERIC_STD.TO_UNSIGNED: vector truncated
at 12779520 ns, Instance /alu_cla_tb/ : Warning: NUMERIC_STD.TO_UNSIGNED: vector truncated
at 13762560 ns, Instance /alu_cla_tb/ : Warning: NUMERIC_STD.TO_UNSIGNED: vector truncated
at 14745600 ns, Instance /alu_cla_tb/ : Warning: NUMERIC_STD.TO_UNSIGNED: vector truncated

64200238>rem ***** test alu flags

64200238>xst -ifn alu_cla_flags.xst
Release 14.7 - xst P.20131013 (nt64)
Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.
-- > Parameter TMPDIR set to xst/projnav.tmp

Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.24 secs

-- > Parameter xsthdpdir set to xst

Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.24 secs

-- >

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=====
* Synthesis Options Summary *

=====

-- -- Source Parameters

Input File Name : "alu_cla_flags_tb.prj"
Ignore Synthesis Constraint File : NO

-- -- Target Parameters

Output File Name : "alu_cla_flags_tb"
Output Format : NGC
Target Device : xc6slx4-3-tqg144

-- -- Source Options

Top Module Name : alu_cla_flags_tb
Automatic FSM Extraction : YES
FSM Encoding Algorithm : Auto
Safe Implementation : No
FSM Style : LUT
RAM Extraction : Yes
RAM Style : Auto
ROM Extraction : Yes
Shift Register Extraction : YES
ROM Style : Auto
Resource Sharing : YES
Asynchronous To Synchronous : NO
Shift Register Minimum Size : 2
Use DSP Block : Auto
Automatic Register Balancing : No

-- -- Target Options

LUT Combining : Auto
Reduce Control Sets : Auto
Add IO Buffers : YES
Global Maximum Fanout : 100000
Add Generic Clock Buffer(BUFG) : 16
Register Duplication : YES
Optimize Instantiated Primitives : NO
Use Clock Enable : Auto
Use Synchronous Set : Auto
Use Synchronous Reset : Auto
Pack IO Registers into IOBs : Auto
Equivalent register Removal : YES

-- -- General Options

Optimization Goal : Speed
Optimization Effort : 1
Power Reduction : NO
Keep Hierarchy : No
Netlist Hierarchy : As_Optimized
RTL Output : Yes
Global Optimization : AllClockNets
Read Cores : YES
Write Timing Constraints : NO
Cross Clock Analysis : NO
Hierarchy Separator : /
Bus Delimiter : <>
Case Specifier : Maintain
Slice Utilization Ratio : 100
BRAM Utilization Ratio : 100
DSP48 Utilization Ratio : 100
Auto BRAM Packing : NO
Slice Utilization Ratio Delta : 5

=====

=====

* HDL Parsing *

=====

Parsing VHDL file "64200238\cla_gp.vhd" into library work
Parsing entity <cla_gp>.
Parsing architecture <ideal> of entity <cla_gp>.
Parsing VHDL file "64200238\cla_add_n_bit.vhd" into library work

```

Parsing entity <cla_add_n_bit>.
Parsing architecture <NDV> of entity <cla_add_n_bit>.
Parsing VHDL file "64200238\alu_cla.vhd" into library work
Parsing entity <alu_cla>.
Parsing architecture <NDV> of entity <alu_cla>.
Parsing VHDL file "64200238\alu_cla_tb_FLAGS_IDEAL.vhd" into library work
Parsing entity <alu_cla_flags_tb>.
Parsing architecture <test_alu_flags> of entity <alu_cla_flags_tb>.

=====
* HDL Elaboration *
=====

Elaborating entity <alu_cla_flags_tb> ( architecture <test_alu_flags> ) with
generics from library <work>.

Elaborating entity <alu_cla> ( architecture <NDV> ) with generics from library
<work>.

Elaborating entity <cla_add_n_bit> ( architecture <NDV> ) with generics from
library <work>.
ERROR:HDLCompiler:890 - "64200238\alu_cla_tb_FLAGS_IDEAL.vhd" Line 144: wait
statement without UNTIL clause not supported for synthesis
Netlist alu_cla_flags_tb( 8 )( test_alu_flags ) remains a blackbox, due to errors
in its contents
-- >

Total memory usage is 4466680 kilobytes

Number of errors : 1 ( 0 filtered )
Number of warnings : 0 ( 0 filtered )
Number of infos : 0 ( 0 filtered )

64200238>fuse -incremental -o alu_cla_flags_tb_isim_beh.exe -prj
alu_cla_flags_tb.prj -top alu_cla_flags_tb
Running: \unwrapped\fuse.exe -incremental -o alu_cla_flags_tb_isim_beh.exe -prj
alu_cla_flags_tb.prj -top alu_cla_flags_tb
ISim P.20131013 ( signature 0x7708f090 )
Number of CPUs detected in this system: 8
Turning on mult-threading, number of parallel sub-compilation jobs: 16
Determining compilation order of HDL files
Parsing VHDL file "cla_gp.vhd" into library work
Parsing VHDL file "cla_add_n_bit.vhd" into library work
Parsing VHDL file "alu_cla.vhd" into library work
Parsing VHDL file "alu_cla_tb_FLAGS_IDEAL.vhd" into library work
Starting static elaboration
Completed static elaboration
Compiling package standard
Compiling package std_logic_1164
Compiling package textio
Compiling package std_logic_textio
Compiling package numeric_std
Compiling package attributes
Compiling package std_logic_misc
Compiling architecture ndv of entity cla_add_n_bit [\cla_add_n_bit( 8 )\]
Compiling architecture ndv of entity alu_cla [\alu_cla( 8 )\]
Compiling architecture test_alu_flags of entity alu_cla_flags_tb
Time Resolution for simulation is 1ps.
Waiting for 1 sub-compilation( s ) to finish...

```

Compiled 12 VHDL Units
Built simulation executable alu_cla_flags_tb_isim_beh.exe
Fuse Memory Usage: 37512 KB
Fuse CPU Usage: 1030 ms

```
64200238>alu_cla_flags_tb_isim_beh.exe -tclbatch isim.tcl -wdb
alu_cla_flags_tb_isim_beh.wdb
ISim P.20131013 ( signature 0x7708f090 )
WARNING: A WEBPACK license was found.
WARNING: Please use Xilinx License Configuration Manager to check out a full ISim
license.
WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for
more information on the differences between the Lite and the Full version.
This is a Lite version of ISim.
Time resolution is 1 ps
Simulator is doing circuit initialization process.
Finished circuit initialization process.
```

```
-- *****
-- **** STUDENT: 64200288
-- *****
-- KOMENTARJI K OCENI NALOGE
-- Matej Možek: Ni pripomb
-- *****
```

```
64200288>rem ***** test cla adder
```

```
64200288>if not exist "xst" mkdir xst
```

```
64200288>cd XST
```

```
64200288\xst>if not exist "projnav.tmp" mkdir "projnav.tmp"
```

```
64200288\xst>cd ..
```

```
64200288>rem ***** test cla operations
```

```
64200288>xst -ifn cla_add_n_bit.xst
Release 14.7 - xst P.20131013 ( nt64 )
Copyright ( c ) 1995-2013 Xilinx, Inc. All rights reserved.
-- > Parameter TMPDIR set to xst/projnav.tmp
```

```
Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.23 secs
```

```
-- > Parameter xsthdpdir set to xst
```

```
Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.23 secs
```

```
-- >
```

```
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- 8.4.5) Cross Clock Domains Report

```
=====
* Synthesis Options Summary *
```

```
=====
-- -- Source Parameters
```

```
Input File Name : "cla_add_n_bit.prj"
```

Ignore Synthesis Constraint File : NO

-- -- Target Parameters

Output File Name : "cla_add_n_bit"

Output Format : NGC

Target Device : xc6slx4-3-tqg144

-- -- Source Options

Top Module Name : cla_add_n_bit

Automatic FSM Extraction : YES

FSM Encoding Algorithm : Auto

Safe Implementation : No

FSM Style : LUT

RAM Extraction : Yes

RAM Style : Auto

ROM Extraction : Yes

Shift Register Extraction : YES

ROM Style : Auto

Resource Sharing : YES

Asynchronous To Synchronous : NO

Shift Register Minimum Size : 2

Use DSP Block : Auto

Automatic Register Balancing : No

-- -- Target Options

LUT Combining : Auto

Reduce Control Sets : Auto

Add IO Buffers : YES

Global Maximum Fanout : 100000

Add Generic Clock Buffer(BUFG) : 16

Register Duplication : YES

Optimize Instantiated Primitives : NO

Use Clock Enable : Auto

Use Synchronous Set : Auto

Use Synchronous Reset : Auto

Pack IO Registers into IOBs : Auto

Equivalent register Removal : YES

-- -- General Options

Optimization Goal : Speed

Optimization Effort : 1

Power Reduction : NO

Keep Hierarchy : No

Netlist Hierarchy : As_Optimized

RTL Output : Yes

Global Optimization : AllClockNets

Read Cores : YES

Write Timing Constraints : NO

Cross Clock Analysis : NO

Hierarchy Separator : /

Bus Delimiter : <>

Case Specifier : Maintain

Slice Utilization Ratio : 100

BRAM Utilization Ratio : 100

DSP48 Utilization Ratio : 100

Auto BRAM Packing : NO

Slice Utilization Ratio Delta : 5

=====

```

=====
* HDL Parsing *
=====
Parsing VHDL file "64200288\cla_gp.vhd" into library work
Parsing entity <cla_gp>.
Parsing architecture <ideal> of entity <cla_gp>.
Parsing VHDL file "64200288\cla_add_n_bit.vhd" into library work
Parsing entity <cla_add_n_bit>.
Parsing architecture <NDV> of entity <cla_add_n_bit>.

=====
* HDL Elaboration *
=====

Elaborating entity <cla_add_n_bit> ( architecture <NDV> ) with generics from
library <work>.

=====
* HDL Synthesis *
=====

Synthesizing Unit <cla_add_n_bit>.
Related source file is "64200288\cla_add_n_bit.vhd".
n = 8
Summary:
Unit <cla_add_n_bit> synthesized.

=====
HDL Synthesis Report

Macro Statistics
# Xors : 16
1-bit xor2 : 16

=====

=====
* Advanced HDL Synthesis *
=====

=====
Advanced HDL Synthesis Report

Macro Statistics
# Xors : 16
1-bit xor2 : 16

=====

=====
* Low Level Synthesis *
=====

Optimizing unit <cla_add_n_bit> ...

Mapping all equations...
Building and optimizing final netlist ...

```


Found area constraint ratio of 100 (+ 5) on block cla_add_n_bit, actual ratio is 1.

Final Macro Processing ...

=====
Final Register Report

Found no macro

=====
* Partition Report *
=====

Partition Implementation Status

-- -- -- -- -- -- -- -- -- -- -- -- -- --
-- -- -

No Partitions were found in this design.

-- -- -- -- -- -- -- -- -- -- -- -- -- --
-- -- -

=====
* Design Summary *
=====

Top Level Output File Name : cla_add_n_bit.ngc

Primitive and Black Box Usage:

-- -- -- -- -- -- -- -- -- -- -- -- -- --
-- --

BELS : 24
LUT2 : 6
LUT3 : 3
LUT5 : 6
LUT6 : 9
IO Buffers : 28
IBUF : 17
OBUF : 11

Device utilization summary:

-- -- -- -- -- -- -- -- -- -- -- -- -- --
-

Selected Device : 6slx4tqg144-3

Slice Logic Utilization:

Number of Slice LUTs: 24 out of 2400 1%
Number used as Logic: 24 out of 2400 1%

Slice Logic Distribution:

Number of LUT Flip Flop pairs used: 24
Number with an unused Flip Flop: 24 out of 24 100%
Number with an unused LUT: 0 out of 24 0%
Number of fully used LUT-FF pairs: 0 out of 24 0%
Number of unique control sets: 0

IO Utilization:

Number of IOs: 28

Number of bonded IOBs: 28 out of 102 27%

Specific Feature Utilization:

```
-- -- -- -- -- -- -- -- -- -- -- -- -- --  
-
```

Partition Resource Summary:

```
-- -- -- -- -- -- -- -- -- -- -- -- -- --  
-
```

No Partitions were found in this design.

```
-- -- -- -- -- -- -- -- -- -- -- -- -- --  
-
```

=====
Timing Report

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.

FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT
GENERATED AFTER PLACE-and-ROUTE.

Clock Information:

```
-- -- -- -- -- -- -- -- -- -- -- -- -- --  
No clock signals found in this design
```

Asynchronous Control Signals Information:

```
-- -- -- -- -- -- -- -- -- -- -- -- -- --  
-- -- -- -- -- -- -- -- -- -- -- -- -- --
```

No asynchronous control signals found in this design

Timing Summary:

```
-- -- -- -- -- -- -- -- -- -- -- -- -- --
```

Speed Grade: -3

Minimum period: No path found

Minimum input arrival time before clock: No path found

Maximum output required time after clock: No path found

Maximum combinational path delay: 9.101ns

Timing Details:

```
-- -- -- -- -- -- -- -- -- -- -- -- -- --
```

All values displayed in nanoseconds (ns)

=====
Timing constraint: Default path analysis

Total number of paths / destination ports: 131 / 11

```
-- -- -- -- -- -- -- -- -- -- -- -- -- --  
-- -- -- -- -- -- -- -- -- -- -- -- -- --  
-- -- -- -- -- -- -- -- -- -- -- -- -- --
```

Delay: 9.101ns (Levels of Logic = 7)

Source: Y<0> (PAD)

Destination: S<7> (PAD)

Data Path: Y<0> to S<7>

Gate Net

Cell:in->out fanout Delay Delay Logical Name (Net Name)

```

--      --      --      --      --      --      --      --      --      --      --
--      --      --      --      --      --      --      --      --      --      --
--      --
IBUF:I->0 6 1.222 0.973 Y_0_IBUF ( Y_0_IBUF )
LUT3:I0->0 2 0.205 0.617 C<3>_SW0 ( N2 )
LUT5:I4->0 3 0.205 0.651 C<3> ( C<3> )
LUT3:I2->0 2 0.205 0.617 C<6>_SW0 ( N4 )
LUT5:I4->0 2 0.205 0.845 C<6> ( C<6> )
LUT5:I2->0 1 0.205 0.579 Mxor_S_sig<7>_xo<0>1 ( S_7_OBUF )
OBUF:I->0 2.571 S_7_OBUF ( S<7> )
--      --      --      --      --      --      --      --      --      --      --
--      --      --      --      --      --      --      --      --      --      --
Total 9.101ns ( 4.818ns logic, 4.283ns route )
( 52.9% logic, 47.1% route )

```

Cross Clock Domains Report:

```

Total REAL time to Xst completion: 9.00 secs
Total CPU time to Xst completion: 8.54 secs

```

```
-- >
```

Total memory usage is 4487500 kilobytes

Number of errors : 0 (0 filtered)

Number of warnings : 0 (0 filtered)

Number of infos : 0 (0 filtered)

```

64200288>fuse -incremental -o cla_add_n_bit_tb_isim_beh.exe -prj
cla_add_n_bit_tb.prj -top cla_add_n_bit_tb
Running: \unwrapped\fuse.exe -incremental -o cla_add_n_bit_tb_isim_beh.exe -prj
cla_add_n_bit_tb.prj -top cla_add_n_bit_tb
ISim P.20131013 ( signature 0x7708f090 )
Number of CPUs detected in this system: 8
Turning on mult-threading, number of parallel sub-compilation jobs: 16
Determining compilation order of HDL files
Parsing VHDL file "cla_gp.vhd" into library work
Parsing VHDL file "cla_add_n_bit.vhd" into library work
Parsing VHDL file "cla_add_n_bit_tb_IDEAL.vhd" into library work
Starting static elaboration
Completed static elaboration
Compiling package standard
Compiling package std_logic_1164
Compiling package textio
Compiling package std_logic_textio
Compiling package numeric_std
Compiling package attributes
Compiling package std_logic_misc
Compiling architecture ndv of entity cla_add_n_bit [\cla_add_n_bit( 8 )\]
Compiling architecture testbench_arch of entity cla_add_n_bit_tb
Time Resolution for simulation is 1ps.
Waiting for 1 sub-compilation( s ) to finish...
Compiled 10 VHDL Units
Built simulation executable cla_add_n_bit_tb_isim_beh.exe

```

Fuse Memory Usage: 37428 KB
Fuse CPU Usage: 937 ms

```
64200288>cla_add_n_bit_tb_isim_beh.exe -tclbatch isim.tcl -wdb
cla_add_n_bit_tb_isim_beh.wdb
ISim P.20131013 ( signature 0x7708f090 )
WARNING: A WEBPACK license was found.
WARNING: Please use Xilinx License Configuration Manager to check out a full ISim
license.
WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for
more information on the differences between the Lite and the Full version.
This is a Lite version of ISim.
Time resolution is 1 ps
Simulator is doing circuit initialization process.
Finished circuit initialization process.
```

```
64200288>rem ***** test cla flags
```

```
64200288>xst -ifn cla_add_n_bit_flags.xst
Release 14.7 - xst P.20131013 ( nt64 )
Copyright ( c ) 1995-2013 Xilinx, Inc. All rights reserved.
-- > Parameter TMPDIR set to xst/projnav.tmp
```

Total REAL time to Xst completion: 1.00 secs
Total CPU time to Xst completion: 0.23 secs

```
-- > Parameter xsthdpdir set to xst
```

Total REAL time to Xst completion: 1.00 secs
Total CPU time to Xst completion: 0.24 secs

```
-- > ERROR:Xst:438 - Can not open file : cla_add_n_bit_flags.prj
```

Total REAL time to Xst completion: 1.00 secs
Total CPU time to Xst completion: 0.26 secs

```
-- >
```

Total memory usage is 4422880 kilobytes

Number of errors : 1 (0 filtered)
Number of warnings : 0 (0 filtered)
Number of infos : 0 (0 filtered)

```
64200288>fuse -incremental -o cla_add_n_bit_tb_flags_isim_beh.exe -prj
cla_add_n_bit_flags_tb.prj -top cla_add_n_bit_flags_tb_IDEAL
Running: \unwrapped\fuse.exe -incremental -o cla_add_n_bit_tb_flags_isim_beh.exe -
prj cla_add_n_bit_flags_tb.prj -top cla_add_n_bit_flags_tb_IDEAL
ISim P.20131013 ( signature 0x7708f090 )
Number of CPUs detected in this system: 8
Turning on mult-threading, number of parallel sub-compilation jobs: 16
Determining compilation order of HDL files
Parsing VHDL file "cla_gp.vhd" into library work
Parsing VHDL file "cla_add_n_bit.vhd" into library work
Parsing VHDL file "cla_add_n_bit_flags_tb_IDEAL.vhd" into library work
Starting static elaboration
Completed static elaboration
Compiling package standard
Compiling package std_logic_1164
```

```

Compiling package textio
Compiling package std_logic_textio
Compiling package numeric_std
Compiling package attributes
Compiling package std_logic_misc
Compiling architecture ndv of entity cla_add_n_bit [\cla_add_n_bit( 8 )\]
Compiling architecture a1 of entity cla_add_n_bit_flags_tb_ideal
Time Resolution for simulation is 1ps.
Waiting for 1 sub-compilation( s ) to finish...
Compiled 10 VHDL Units
Built simulation executable cla_add_n_bit_tb_flags_isim_beh.exe
Fuse Memory Usage: 36764 KB
Fuse CPU Usage: 937 ms

64200288>cla_add_n_bit_tb_flags_isim_beh.exe -tclbatch isim.tcl -wdb
cla_add_n_bit_flags_tb.wdb
ISim P.20131013 ( signature 0x7708f090 )
WARNING: A WEBPACK license was found.
WARNING: Please use Xilinx License Configuration Manager to check out a full ISim
license.
WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for
more information on the differences between the Lite and the Full version.
This is a Lite version of ISim.
Time resolution is 1 ps
Simulator is doing circuit initialization process.
Finished circuit initialization process.

64200288>rem ***** test alu operations

64200288>xst -ifn alu_cla.xst
Release 14.7 - xst P.20131013 ( nt64 )
Copyright ( c ) 1995-2013 Xilinx, Inc. All rights reserved.
-- > Parameter TMPDIR set to xst/projnav.tmp

Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.25 secs

-- > Parameter xsthdpdir set to xst

Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.25 secs

-- >
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8.4.1 ) Clock Information

```

- 8.4.2) Asynchronous Control Signals Information
- 8.4.3) Timing Summary
- 8.4.4) Timing Details
- 8.4.5) Cross Clock Domains [Report](#)

```
=====
* Synthesis Options Summary *
=====
--      -- Source Parameters
Input File Name : "alu_cla.prj"
Ignore Synthesis Constraint File : NO

--      -- Target Parameters
Output File Name : "alu_cla"
Output Format : NGC
Target Device : xc6slx4-3-tqg144

--      -- Source Options
Top Module Name : alu_cla
Automatic FSM Extraction : YES
FSM Encoding Algorithm : Auto
Safe Implementation : No
FSM Style : LUT
RAM Extraction : Yes
RAM Style : Auto
ROM Extraction : Yes
Shift Register Extraction : YES
ROM Style : Auto
Resource Sharing : YES
Asynchronous To Synchronous : NO
Shift Register Minimum Size : 2
Use DSP Block : Auto
Automatic Register Balancing : No

--      -- Target Options
LUT Combining : Auto
Reduce Control Sets : Auto
Add IO Buffers : YES
Global Maximum Fanout : 100000
Add Generic Clock Buffer( BUFG ) : 16
Register Duplication : YES
Optimize Instantiated Primitives : NO
Use Clock Enable : Auto
Use Synchronous Set : Auto
Use Synchronous Reset : Auto
Pack IO Registers into IOBs : Auto
Equivalent register Removal : YES

--      -- General Options
Optimization Goal : Speed
Optimization Effort : 1
Power Reduction : NO
Keep Hierarchy : No
Netlist Hierarchy : As_Optimized
RTL Output : Yes
Global Optimization : AllClockNets
Read Cores : YES
Write Timing Constraints : NO
Cross Clock Analysis : NO
```

Hierarchy Separator : /
Bus Delimiter : <>
Case Specifier : Maintain
Slice Utilization Ratio : 100
BRAM Utilization Ratio : 100
DSP48 Utilization Ratio : 100
Auto BRAM Packing : NO
Slice Utilization Ratio Delta : 5

=====

=====

* HDL Parsing *

=====

Parsing VHDL file "64200288\cla_gp.vhd" into library work
Parsing entity <cla_gp>.
Parsing architecture <ideal> of entity <cla_gp>.
Parsing VHDL file "64200288\cla_add_n_bit.vhd" into library work
Parsing entity <cla_add_n_bit>.
Parsing architecture <NDV> of entity <cla_add_n_bit>.
Parsing VHDL file "64200288\alu_cla.vhd" into library work
Parsing entity <alu_cla>.
Parsing architecture <NDV> of entity <alu_cla>.

=====

* HDL Elaboration *

=====

Elaborating entity <alu_cla> (architecture <NDV>) with generics from library <work>.

Elaborating entity <cla_add_n_bit> (architecture <NDV>) with generics from library <work>.

=====

* HDL Synthesis *

=====

Synthesizing Unit <alu_cla>.
Related source file is "64200288\alu_cla.vhd".
n = 8
Found 8-bit 12-to-1 multiplexer for signal <S> created at line 63.
Summary:
inferred 17 Multiplexer(s).
Unit <alu_cla> synthesized.

Synthesizing Unit <cla_add_n_bit>.
Related source file is "64200288\cla_add_n_bit.vhd".
n = 8
Summary:
Unit <cla_add_n_bit> synthesized.

=====

HDL Synthesis Report

Macro Statistics

Multiplexers : 17
1-bit 2-to-1 multiplexer : 10
8-bit 12-to-1 multiplexer : 1

```
8-bit 2-to-1 multiplexer : 6
# Xors : 17
1-bit xor2 : 16
8-bit xor2 : 1
```

=====

=====

* Advanced HDL Synthesis *

=====

=====

Advanced HDL Synthesis Report

Macro Statistics

```
# Multiplexers : 17
1-bit 2-to-1 multiplexer : 10
8-bit 12-to-1 multiplexer : 1
8-bit 2-to-1 multiplexer : 6
# Xors : 17
1-bit xor2 : 16
8-bit xor2 : 1
```

=====

=====

* Low Level Synthesis *

=====

Optimizing unit <alu_cla> ...

Optimizing unit <cla_add_n_bit> ...

Mapping all equations...

Building and optimizing final netlist ...

Found area constraint ratio of 100 (+ 5) on block alu_cla, actual ratio is 3.

Final Macro Processing ...

=====

Final Register Report

Found no macro

=====

=====

* Partition Report *

=====

Partition Implementation Status

```
--      --      --      --      --      --      --      --      --      --      --      --
--      --      --      --      --      --      --      --      --      --      --      --
```

No Partitions were found in this design.

```
--      --      --      --      --      --      --      --      --      --      --      --
--      --      --      --      --      --      --      --      --      --      --      --
```

=====

* Design Summary *

=====

Top Level Output File Name : alu_cla.ngc

Primitive and Black Box Usage:

```
--      --      --      --      --      --      --      --      --      --      --      --
--      --      --
# BELS : 60
# LUT3 : 4
# LUT5 : 14
# LUT6 : 41
# MUXF7 : 1
# IO Buffers : 34
# IBUF : 20
# OBUF : 14
```

Device utilization summary:

```
--      --      --      --      --      --      --      --      --      --      --      --
-
```

Selected Device : 6slx4tqg144-3

Slice Logic Utilization:

Number of Slice LUTs: 59 out of 2400 2%
Number used as Logic: 59 out of 2400 2%

Slice Logic Distribution:

Number of LUT Flip Flop pairs used: 59
Number with an unused Flip Flop: 59 out of 59 100%
Number with an unused LUT: 0 out of 59 0%
Number of fully used LUT-FF pairs: 0 out of 59 0%
Number of unique control sets: 0

IO Utilization:

Number of IOs: 34
Number of bonded IOBs: 34 out of 102 33%

Specific Feature Utilization:

```
--      --      --      --      --      --      --      --      --      --      --      --
-
```

Partition Resource Summary:

```
--      --      --      --      --      --      --      --      --      --      --      --
-
```

No Partitions were found in this design.

```
--      --      --      --      --      --      --      --      --      --      --      --
-
```

=====

Timing Report

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.
FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT
GENERATED AFTER PLACE-and-ROUTE.

Clock Information:

```

--      --      --      --      --      --      --      --      --
No clock signals found in this design

Asynchronous Control Signals Information:
--      --      --      --      --      --      --      --      --
--      --      --      --      --      --      --      --      --
No asynchronous control signals found in this design

Timing Summary:
--      --      --      --      --      --      --      --
Speed Grade: -3

Minimum period: No path found
Minimum input arrival time before clock: No path found
Maximum output required time after clock: No path found
Maximum combinational path delay: 11.168ns

Timing Details:
--      --      --      --      --      --      --      --
All values displayed in nanoseconds ( ns )

=====
Timing constraint: Default path analysis
Total number of paths / destination ports: 1146 / 14
--      --      --      --      --      --      --      --      --
--      --      --      --      --      --      --      --      --
--      --      --      --      --      --      --      --      --
Delay: 11.168ns ( Levels of Logic = 8 )
Source: F<2> ( PAD )
Destination: Negative ( PAD )

Data Path: F<2> to Negative
Gate Net
Cell:in->out fanout Delay Delay Logical Name ( Net Name )
--      --      --      --      --      --      --      --      --
--      --      --      --      --      --      --      --      --
--      --      --      --      --      --      --      --      --
IBUF:I->O 35 1.222 1.679 F_2_IBUF ( F_2_IBUF )
LUT6:I1->O 6 0.203 0.973 Mmux_Y_sig31 ( Y_sig<1> )
LUT5:I2->O 4 0.205 1.028 U1/C<3>2 ( U1/C<3> )
LUT6:I1->O 1 0.203 0.000 U1/C<6>_G ( N16 )
MUXF7:I1->O 5 0.140 0.943 U1/C<6> ( U1/C<6> )
LUT5:I2->O 3 0.205 1.015 U1/Mxor_S_sig<7>_xo<0>1 ( S_temporary<7> )
LUT6:I0->O 1 0.203 0.579 Mmux_Negative1 ( Negative_OBUF )
OBUF:I->O 2.571 Negative_OBUF ( Negative )
--      --      --      --      --      --      --      --      --
--      --      --      --      --      --      --      --      --
Total 11.168ns ( 4.952ns logic, 6.216ns route )
( 44.3% logic, 55.7% route )

=====

Cross Clock Domains Report:
--      --      --      --      --      --      --      --      --
--      --      --      --      --      --      --      --      --
=====

Total REAL time to Xst completion: 10.00 secs
Total CPU time to Xst completion: 10.03 secs

```

-- >

Total memory usage is 4487500 kilobytes

Number of errors : 0 (0 filtered)

Number of warnings : 0 (0 filtered)

Number of infos : 0 (0 filtered)

64200288>fuse -incremental -o alu_cla_tb_isim_beh.exe -prj alu_cla_tb.prj -top alu_cla_tb

Running: \unwrapped\fuse.exe -incremental -o alu_cla_tb_isim_beh.exe -prj alu_cla_tb.prj -top alu_cla_tb

ISim P.20131013 (signature 0x7708f090)

Number of CPUs detected in this system: 8

Turning on mult-threading, number of parallel sub-compilation jobs: 16

Determining compilation order of HDL files

Parsing VHDL file "cla_gp.vhd" into library work

Parsing VHDL file "cla_add_n_bit.vhd" into library work

Parsing VHDL file "alu_cla.vhd" into library work

Parsing VHDL file "alu_cla_tb_IDEAL.vhd" into library work

Starting static elaboration

Completed static elaboration

Compiling package standard

Compiling package std_logic_1164

Compiling package textio

Compiling package std_logic_textio

Compiling package numeric_std

Compiling package attributes

Compiling package std_logic_misc

Compiling architecture ndv of entity cla_add_n_bit [\cla_add_n_bit(8)\]

Compiling architecture ndv of entity alu_cla [\alu_cla(8)\]

Compiling architecture testbench_arch of entity alu_cla_tb

Time Resolution for simulation is 1ps.

Waiting for 1 sub-compilation(s) to finish...

Compiled 12 VHDL Units

Built simulation executable alu_cla_tb_isim_beh.exe

Fuse Memory Usage: 37804 KB

Fuse CPU Usage: 905 ms

64200288>alu_cla_tb_isim_beh.exe -tclbatch isim.tcl -wdb alu_cla_tb_isim_beh.wdb

ISim P.20131013 (signature 0x7708f090)

WARNING: A WEBPACK license was found.

WARNING: Please use Xilinx License Configuration Manager to check out a full ISim license.

WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for more information on the differences between the Lite and the Full version.

This is a Lite version of ISim.

Time resolution is 1 ps

Simulator is doing circuit initialization process.

Finished circuit initialization process.

at 7864320 ns, Instance /alu_cla_tb/ : Warning: NUMERIC_STD.TO_UNSIGNED: vector truncated

at 8847360 ns, Instance /alu_cla_tb/ : Warning: NUMERIC_STD.TO_UNSIGNED: vector truncated

at 9830400 ns, Instance /alu_cla_tb/ : Warning: NUMERIC_STD.TO_UNSIGNED: vector truncated

at 10813440 ns, Instance /alu_cla_tb/ : Warning: NUMERIC_STD.TO_UNSIGNED: vector truncated

at 11796480 ns, Instance /alu_cla_tb/ : Warning: NUMERIC_STD.TO_UNSIGNED: vector truncated
at 12779520 ns, Instance /alu_cla_tb/ : Warning: NUMERIC_STD.TO_UNSIGNED: vector truncated
at 13762560 ns, Instance /alu_cla_tb/ : Warning: NUMERIC_STD.TO_UNSIGNED: vector truncated
at 14745600 ns, Instance /alu_cla_tb/ : Warning: NUMERIC_STD.TO_UNSIGNED: vector truncated

64200288>rem ***** test alu flags

64200288>xst -ifn alu_cla_flags.xst
Release 14.7 - xst P.20131013 (nt64)
Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.
-- > Parameter TMPDIR set to xst/projnav.tmp

Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.23 secs

-- > Parameter xsthdpdir set to xst

Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.24 secs

-- >

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=====
* Synthesis Options Summary *

=====

-- -- Source Parameters

Input File Name : "alu_cla_flags_tb.prj"
Ignore Synthesis Constraint File : NO

-- -- Target Parameters

Output File Name : "alu_cla_flags_tb"
Output Format : NGC
Target Device : xc6slx4-3-tqg144

-- -- Source Options

Top Module Name : alu_cla_flags_tb
Automatic FSM Extraction : YES
FSM Encoding Algorithm : Auto
Safe Implementation : No
FSM Style : LUT
RAM Extraction : Yes
RAM Style : Auto
ROM Extraction : Yes
Shift Register Extraction : YES
ROM Style : Auto
Resource Sharing : YES
Asynchronous To Synchronous : NO
Shift Register Minimum Size : 2
Use DSP Block : Auto
Automatic Register Balancing : No

-- -- Target Options

LUT Combining : Auto
Reduce Control Sets : Auto
Add IO Buffers : YES
Global Maximum Fanout : 100000
Add Generic Clock Buffer(BUFG) : 16
Register Duplication : YES
Optimize Instantiated Primitives : NO
Use Clock Enable : Auto
Use Synchronous Set : Auto
Use Synchronous Reset : Auto
Pack IO Registers into IOBs : Auto
Equivalent register Removal : YES

-- -- General Options

Optimization Goal : Speed
Optimization Effort : 1
Power Reduction : NO
Keep Hierarchy : No
Netlist Hierarchy : As_Optimized
RTL Output : Yes
Global Optimization : AllClockNets
Read Cores : YES
Write Timing Constraints : NO
Cross Clock Analysis : NO
Hierarchy Separator : /
Bus Delimiter : <>
Case Specifier : Maintain
Slice Utilization Ratio : 100
BRAM Utilization Ratio : 100
DSP48 Utilization Ratio : 100
Auto BRAM Packing : NO
Slice Utilization Ratio Delta : 5

=====

=====

* HDL Parsing *

=====

Parsing VHDL file "64200288\cla_gp.vhd" into library work
Parsing entity <cla_gp>.
Parsing architecture <ideal> of entity <cla_gp>.
Parsing VHDL file "64200288\cla_add_n_bit.vhd" into library work

```

Parsing entity <cla_add_n_bit>.
Parsing architecture <NDV> of entity <cla_add_n_bit>.
Parsing VHDL file "64200288\alu_cla.vhd" into library work
Parsing entity <alu_cla>.
Parsing architecture <NDV> of entity <alu_cla>.
Parsing VHDL file "64200288\alu_cla_tb_FLAGS_IDEAL.vhd" into library work
Parsing entity <alu_cla_flags_tb>.
Parsing architecture <test_alu_flags> of entity <alu_cla_flags_tb>.

=====
* HDL Elaboration *
=====

Elaborating entity <alu_cla_flags_tb> ( architecture <test_alu_flags> ) with
generics from library <work>.

Elaborating entity <alu_cla> ( architecture <NDV> ) with generics from library
<work>.

Elaborating entity <cla_add_n_bit> ( architecture <NDV> ) with generics from
library <work>.
ERROR:HDLCompiler:890 - "64200288\alu_cla_tb_FLAGS_IDEAL.vhd" Line 144: wait
statement without UNTIL clause not supported for synthesis
Netlist alu_cla_flags_tb( 8 )( test_alu_flags ) remains a blackbox, due to errors
in its contents
-- >

Total memory usage is 4466680 kilobytes

Number of errors : 1 ( 0 filtered )
Number of warnings : 0 ( 0 filtered )
Number of infos : 0 ( 0 filtered )

64200288>fuse -incremental -o alu_cla_flags_tb_isim_beh.exe -prj
alu_cla_flags_tb.prj -top alu_cla_flags_tb
Running: \unwrapped\fuse.exe -incremental -o alu_cla_flags_tb_isim_beh.exe -prj
alu_cla_flags_tb.prj -top alu_cla_flags_tb
ISim P.20131013 ( signature 0x7708f090 )
Number of CPUs detected in this system: 8
Turning on mult-threading, number of parallel sub-compilation jobs: 16
Determining compilation order of HDL files
Parsing VHDL file "cla_gp.vhd" into library work
Parsing VHDL file "cla_add_n_bit.vhd" into library work
Parsing VHDL file "alu_cla.vhd" into library work
Parsing VHDL file "alu_cla_tb_FLAGS_IDEAL.vhd" into library work
Starting static elaboration
Completed static elaboration
Compiling package standard
Compiling package std_logic_1164
Compiling package textio
Compiling package std_logic_textio
Compiling package numeric_std
Compiling package attributes
Compiling package std_logic_misc
Compiling architecture ndv of entity cla_add_n_bit [\cla_add_n_bit( 8 )\]
Compiling architecture ndv of entity alu_cla [\alu_cla( 8 )\]
Compiling architecture test_alu_flags of entity alu_cla_flags_tb
Time Resolution for simulation is 1ps.
Waiting for 1 sub-compilation( s ) to finish...

```

Compiled 12 VHDL Units
Built simulation executable alu_cla_flags_tb_isim_beh.exe
Fuse Memory Usage: 37548 KB
Fuse CPU Usage: 1077 ms

```
64200288>alu_cla_flags_tb_isim_beh.exe -tclbatch isim.tcl -wdb
alu_cla_flags_tb_isim_beh.wdb
ISim P.20131013 ( signature 0x7708f090 )
WARNING: A WEBPACK license was found.
WARNING: Please use Xilinx License Configuration Manager to check out a full ISim
license.
WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for
more information on the differences between the Lite and the Full version.
This is a Lite version of ISim.
Time resolution is 1 ps
Simulator is doing circuit initialization process.
Finished circuit initialization process.
```

```
-- *****
-- **** STUDENT: 64200296
-- *****
-- KOMENTARJI K OCENI NALOGE
-- Matej Možek: Ni pripomb
-- *****
```

```
64200296>rem ***** test cla adder
```

```
64200296>if not exist "xst" mkdir xst
```

```
64200296>cd XST
```

```
64200296\xst>if not exist "projnav.tmp" mkdir "projnav.tmp"
```

```
64200296\xst>cd ..
```

```
64200296>rem ***** test cla operations
```

```
64200296>xst -ifn cla_add_n_bit.xst
Release 14.7 - xst P.20131013 ( nt64 )
Copyright ( c ) 1995-2013 Xilinx, Inc. All rights reserved.
-- > Parameter TMPDIR set to xst/projnav.tmp
```

```
Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.24 secs
```

```
-- > Parameter xsthdpdir set to xst
```

```
Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.24 secs
```

```
-- >
```

```
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```
=====
* Synthesis Options Summary *
```

```
=====
-- -- Source Parameters
```

```
Input File Name : "cla_add_n_bit.prj"
```


Ignore Synthesis Constraint File : NO

-- -- Target Parameters

Output File Name : "cla_add_n_bit"

Output Format : NGC

Target Device : xc6slx4-3-tqg144

-- -- Source Options

Top Module Name : cla_add_n_bit

Automatic FSM Extraction : YES

FSM Encoding Algorithm : Auto

Safe Implementation : No

FSM Style : LUT

RAM Extraction : Yes

RAM Style : Auto

ROM Extraction : Yes

Shift Register Extraction : YES

ROM Style : Auto

Resource Sharing : YES

Asynchronous To Synchronous : NO

Shift Register Minimum Size : 2

Use DSP Block : Auto

Automatic Register Balancing : No

-- -- Target Options

LUT Combining : Auto

Reduce Control Sets : Auto

Add IO Buffers : YES

Global Maximum Fanout : 100000

Add Generic Clock Buffer(BUFG) : 16

Register Duplication : YES

Optimize Instantiated Primitives : NO

Use Clock Enable : Auto

Use Synchronous Set : Auto

Use Synchronous Reset : Auto

Pack IO Registers into IOBs : Auto

Equivalent register Removal : YES

-- -- General Options

Optimization Goal : Speed

Optimization Effort : 1

Power Reduction : NO

Keep Hierarchy : No

Netlist Hierarchy : As_Optimized

RTL Output : Yes

Global Optimization : AllClockNets

Read Cores : YES

Write Timing Constraints : NO

Cross Clock Analysis : NO

Hierarchy Separator : /

Bus Delimiter : <>

Case Specifier : Maintain

Slice Utilization Ratio : 100

BRAM Utilization Ratio : 100

DSP48 Utilization Ratio : 100

Auto BRAM Packing : NO

Slice Utilization Ratio Delta : 5

=====

```

=====
* HDL Parsing *
=====
Parsing VHDL file "64200296\cla_gp.vhd" into library work
Parsing entity <cla_gp>.
Parsing architecture <ideal> of entity <cla_gp>.
Parsing VHDL file "64200296\cla_add_n_bit.vhd" into library work
Parsing entity <cla_add_n_bit>.
Parsing architecture <NDV> of entity <cla_add_n_bit>.

=====
* HDL Elaboration *
=====

Elaborating entity <cla_add_n_bit> ( architecture <NDV> ) with generics from
library <work>.

=====
* HDL Synthesis *
=====

Synthesizing Unit <cla_add_n_bit>.
Related source file is "64200296\cla_add_n_bit.vhd".
n = 8
Summary:
Unit <cla_add_n_bit> synthesized.

=====
HDL Synthesis Report

Macro Statistics
# Xors : 16
1-bit xor2 : 16

=====

=====
* Advanced HDL Synthesis *
=====

=====
Advanced HDL Synthesis Report

Macro Statistics
# Xors : 16
1-bit xor2 : 16

=====

=====
* Low Level Synthesis *
=====

Optimizing unit <cla_add_n_bit> ...

Mapping all equations...
Building and optimizing final netlist ...

```

Found area constraint ratio of 100 (+ 5) on block cla_add_n_bit, actual ratio is 1.

Final Macro Processing ...

=====
Final Register Report

Found no macro

=====
* Partition Report *
=====

Partition Implementation Status

-- -- -- -- -- -- -- -- -- -- -- -- -- --
-- -- -

No Partitions were found in this design.

-- -- -- -- -- -- -- -- -- -- -- -- -- --
-- -- -

=====
* Design Summary *
=====

Top Level Output File Name : cla_add_n_bit.ngc

Primitive and Black Box Usage:

-- -- -- -- -- -- -- -- -- -- -- -- -- --
-- -- -

BELS : 24
LUT2 : 6
LUT3 : 3
LUT5 : 6
LUT6 : 9
IO Buffers : 28
IBUF : 17
OBUF : 11

Device utilization summary:

-- -- -- -- -- -- -- -- -- -- -- -- -- --
-

Selected Device : 6slx4tqg144-3

Slice Logic Utilization:

Number of Slice LUTs: 24 out of 2400 1%
Number used as Logic: 24 out of 2400 1%

Slice Logic Distribution:

Number of LUT Flip Flop pairs used: 24
Number with an unused Flip Flop: 24 out of 24 100%
Number with an unused LUT: 0 out of 24 0%
Number of fully used LUT-FF pairs: 0 out of 24 0%
Number of unique control sets: 0

IO Utilization:

Number of IOs: 28

Number of bonded IOBs: 28 out of 102 27%

Specific Feature Utilization:

```
-- -- -- -- -- -- -- -- -- -- -- -- -- --
-
```

Partition Resource Summary:

```
-- -- -- -- -- -- -- -- -- -- -- -- -- --
-
```

No Partitions were found in this design.

```
-- -- -- -- -- -- -- -- -- -- -- -- -- --
-
```

=====
Timing Report

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.

FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT
GENERATED AFTER PLACE-and-ROUTE.

Clock Information:

```
-- -- -- -- -- -- -- -- -- -- -- -- -- --
```

No clock signals found in this design

Asynchronous Control Signals Information:

```
-- -- -- -- -- -- -- -- -- -- -- -- -- --
-- -- -- -- -- -- -- -- -- -- -- -- -- --
```

No asynchronous control signals found in this design

Timing Summary:

```
-- -- -- -- -- -- -- -- -- -- -- -- -- --
```

Speed Grade: -3

Minimum period: No path found

Minimum input arrival time before clock: No path found

Maximum output required time after clock: No path found

Maximum combinational path delay: 9.101ns

Timing Details:

```
-- -- -- -- -- -- -- -- -- -- -- -- -- --
```

All values displayed in nanoseconds (ns)

=====
Timing constraint: Default path analysis

Total number of paths / destination ports: 131 / 11

```
-- -- -- -- -- -- -- -- -- -- -- -- -- --
-- -- -- -- -- -- -- -- -- -- -- -- -- --
-- -- -- -- -- -- -- -- -- -- -- -- -- --
```

Delay: 9.101ns (Levels of Logic = 7)

Source: Y<0> (PAD)

Destination: S<7> (PAD)

Data Path: Y<0> to S<7>

Gate Net

Cell:in->out fanout Delay Delay Logical Name (Net Name)

```

--      --      --      --      --      --      --      --      --      --      --
--      --      --      --      --      --      --      --      --      --      --
--      --
IBUF:I->0 6 1.222 0.973 Y_0_IBUF ( Y_0_IBUF )
LUT3:I0->0 2 0.205 0.617 c<3>_SW0 ( N2 )
LUT5:I4->0 3 0.205 0.651 c<3> ( c<3> )
LUT3:I2->0 2 0.205 0.617 c<6>_SW0 ( N4 )
LUT5:I4->0 2 0.205 0.845 c<6> ( c<6> )
LUT5:I2->0 1 0.205 0.579 Mxor_s_sig<7>_xo<0>1 ( S_7_OBUF )
OBUF:I->0 2.571 S_7_OBUF ( S<7> )
--      --      --      --      --      --      --      --      --      --      --
--      --      --      --      --      --      --      --      --      --      --
Total 9.101ns ( 4.818ns logic, 4.283ns route )
( 52.9% logic, 47.1% route )

```

Cross Clock Domains Report:

```

Total REAL time to Xst completion: 9.00 secs
Total CPU time to Xst completion: 8.99 secs

```

```
-- >
```

Total memory usage is 4487500 kilobytes

Number of errors : 0 (0 filtered)

Number of warnings : 0 (0 filtered)

Number of infos : 0 (0 filtered)

```

64200296>fuse -incremental -o cla_add_n_bit_tb_isim_beh.exe -prj
cla_add_n_bit_tb.prj -top cla_add_n_bit_tb
Running: \unwrapped\fuse.exe -incremental -o cla_add_n_bit_tb_isim_beh.exe -prj
cla_add_n_bit_tb.prj -top cla_add_n_bit_tb
ISim P.20131013 ( signature 0x7708f090 )
Number of CPUs detected in this system: 8
Turning on mult-threading, number of parallel sub-compilation jobs: 16
Determining compilation order of HDL files
Parsing VHDL file "cla_gp.vhd" into library work
Parsing VHDL file "cla_add_n_bit.vhd" into library work
Parsing VHDL file "cla_add_n_bit_tb_IDEAL.vhd" into library work
Starting static elaboration
Completed static elaboration
Compiling package standard
Compiling package std_logic_1164
Compiling package textio
Compiling package std_logic_textio
Compiling package numeric_std
Compiling package attributes
Compiling package std_logic_misc
Compiling architecture ndv of entity cla_add_n_bit [\cla_add_n_bit( 8 )\]
Compiling architecture testbench_arch of entity cla_add_n_bit_tb
Time Resolution for simulation is 1ps.
Compiled 10 VHDL Units
Built simulation executable cla_add_n_bit_tb_isim_beh.exe
Fuse Memory Usage: 37376 KB

```

Fuse CPU Usage: 874 ms

```
64200296>cla_add_n_bit_tb_isim_beh.exe -tclbatch isim.tcl -wdb
cla_add_n_bit_tb_isim_beh.wdb
ISim P.20131013 ( signature 0x7708f090 )
WARNING: A WEBPACK license was found.
WARNING: Please use Xilinx License Configuration Manager to check out a full ISim
license.
WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for
more information on the differences between the Lite and the Full version.
This is a Lite version of ISim.
Time resolution is 1 ps
Simulator is doing circuit initialization process.
Finished circuit initialization process.
```

```
64200296>rem ***** test cla flags
```

```
64200296>xst -ifn cla_add_n_bit_flags.xst
Release 14.7 - xst P.20131013 ( nt64 )
Copyright ( c ) 1995-2013 Xilinx, Inc. All rights reserved.
-- > Parameter TMPDIR set to xst/projnav.tmp
```

```
Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.23 secs
```

```
-- > Parameter xsthdpdir set to xst
```

```
Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.23 secs
```

```
-- > ERROR:Xst:438 - Can not open file : cla_add_n_bit_flags.prj
```

```
Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.25 secs
```

```
-- >
```

Total memory usage is 4422880 kilobytes

Number of errors : 1 (0 filtered)

Number of warnings : 0 (0 filtered)

Number of infos : 0 (0 filtered)

```
64200296>fuse -incremental -o cla_add_n_bit_tb_flags_isim_beh.exe -prj
cla_add_n_bit_flags_tb.prj -top cla_add_n_bit_flags_tb_IDEAL
Running: \unwrapped\fuse.exe -incremental -o cla_add_n_bit_tb_flags_isim_beh.exe -
prj cla_add_n_bit_flags_tb.prj -top cla_add_n_bit_flags_tb_IDEAL
ISim P.20131013 ( signature 0x7708f090 )
Number of CPUs detected in this system: 8
Turning on mult-threading, number of parallel sub-compilation jobs: 16
Determining compilation order of HDL files
Parsing VHDL file "cla_gp.vhd" into library work
Parsing VHDL file "cla_add_n_bit.vhd" into library work
Parsing VHDL file "cla_add_n_bit_flags_tb_IDEAL.vhd" into library work
Starting static elaboration
Completed static elaboration
Compiling package standard
Compiling package std_logic_1164
Compiling package textio
```

```

Compiling package std_logic_textio
Compiling package numeric_std
Compiling package attributes
Compiling package std_logic_misc
Compiling architecture ndv of entity cla_add_n_bit [\cla_add_n_bit( 8 )\]
Compiling architecture a1 of entity cla_add_n_bit_flags_tb_ideal
Time Resolution for simulation is 1ps.
Waiting for 1 sub-compilation( s ) to finish...
Compiled 10 VHDL Units
Built simulation executable cla_add_n_bit_tb_flags_isim_beh.exe
Fuse Memory Usage: 37344 KB
Fuse CPU Usage: 905 ms

64200296>cla_add_n_bit_tb_flags_isim_beh.exe -tclbatch isim.tcl -wdb
cla_add_n_bit_flags_tb.wdb
ISim P.20131013 ( signature 0x7708f090 )
WARNING: A WEBPACK license was found.
WARNING: Please use Xilinx License Configuration Manager to check out a full ISim
license.
WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for
more information on the differences between the Lite and the Full version.
This is a Lite version of ISim.
Time resolution is 1 ps
Simulator is doing circuit initialization process.
Finished circuit initialization process.

64200296>rem ***** test alu operations

64200296>xst -ifn alu_cla.xst
Release 14.7 - xst P.20131013 ( nt64 )
Copyright ( c ) 1995-2013 Xilinx, Inc. All rights reserved.
-- > Parameter TMPDIR set to xst/projnav.tmp

Total REAL time to Xst completion: 1.00 secs
Total CPU time to Xst completion: 0.25 secs

-- > Parameter xsthdpdir set to xst

Total REAL time to Xst completion: 1.00 secs
Total CPU time to Xst completion: 0.26 secs

-- >
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```

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- 8.4.5) Cross Clock Domains [Report](#)

```
=====
* Synthesis Options Summary *
=====
```

```
--      -- Source Parameters
```

```
Input File Name : "alu_cla.prj"
```

```
Ignore Synthesis Constraint File : NO
```

```
--      -- Target Parameters
```

```
Output File Name : "alu_cla"
```

```
Output Format : NGC
```

```
Target Device : xc6slx4-3-tqg144
```

```
--      -- Source Options
```

```
Top Module Name : alu_cla
```

```
Automatic FSM Extraction : YES
```

```
FSM Encoding Algorithm : Auto
```

```
Safe Implementation : No
```

```
FSM Style : LUT
```

```
RAM Extraction : Yes
```

```
RAM Style : Auto
```

```
ROM Extraction : Yes
```

```
Shift Register Extraction : YES
```

```
ROM Style : Auto
```

```
Resource Sharing : YES
```

```
Asynchronous To Synchronous : NO
```

```
Shift Register Minimum Size : 2
```

```
Use DSP Block : Auto
```

```
Automatic Register Balancing : No
```

```
--      -- Target Options
```

```
LUT Combining : Auto
```

```
Reduce Control Sets : Auto
```

```
Add IO Buffers : YES
```

```
Global Maximum Fanout : 100000
```

```
Add Generic Clock Buffer( BUFG ) : 16
```

```
Register Duplication : YES
```

```
Optimize Instantiated Primitives : NO
```

```
Use Clock Enable : Auto
```

```
Use Synchronous Set : Auto
```

```
Use Synchronous Reset : Auto
```

```
Pack IO Registers into IOBs : Auto
```

```
Equivalent register Removal : YES
```

```
--      -- General Options
```

```
Optimization Goal : Speed
```

```
Optimization Effort : 1
```

```
Power Reduction : NO
```

```
Keep Hierarchy : No
```

```
Netlist Hierarchy : As_Optimized
```

```
RTL Output : Yes
```

```
Global Optimization : AllClockNets
```

```
Read Cores : YES
```

```
Write Timing Constraints : NO
```

```
Cross Clock Analysis : NO
```

```
Hierarchy Separator : /
```


Bus Delimiter : <>
Case Specifier : Maintain
Slice Utilization Ratio : 100
BRAM Utilization Ratio : 100
DSP48 Utilization Ratio : 100
Auto BRAM Packing : NO
Slice Utilization Ratio Delta : 5

=====

=====

* HDL Parsing *

=====

Parsing VHDL file "64200296\cla_gp.vhd" into library work
Parsing entity <cla_gp>.
Parsing architecture <ideal> of entity <cla_gp>.
Parsing VHDL file "64200296\cla_add_n_bit.vhd" into library work
Parsing entity <cla_add_n_bit>.
Parsing architecture <NDV> of entity <cla_add_n_bit>.
Parsing VHDL file "64200296\alu_cla.vhd" into library work
Parsing entity <alu_cla>.
Parsing architecture <NDV> of entity <alu_cla>.

=====

* HDL Elaboration *

=====

Elaborating entity <alu_cla> (architecture <NDV>) with generics from library <work>.

Elaborating entity <cla_add_n_bit> (architecture <NDV>) with generics from library <work>.

=====

* HDL Synthesis *

=====

Synthesizing Unit <alu_cla>.
Related source file is "64200296\alu_cla.vhd".
n = 8
Found 8-bit 12-to-1 multiplexer for signal <S> created at line 40.
Summary:
inferred 7 Multiplexer(s).
Unit <alu_cla> synthesized.

Synthesizing Unit <cla_add_n_bit>.
Related source file is "64200296\cla_add_n_bit.vhd".
n = 8
Summary:
Unit <cla_add_n_bit> synthesized.

=====

HDL Synthesis Report

Macro Statistics

Multiplexers : 7
8-bit 12-to-1 multiplexer : 1
8-bit 2-to-1 multiplexer : 6
Xors : 17

1-bit xor2 : 16
8-bit xor2 : 1

=====

=====

* Advanced HDL Synthesis *

=====

=====

Advanced HDL Synthesis Report

Macro Statistics

Multiplexers : 7

8-bit 12-to-1 multiplexer : 1

8-bit 2-to-1 multiplexer : 6

Xors : 17

1-bit xor2 : 16

8-bit xor2 : 1

=====

=====

* Low Level Synthesis *

=====

Optimizing unit <alu_cla> ...

Optimizing unit <cla_add_n_bit> ...

Mapping all equations...

Building and optimizing final netlist ...

Found area constraint ratio of 100 (+ 5) on block alu_cla, actual ratio is 3.

Final Macro Processing ...

=====

Final Register Report

Found no macro

=====

=====

* Partition Report *

=====

Partition Implementation Status

-- -- -- -- -- -- -- -- -- -- -- --
-- -- --

No Partitions were found in this design.

-- -- -- -- -- -- -- -- -- -- -- --
-- -- --

=====

* Design Summary *

=====

Primitive and Black Box Usage:

```
# BELS : 49
# LUT3 : 2
# LUT5 : 15
# LUT6 : 30
# MUXF7 : 2
# IO Buffers : 34
# IBUF : 20
# OBUF : 14
```

Selected Device : 6slx4tqg144-3

Number of Slice LUTs: 47 out of 2400 1%
Number used as Logic: 47 out of 2400 1%

```

Number of LUT Flip Flop pairs used: 47
Number with an unused Flip Flop: 47 out of 47 100%
Number with an unused LUT: 0 out of 47 0%
Number of fully used LUT-FF pairs: 0 out of 47 0%
Number of unique control sets: 0

```

Number of IOs: 34
Number of bonded IOBs: 34 out of 102 33%

Partition Resource Summary:

No Partitions were found in this design.

=====

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.
FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT
GENERATED AFTER PLACE-and-ROUTE.

No clock signals found in this design

Asynchronous Control Signals Information:

```
-- -- -- -- -- -- -- -- -- -- -- -- -- --
-- -- -- -- -- -- -- -- -- -- -- -- -- --
```

No asynchronous control signals found in this design

Timing Summary:

```
-- -- -- -- -- -- -- -- -- -- -- -- -- --
Speed Grade: -3
```

Minimum period: No path found

Minimum input arrival time before clock: No path found

Maximum output required time after clock: No path found

Maximum combinational path delay: 12.446ns

Timing Details:

```
-- -- -- -- -- -- -- -- -- -- -- -- -- --
All values displayed in nanoseconds ( ns )
```

Timing constraint: Default path analysis

Total number of paths / destination ports: 902 / 14

```
-- -- -- -- -- -- -- -- -- -- -- -- -- --
-- -- -- -- -- -- -- -- -- -- -- -- -- --
-- -- -- -- -- -- -- -- -- -- -- -- -- --
```

Delay: 12.446ns (Levels of Logic = 9)

Source: F<2> (PAD)

Destination: Zero (PAD)

Data Path: F<2> to Zero

Gate Net

Cell:in->out fanout Delay Delay Logical Name (Net Name)

```
-- -- -- -- -- -- -- -- -- -- -- -- -- --
-- -- -- -- -- -- -- -- -- -- -- -- -- --
-- -- -- -- -- -- -- -- -- -- -- -- -- --
```

IBUF:I->O 30 1.222 1.608 F_2_IBUF (F_2_IBUF)

LUT6:I1->O 5 0.203 0.943 Mmux_sig_y31 (sig_y<1>)

LUT5:I2->O 4 0.205 0.684 U1/c<3>2 (U1/c<3>)

LUT3:I2->O 1 0.205 0.580 U1/c<6>_SW2 (N11)

LUT5:I4->O 4 0.205 0.912 U1/c<6> (U1/c<6>)

LUT5:I2->O 1 0.205 0.924 U1/Mxor_s_sig<7>_xo<0>1 (sig_s<7>)

LUT6:I1->O 3 0.203 0.995 Mmux_S22 (Negative_OBUF)

LUT6:I1->O 1 0.203 0.579 Zero (Zero_OBUF)

OBUF:I->O 2.571 Zero_OBUF (Zero)

```
-- -- -- -- -- -- -- -- -- -- -- -- -- --
-- -- -- -- -- -- -- -- -- -- -- -- -- --
```

Total 12.446ns (5.222ns logic, 7.224ns route)

(42.0% logic, 58.0% route)

Cross Clock Domains Report:

```
-- -- -- -- -- -- -- -- -- -- -- -- -- --
-- -- -- -- -- -- -- -- -- -- -- -- -- --
```

Total REAL time to Xst completion: 10.00 secs

Total CPU time to Xst completion: 9.40 secs

-- >

Total memory usage is 4487500 kilobytes

Number of errors : 0 (0 filtered)

Number of warnings : 0 (0 filtered)

Number of infos : 0 (0 filtered)

64200296>fuse -incremental -o alu_cla_tb_isim_beh.exe -prj alu_cla_tb.prj -top alu_cla_tb

Running: \unwrapped\fuse.exe -incremental -o alu_cla_tb_isim_beh.exe -prj alu_cla_tb.prj -top alu_cla_tb

ISim P.20131013 (signature 0x7708f090)

Number of CPUs detected in this system: 8

Turning on mult-threading, number of parallel sub-compilation jobs: 16

Determining compilation order of HDL files

Parsing VHDL file "cla_gp.vhd" into library work

Parsing VHDL file "cla_add_n_bit.vhd" into library work

Parsing VHDL file "alu_cla.vhd" into library work

Parsing VHDL file "alu_cla_tb_IDEAL.vhd" into library work

Starting static elaboration

Completed static elaboration

Compiling package standard

Compiling package std_logic_1164

Compiling package textio

Compiling package std_logic_textio

Compiling package numeric_std

Compiling package attributes

Compiling package std_logic_misc

Compiling architecture ndv of entity cla_add_n_bit [\cla_add_n_bit(8)\]

Compiling architecture ndv of entity alu_cla [\alu_cla(8)\]

Compiling architecture testbench_arch of entity alu_cla_tb

Time Resolution for simulation is 1ps.

Waiting for 1 sub-compilation(s) to finish...

Compiled 12 VHDL Units

Built simulation executable alu_cla_tb_isim_beh.exe

Fuse Memory Usage: 37600 KB

Fuse CPU Usage: 983 ms

64200296>alu_cla_tb_isim_beh.exe -tclbatch isim.tcl -wdb alu_cla_tb_isim_beh.wdb

ISim P.20131013 (signature 0x7708f090)

WARNING: A WEBPACK license was found.

WARNING: Please use Xilinx License Configuration Manager to check out a full ISim license.

WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for more information on the differences between the Lite and the Full version.

This is a Lite version of ISim.

Time resolution is 1 ps

Simulator is doing circuit initialization process.

Finished circuit initialization process.

at 7864320 ns, Instance /alu_cla_tb/ : Warning: NUMERIC_STD.TO_UNSIGNED: vector truncated

at 8847360 ns, Instance /alu_cla_tb/ : Warning: NUMERIC_STD.TO_UNSIGNED: vector truncated

at 9830400 ns, Instance /alu_cla_tb/ : Warning: NUMERIC_STD.TO_UNSIGNED: vector truncated

at 10813440 ns, Instance /alu_cla_tb/ : Warning: NUMERIC_STD.TO_UNSIGNED: vector truncated

at 11796480 ns, Instance /alu_cla_tb/ : Warning: NUMERIC_STD.TO_UNSIGNED: vector truncated

at 12779520 ns, Instance /alu_cla_tb/ : Warning: NUMERIC_STD.TO_UNSIGNED: vector truncated
at 13762560 ns, Instance /alu_cla_tb/ : Warning: NUMERIC_STD.TO_UNSIGNED: vector truncated
at 14745600 ns, Instance /alu_cla_tb/ : Warning: NUMERIC_STD.TO_UNSIGNED: vector truncated

64200296>rem ***** test alu flags

64200296>xst -ifn alu_cla_flags.xst
Release 14.7 - xst P.20131013 (nt64)
Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.
-- > Parameter TMPDIR set to xst/projnav.tmp

Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.25 secs

-- > Parameter xsthdpdir set to xst

Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.25 secs

-- >

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 - 8.4.5) Cross Clock Domains Report

=====
* Synthesis Options Summary *

-- -- Source Parameters

Input File Name : "alu_cla_flags_tb.prj"
Ignore Synthesis Constraint File : NO

-- -- Target Parameters

Output File Name : "alu_cla_flags_tb"
Output Format : NGC
Target Device : xc6slx4-3-tqg144

-- -- Source Options

Top Module Name : alu_cla_flags_tb
Automatic FSM Extraction : YES

FSM Encoding Algorithm : Auto
Safe Implementation : No
FSM Style : LUT
RAM Extraction : Yes
RAM Style : Auto
ROM Extraction : Yes
Shift Register Extraction : YES
ROM Style : Auto
Resource Sharing : YES
Asynchronous To Synchronous : NO
Shift Register Minimum Size : 2
Use DSP Block : Auto
Automatic Register Balancing : No

-- -- Target Options

LUT Combining : Auto
Reduce Control Sets : Auto
Add IO Buffers : YES
Global Maximum Fanout : 100000
Add Generic Clock Buffer(BUFG) : 16
Register Duplication : YES
Optimize Instantiated Primitives : NO
Use Clock Enable : Auto
Use Synchronous Set : Auto
Use Synchronous Reset : Auto
Pack IO Registers into IOBs : Auto
Equivalent register Removal : YES

-- -- General Options

Optimization Goal : Speed
Optimization Effort : 1
Power Reduction : NO
Keep Hierarchy : No
Netlist Hierarchy : As_Optimized
RTL Output : Yes
Global Optimization : AllClockNets
Read Cores : YES
Write Timing Constraints : NO
Cross Clock Analysis : NO
Hierarchy Separator : /
Bus Delimiter : <>
Case Specifier : Maintain
Slice Utilization Ratio : 100
BRAM Utilization Ratio : 100
DSP48 Utilization Ratio : 100
Auto BRAM Packing : NO
Slice Utilization Ratio Delta : 5

=====

=====

* HDL Parsing *

=====

Parsing VHDL file "64200296\cla_gp.vhd" into library work
Parsing entity <cla_gp>.
Parsing architecture <ideal> of entity <cla_gp>.
Parsing VHDL file "64200296\cla_add_n_bit.vhd" into library work
Parsing entity <cla_add_n_bit>.
Parsing architecture <NDV> of entity <cla_add_n_bit>.

```

Parsing VHDL file "64200296\alu_cla.vhd" into library work
Parsing entity <alu_cla>.
Parsing architecture <NDV> of entity <alu_cla>.
Parsing VHDL file "64200296\alu_cla_tb_FLAGS_IDEAL.vhd" into library work
Parsing entity <alu_cla_flags_tb>.
Parsing architecture <test_alu_flags> of entity <alu_cla_flags_tb>.

=====
* HDL Elaboration *
=====

Elaborating entity <alu_cla_flags_tb> ( architecture <test_alu_flags> ) with
generics from library <work>.

Elaborating entity <alu_cla> ( architecture <NDV> ) with generics from library
<work>.

Elaborating entity <cla_add_n_bit> ( architecture <NDV> ) with generics from
library <work>.
ERROR:HDLCompiler:890 - "64200296\alu_cla_tb_FLAGS_IDEAL.vhd" Line 144: wait
statement without UNTIL clause not supported for synthesis
Netlist alu_cla_flags_tb( 8 )( test_alu_flags ) remains a blackbox, due to errors
in its contents
-- >

Total memory usage is 4466680 kilobytes

Number of errors : 1 ( 0 filtered )
Number of warnings : 0 ( 0 filtered )
Number of infos : 0 ( 0 filtered )

64200296>fuse -incremental -o alu_cla_flags_tb_isim_beh.exe -prj
alu_cla_flags_tb.prj -top alu_cla_flags_tb
Running: \unwrapped\fuse.exe -incremental -o alu_cla_flags_tb_isim_beh.exe -prj
alu_cla_flags_tb.prj -top alu_cla_flags_tb
ISim P.20131013 ( signature 0x7708f090 )
Number of CPUs detected in this system: 8
Turning on mult-threading, number of parallel sub-compilation jobs: 16
Determining compilation order of HDL files
Parsing VHDL file "cla_gp.vhd" into library work
Parsing VHDL file "cla_add_n_bit.vhd" into library work
Parsing VHDL file "alu_cla.vhd" into library work
Parsing VHDL file "alu_cla_tb_FLAGS_IDEAL.vhd" into library work
Starting static elaboration
Completed static elaboration
Compiling package standard
Compiling package std_logic_1164
Compiling package textio
Compiling package std_logic_textio
Compiling package numeric_std
Compiling package attributes
Compiling package std_logic_misc
Compiling architecture ndv of entity cla_add_n_bit [\cla_add_n_bit( 8 )\]
Compiling architecture ndv of entity alu_cla [\alu_cla( 8 )\]
Compiling architecture test_alu_flags of entity alu_cla_flags_tb
Time Resolution for simulation is 1ps.
Waiting for 1 sub-compilation( s ) to finish...
Compiled 12 VHDL Units
Built simulation executable alu_cla_flags_tb_isim_beh.exe

```


Fuse Memory Usage: 37536 KB
Fuse CPU Usage: 858 ms

```
64200296>alu_cla_flags_tb_isim_beh.exe -tclbatch isim.tcl -wdb
alu_cla_flags_tb_isim_beh.wdb
ISim P.20131013 ( signature 0x7708f090 )
WARNING: A WEBPACK license was found.
WARNING: Please use Xilinx License Configuration Manager to check out a full ISim
license.
WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for
more information on the differences between the Lite and the Full version.
This is a Lite version of ISim.
Time resolution is 1 ps
Simulator is doing circuit initialization process.
Finished circuit initialization process.
```

```
-- *****
-- **** STUDENT: 64200385
-- *****
-- KOMENTARJI K OCENI NALOGE
-- Matej Možek: Ni pripomb
-- *****
```

```
64200385>rem ***** test cla adder
```

```
64200385>if not exist "xst" mkdir xst
```

```
64200385>cd XST
```

```
64200385\xst>if not exist "projnav.tmp" mkdir "projnav.tmp"
```

```
64200385\xst>cd ..
```

```
64200385>rem ***** test cla operations
```

```
64200385>xst -ifn cla_add_n_bit.xst
Release 14.7 - xst P.20131013 ( nt64 )
Copyright ( c ) 1995-2013 Xilinx, Inc. All rights reserved.
-- > Parameter TMPDIR set to xst/projnav.tmp
```

```
Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.25 secs
```

```
-- > Parameter xsthdpdir set to xst
```

```
Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.25 secs
```

```
-- >
```

```
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```
=====
* Synthesis Options Summary *
```

```
=====
-- -- Source Parameters
```

```
Input File Name : "cla_add_n_bit.prj"
```

Ignore Synthesis Constraint File : NO

-- -- Target Parameters

Output File Name : "cla_add_n_bit"

Output Format : NGC

Target Device : xc6slx4-3-tqg144

-- -- Source Options

Top Module Name : cla_add_n_bit

Automatic FSM Extraction : YES

FSM Encoding Algorithm : Auto

Safe Implementation : No

FSM Style : LUT

RAM Extraction : Yes

RAM Style : Auto

ROM Extraction : Yes

Shift Register Extraction : YES

ROM Style : Auto

Resource Sharing : YES

Asynchronous To Synchronous : NO

Shift Register Minimum Size : 2

Use DSP Block : Auto

Automatic Register Balancing : No

-- -- Target Options

LUT Combining : Auto

Reduce Control Sets : Auto

Add IO Buffers : YES

Global Maximum Fanout : 100000

Add Generic Clock Buffer(BUFG) : 16

Register Duplication : YES

Optimize Instantiated Primitives : NO

Use Clock Enable : Auto

Use Synchronous Set : Auto

Use Synchronous Reset : Auto

Pack IO Registers into IOBs : Auto

Equivalent register Removal : YES

-- -- General Options

Optimization Goal : Speed

Optimization Effort : 1

Power Reduction : NO

Keep Hierarchy : No

Netlist Hierarchy : As_Optimized

RTL Output : Yes

Global Optimization : AllClockNets

Read Cores : YES

Write Timing Constraints : NO

Cross Clock Analysis : NO

Hierarchy Separator : /

Bus Delimiter : <>

Case Specifier : Maintain

Slice Utilization Ratio : 100

BRAM Utilization Ratio : 100

DSP48 Utilization Ratio : 100

Auto BRAM Packing : NO

Slice Utilization Ratio Delta : 5

=====

```

=====
* HDL Parsing *
=====
Parsing VHDL file "64200385\cla_gp.vhd" into library work
Parsing entity <cla_gp>.
Parsing architecture <ideal> of entity <cla_gp>.
Parsing VHDL file "64200385\cla_add_n_bit.vhd" into library work
Parsing entity <cla_add_n_bit>.
Parsing architecture <arch> of entity <cla_add_n_bit>.

=====
* HDL Elaboration *
=====

Elaborating entity <cla_add_n_bit> ( architecture <arch> ) with generics from
library <work>.

=====
* HDL Synthesis *
=====

Synthesizing Unit <cla_add_n_bit>.
Related source file is "64200385\cla_add_n_bit.vhd".
  n = 8
  Summary:
Unit <cla_add_n_bit> synthesized.

=====
HDL Synthesis Report

Macro Statistics
# Xors : 16
  1-bit xor2 : 16

=====

=====
* Advanced HDL Synthesis *
=====

=====
Advanced HDL Synthesis Report

Macro Statistics
# Xors : 16
  1-bit xor2 : 16

=====

=====
* Low Level Synthesis *
=====

Optimizing unit <cla_add_n_bit> ...

Mapping all equations...
Building and optimizing final netlist ...

```

Found area constraint ratio of 100 (+ 5) on block cla_add_n_bit, actual ratio is 1.

Final Macro Processing ...

=====
Final Register Report

Found no macro

=====
* Partition Report *
=====

Partition Implementation Status

-- -- -- -- -- -- -- -- -- -- -- -- -- --
-- -- -

No Partitions were found in this design.

-- -- -- -- -- -- -- -- -- -- -- -- -- --
-- -- -

=====
* Design Summary *
=====

Top Level Output File Name : cla_add_n_bit.ngc

Primitive and Black Box Usage:

-- -- -- -- -- -- -- -- -- -- -- -- -- --
-- -- -

BELS : 24
LUT2 : 3
LUT3 : 4
LUT4 : 2
LUT5 : 5
LUT6 : 9
MUXF7 : 1
IO Buffers : 28
IBUF : 17
OBUF : 11

Device utilization summary:

-- -- -- -- -- -- -- -- -- -- -- -- -- --
-

Selected Device : 6slx4tqg144-3

Slice Logic Utilization:

Number of Slice LUTs: 23 out of 2400 0%
Number used as Logic: 23 out of 2400 0%

Slice Logic Distribution:

Number of LUT Flip Flop pairs used: 23
Number with an unused Flip Flop: 23 out of 23 100%
Number with an unused LUT: 0 out of 23 0%
Number of fully used LUT-FF pairs: 0 out of 23 0%

Number of unique control sets: 0

IO Utilization:

Number of IOs: 28

Number of bonded IOBs: 28 out of 102 27%

Specific Feature Utilization:

```
-- -- -- -- -- -- -- -- -- -- -- -- -- --
-
Partition Resource Summary:
-- -- -- -- -- -- -- -- -- -- -- -- -- --
-
```

No Partitions were found in this design.

```
-- -- -- -- -- -- -- -- -- -- -- -- -- --
-
```

=====
Timing Report

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.
FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT
GENERATED AFTER PLACE-and-ROUTE.

Clock Information:

```
-- -- -- -- -- -- -- -- -- -- -- -- -- --
```

No clock signals found in this design

Asynchronous Control Signals Information:

```
-- -- -- -- -- -- -- -- -- -- -- -- -- --
-- -- -- -- -- -- -- -- -- -- -- -- -- --
```

No asynchronous control signals found in this design

Timing Summary:

```
-- -- -- -- -- -- -- -- -- -- -- -- -- --
```

Speed Grade: -3

Minimum period: No path found
Minimum input arrival time before clock: No path found
Maximum output required time after clock: No path found
Maximum combinational path delay: 8.614ns

Timing Details:

```
-- -- -- -- -- -- -- -- -- -- -- -- -- --
```

All values displayed in nanoseconds (ns)

=====
Timing constraint: Default path analysis

Total number of paths / destination ports: 159 / 11

```
-- -- -- -- -- -- -- -- -- -- -- -- -- --
-- -- -- -- -- -- -- -- -- -- -- -- -- --
-- -- -- -- -- -- -- -- -- -- -- -- -- --
```

Delay: 8.614ns (Levels of Logic = 7)
Source: Y<0> (PAD)
Destination: Cout (PAD)

Data Path: Y<0> to Cout

```

Gate Net
Cell:in->out fanout Delay Delay Logical Name ( Net Name )
-- -- -- -- -- -- -- -- -- -- -- --
-- -- -- -- -- -- -- -- -- -- -- --
-- --
IBUF:I->0 6 1.222 0.973 Y_0_IBUF ( Y_0_IBUF )
LUT3:I0->0 1 0.205 0.580 C<4>2_SW0 ( N01 )
LUT5:I4->0 4 0.205 0.684 C<4>2 ( C<4>2 )
LUT5:I4->0 4 0.205 1.048 Mxor_S_sig<5>_xo<0>11 ( Mxor_S_sig<5>_xo<0>1 )
LUT6:I0->0 1 0.203 0.000 Cout_G ( N8 )
MUXF7:I1->0 1 0.140 0.579 Cout ( Cout_OBUF )
OBUF:I->0 2.571 Cout_OBUF ( Cout )
-- -- -- -- -- -- -- -- -- -- -- --
-- -- -- -- -- -- -- -- -- -- -- --
Total 8.614ns ( 4.751ns logic, 3.863ns route )
( 55.2% logic, 44.8% route )

```

===== Cross Clock Domains Report:

```

-- -- -- -- -- -- -- -- -- -- -- --
=====  

Total REAL time to Xst completion: 9.00 secs
Total CPU time to Xst completion: 8.40 secs

```

```
-- >
```

Total memory usage is 4487500 kilobytes

Number of errors : 0 (0 filtered)

Number of warnings : 0 (0 filtered)

Number of infos : 0 (0 filtered)

```

64200385>fuse -incremental -o cla_add_n_bit_tb_isim_beh.exe -prj
cla_add_n_bit_tb.prj -top cla_add_n_bit_tb
Running: \unwrapped\fuse.exe -incremental -o cla_add_n_bit_tb_isim_beh.exe -prj
cla_add_n_bit_tb.prj -top cla_add_n_bit_tb
ISim P.20131013 ( signature 0x7708f090 )
Number of CPUs detected in this system: 8
Turning on mult-threading, number of parallel sub-compilation jobs: 16
Determining compilation order of HDL files
Parsing VHDL file "cla_gp.vhd" into library work
Parsing VHDL file "cla_add_n_bit.vhd" into library work
Parsing VHDL file "cla_add_n_bit_tb_IDEAL.vhd" into library work
Starting static elaboration
Completed static elaboration
Compiling package standard
Compiling package std_logic_1164
Compiling package textio
Compiling package std_logic_textio
Compiling package numeric_std
Compiling package attributes
Compiling package std_logic_misc
Compiling architecture arch of entity cla_add_n_bit [\cla_add_n_bit( 8 )\]
Compiling architecture testbench_arch of entity cla_add_n_bit_tb
Time Resolution for simulation is 1ps.
Waiting for 1 sub-compilation( s ) to finish...

```

Compiled 10 VHDL Units
Built simulation executable cla_add_n_bit_tb_isim_beh.exe
Fuse Memory Usage: 37456 KB
Fuse CPU Usage: 859 ms

```
64200385>cla_add_n_bit_tb_isim_beh.exe -tclbatch isim.tcl -wdb
cla_add_n_bit_tb_isim_beh.wdb
ISim P.20131013 ( signature 0x7708f090 )
WARNING: A WEBPACK license was found.
WARNING: Please use Xilinx License Configuration Manager to check out a full ISim
license.
WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for
more information on the differences between the Lite and the Full version.
This is a Lite version of ISim.
Time resolution is 1 ps
Simulator is doing circuit initialization process.
Finished circuit initialization process.
```

```
64200385>rem ***** test cla flags
```

```
64200385>xst -ifn cla_add_n_bit_flags.xst
Release 14.7 - xst P.20131013 ( nt64 )
Copyright ( c ) 1995-2013 Xilinx, Inc. All rights reserved.
-- > Parameter TMPDIR set to xst/projnav.tmp
```

```
Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.23 secs
```

```
-- > Parameter xsthdpdir set to xst
```

```
Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.24 secs
```

```
-- > ERROR:Xst:438 - Can not open file : cla_add_n_bit_flags.prj
```

```
Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.26 secs
```

```
-- >
```

```
Total memory usage is 4422880 kilobytes
```

```
Number of errors : 1 ( 0 filtered )
```

```
Number of warnings : 0 ( 0 filtered )
```

```
Number of infos : 0 ( 0 filtered )
```

```
64200385>fuse -incremental -o cla_add_n_bit_tb_flags_isim_beh.exe -prj
cla_add_n_bit_flags_tb.prj -top cla_add_n_bit_flags_tb_IDEAL
Running: \unwrapped\fuse.exe -incremental -o cla_add_n_bit_tb_flags_isim_beh.exe -
prj cla_add_n_bit_flags_tb.prj -top cla_add_n_bit_flags_tb_IDEAL
ISim P.20131013 ( signature 0x7708f090 )
Number of CPUs detected in this system: 8
Turning on mult-threading, number of parallel sub-compilation jobs: 16
Determining compilation order of HDL files
Parsing VHDL file "cla_gp.vhd" into library work
Parsing VHDL file "cla_add_n_bit.vhd" into library work
Parsing VHDL file "cla_add_n_bit_flags_tb_IDEAL.vhd" into library work
Starting static elaboration
Completed static elaboration
```



```

Compiling package standard
Compiling package std_logic_1164
Compiling package textio
Compiling package std_logic_textio
Compiling package numeric_std
Compiling package attributes
Compiling package std_logic_misc
Compiling architecture arch of entity cla_add_n_bit [\cla_add_n_bit( 8 )\]
Compiling architecture a1 of entity cla_add_n_bit_flags_tb_ideal
Time Resolution for simulation is 1ps.
Waiting for 1 sub-compilation( s ) to finish...
Compiled 10 VHDL Units
Built simulation executable cla_add_n_bit_tb_flags_isim_beh.exe
Fuse Memory Usage: 37444 KB
Fuse CPU Usage: 999 ms

64200385>cla_add_n_bit_tb_flags_isim_beh.exe -tclbatch isim.tcl -wdb
cla_add_n_bit_flags_tb.wdb
ISim P.20131013 ( signature 0x7708f090 )
WARNING: A WEBPACK license was found.
WARNING: Please use Xilinx License Configuration Manager to check out a full ISim
license.
WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for
more information on the differences between the Lite and the Full version.
This is a Lite version of ISim.
Time resolution is 1 ps
Simulator is doing circuit initialization process.
Finished circuit initialization process.

64200385>rem ***** test alu operations

64200385>xst -ifn alu_cla.xst
Release 14.7 - xst P.20131013 ( nt64 )
Copyright ( c ) 1995-2013 Xilinx, Inc. All rights reserved.
-- > Parameter TMPDIR set to xst/projnav.tmp

Total REAL time to Xst completion: 1.00 secs
Total CPU time to Xst completion: 0.23 secs

-- > Parameter xsthdmdir set to xst

Total REAL time to Xst completion: 1.00 secs
Total CPU time to Xst completion: 0.24 secs

-- >
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```

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8.4.5) Cross Clock Domains Report

```
=====
* Synthesis Options Summary *
=====
--      -- Source Parameters
Input File Name : "alu_cla.prj"
Ignore Synthesis Constraint File : NO

--      -- Target Parameters
Output File Name : "alu_cla"
Output Format : NGC
Target Device : xc6slx4-3-tqg144

--      -- Source Options
Top Module Name : alu_cla
Automatic FSM Extraction : YES
FSM Encoding Algorithm : Auto
Safe Implementation : No
FSM Style : LUT
RAM Extraction : Yes
RAM Style : Auto
ROM Extraction : Yes
Shift Register Extraction : YES
ROM Style : Auto
Resource Sharing : YES
Asynchronous To Synchronous : NO
Shift Register Minimum Size : 2
Use DSP Block : Auto
Automatic Register Balancing : No

--      -- Target Options
LUT Combining : Auto
Reduce Control Sets : Auto
Add IO Buffers : YES
Global Maximum Fanout : 100000
Add Generic Clock Buffer( BUFG ) : 16
Register Duplication : YES
Optimize Instantiated Primitives : NO
Use Clock Enable : Auto
Use Synchronous Set : Auto
Use Synchronous Reset : Auto
Pack IO Registers into IOBs : Auto
Equivalent register Removal : YES

--      -- General Options
Optimization Goal : Speed
Optimization Effort : 1
Power Reduction : NO
Keep Hierarchy : No
Netlist Hierarchy : As_Optimized
RTL Output : Yes
Global Optimization : AllClockNets
Read Cores : YES
```

Write Timing Constraints : NO

Cross Clock Analysis : NO

Hierarchy Separator : /

Bus Delimiter : <>

Case Specifier : Maintain

Slice Utilization Ratio : 100

BRAM Utilization Ratio : 100

DSP48 Utilization Ratio : 100

Auto BRAM Packing : NO

Slice Utilization Ratio Delta : 5

=====

=====

* HDL Parsing *

=====

Parsing VHDL file "64200385\cla_gp.vhd" into library work

Parsing entity <cla_gp>.

Parsing architecture <ideal> of entity <cla_gp>.

Parsing VHDL file "64200385\cla_add_n_bit.vhd" into library work

Parsing entity <cla_add_n_bit>.

Parsing architecture <arch> of entity <cla_add_n_bit>.

Parsing VHDL file "64200385\alu_cla.vhd" into library work

Parsing entity <alu_cla>.

Parsing architecture <NDV> of entity <alu_cla>.

=====

* HDL Elaboration *

=====

Elaborating entity <alu_cla> (architecture <NDV>) with generics from library <work>.

Elaborating entity <cla_add_n_bit> (architecture <arch>) with generics from library <work>.

=====

* HDL Synthesis *

=====

Synthesizing Unit <alu_cla>.

Related source file is "64200385\alu_cla.vhd".

n = 8

Found 8-bit 12-to-1 multiplexer for signal <S> created at line 49.

Summary:

inferred 7 Multiplexer(s).

Unit <alu_cla> synthesized.

Synthesizing Unit <cla_add_n_bit>.

Related source file is "64200385\cla_add_n_bit.vhd".

n = 8

Summary:

Unit <cla_add_n_bit> synthesized.

=====

HDL Synthesis Report

Macro Statistics

Multiplexers : 7

```
8-bit 12-to-1 multiplexer : 1
8-bit 2-to-1 multiplexer : 6
# Xors : 17
1-bit xor2 : 16
8-bit xor2 : 1
```

=====

=====

```
* Advanced HDL Synthesis *
```

=====

=====

```
Advanced HDL Synthesis Report
```

```
Macro Statistics
```

```
# Multiplexers : 7
8-bit 12-to-1 multiplexer : 1
8-bit 2-to-1 multiplexer : 6
# Xors : 17
1-bit xor2 : 16
8-bit xor2 : 1
```

=====

=====

```
* Low Level Synthesis *
```

=====

```
Optimizing unit <alu_cla> ...
```

```
Optimizing unit <cla_add_n_bit> ...
```

```
Mapping all equations...
```

```
Building and optimizing final netlist ...
```

```
Found area constraint ratio of 100 ( + 5 ) on block alu_cla, actual ratio is 3.
```

```
Final Macro Processing ...
```

=====

```
Final Register Report
```

```
Found no macro
```

=====

=====

```
* Partition Report *
```

=====

```
Partition Implementation Status
```

```
--      --      --      --      --      --      --      --      --      --      --      --
--      --      --      --      --      --      --      --      --      --      --      --
```

```
No Partitions were found in this design.
```

```
--      --      --      --      --      --      --      --      --      --      --      --
--      --      --      --      --      --      --      --      --      --      --      --
```

=====

* Design Summary *

=====

Top Level Output File Name : alu_cla.ngc

Primitive and Black Box Usage:

```
--      --      --      --      --      --      --      --      --      --      --      --
--      --      --
# BELS : 49
# LUT3 : 3
# LUT4 : 2
# LUT5 : 13
# LUT6 : 28
# MUXF7 : 3
# IO Buffers : 34
# IBUF : 20
# OBUF : 14
```

Device utilization summary:

```
--      --      --      --      --      --      --      --      --      --      --      --
-
```

Selected Device : 6slx4tqg144-3

Slice Logic Utilization:

Number of Slice LUTs: 46 out of 2400 1%
Number used as Logic: 46 out of 2400 1%

Slice Logic Distribution:

Number of LUT Flip Flop pairs used: 46
Number with an unused Flip Flop: 46 out of 46 100%
Number with an unused LUT: 0 out of 46 0%
Number of fully used LUT-FF pairs: 0 out of 46 0%
Number of unique control sets: 0

IO Utilization:

Number of IOs: 34
Number of bonded IOBs: 34 out of 102 33%

Specific Feature Utilization:

```
--      --      --      --      --      --      --      --      --      --      --      --
-
```

Partition Resource Summary:

```
--      --      --      --      --      --      --      --      --      --      --      --
-
```

No Partitions were found in this design.

```
--      --      --      --      --      --      --      --      --      --      --      --
-
```

=====

Timing Report

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.
FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT
GENERATED AFTER PLACE-and-ROUTE.

Clock Information:

-- -- -- -- --
No clock signals found in this design

Asynchronous Control Signals Information:

-- -- -- -- --
-- -- -- -- --
No asynchronous control signals found in this design

Timing Summary:

-- -- -- -- --
Speed Grade: -3

Minimum period: No path found
Minimum input arrival time before clock: No path found
Maximum output required time after clock: No path found
Maximum combinational path delay: 11.603ns

Timing Details:

-- -- -- -- --
All values displayed in nanoseconds (ns)

=====
Timing constraint: Default path analysis

Total number of paths / destination ports: 1008 / 14

-- -- -- -- --
-- -- -- -- --
-- -- -- -- --

Delay: 11.603ns (Levels of Logic = 8)

Source: F<2> (PAD)

Destination: Zero (PAD)

Data Path: F<2> to Zero

Gate Net

Cell: in->out fanout Delay Delay Logical Name (Net Name)

-- -- -- -- --
-- -- -- -- --
-- -- -- -- --

IBUF:I->O 27 1.222 1.565 F_2_IBUF (F_2_IBUF)

LUT6:I1->O 5 0.203 0.943 Mmux_Yint31 (Yint<1>)

LUT5:I2->O 3 0.205 0.651 U1/C<4>22 (U1/C<4>2)

LUT5:I4->O 5 0.205 0.943 U1/Mxor_S_sig<5>_xo<0>11 (U1/Mxor_S_sig<5>_xo<0>1)

LUT5:I2->O 1 0.205 0.924 U1/Mxor_S_sig<6>_xo<0>1 (Sint<6>)

LUT6:I1->O 2 0.203 0.981 Mmux_S162 (S_6_OBUF)

LUT6:I0->O 1 0.203 0.579 Zero (Zero_OBUF)

OBUF:I->O 2.571 Zero_OBUF (Zero)

-- -- -- -- --
-- -- -- -- --

Total 11.603ns (5.017ns logic, 6.586ns route)

(43.2% logic, 56.8% route)

=====
Cross Clock Domains Report:

-- -- -- -- --

=====
Total REAL time to Xst completion: 10.00 secs

Total CPU time to Xst completion: 9.53 secs

-- >

Total memory usage is 4487500 kilobytes

Number of errors : 0 (0 filtered)

Number of warnings : 0 (0 filtered)

Number of infos : 0 (0 filtered)

64200385>fuse -incremental -o alu_cla_tb_isim_beh.exe -prj alu_cla_tb.prj -top alu_cla_tb

Running: \unwrapped\fuse.exe -incremental -o alu_cla_tb_isim_beh.exe -prj alu_cla_tb.prj -top alu_cla_tb

ISim P.20131013 (signature 0x7708f090)

Number of CPUs detected in this system: 8

Turning on mult-threading, number of parallel sub-compilation jobs: 16

Determining compilation order of HDL files

Parsing VHDL file "cla_gp.vhd" into library work

Parsing VHDL file "cla_add_n_bit.vhd" into library work

Parsing VHDL file "alu_cla.vhd" into library work

Parsing VHDL file "alu_cla_tb_IDEAL.vhd" into library work

Starting static elaboration

Completed static elaboration

Compiling package standard

Compiling package std_logic_1164

Compiling package textio

Compiling package std_logic_textio

Compiling package numeric_std

Compiling package attributes

Compiling package std_logic_misc

Compiling architecture arch of entity cla_add_n_bit [\cla_add_n_bit(8)\]

Compiling architecture ndv of entity alu_cla [\alu_cla(8)\]

Compiling architecture testbench_arch of entity alu_cla_tb

Time Resolution for simulation is 1ps.

Waiting for 1 sub-compilation(s) to finish...

Compiled 12 VHDL Units

Built simulation executable alu_cla_tb_isim_beh.exe

Fuse Memory Usage: 37484 KB

Fuse CPU Usage: 952 ms

64200385>alu_cla_tb_isim_beh.exe -tclbatch isim.tcl -wdb alu_cla_tb_isim_beh.wdb

ISim P.20131013 (signature 0x7708f090)

WARNING: A WEBPACK license was found.

WARNING: Please use Xilinx License Configuration Manager to check out a full ISim license.

WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for more information on the differences between the Lite and the Full version.

This is a Lite version of ISim.

Time resolution is 1 ps

Simulator is doing circuit initialization process.

Finished circuit initialization process.

at 7864320 ns, Instance /alu_cla_tb/ : Warning: NUMERIC_STD.TO_UNSIGNED: vector truncated

at 8847360 ns, Instance /alu_cla_tb/ : Warning: NUMERIC_STD.TO_UNSIGNED: vector truncated

at 9830400 ns, Instance /alu_cla_tb/ : Warning: NUMERIC_STD.TO_UNSIGNED: vector truncated

at 10813440 ns, Instance /alu_cla_tb/ : Warning: NUMERIC_STD.TO_UNSIGNED: vector truncated
at 11796480 ns, Instance /alu_cla_tb/ : Warning: NUMERIC_STD.TO_UNSIGNED: vector truncated
at 12779520 ns, Instance /alu_cla_tb/ : Warning: NUMERIC_STD.TO_UNSIGNED: vector truncated
at 13762560 ns, Instance /alu_cla_tb/ : Warning: NUMERIC_STD.TO_UNSIGNED: vector truncated
at 14745600 ns, Instance /alu_cla_tb/ : Warning: NUMERIC_STD.TO_UNSIGNED: vector truncated

64200385>rem ***** test alu flags

64200385>xst -ifn alu_cla_flags.xst
Release 14.7 - xst P.20131013 (nt64)
Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.
-- > Parameter TMPDIR set to xst/projnav.tmp

Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.24 secs

-- > Parameter xsthdpdir set to xst

Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.24 secs

-- >

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=====
* Synthesis Options Summary *
=====

-- -- Source Parameters

Input File Name : "alu_cla_flags_tb.prj"
Ignore Synthesis Constraint File : NO

-- -- Target Parameters

Output File Name : "alu_cla_flags_tb"
Output Format : NGC
Target Device : xc6slx4-3-tqg144

-- -- Source Options

Top Module Name : alu_cla_flags_tb
Automatic FSM Extraction : YES
FSM Encoding Algorithm : Auto
Safe Implementation : No
FSM Style : LUT
RAM Extraction : Yes
RAM Style : Auto
ROM Extraction : Yes
Shift Register Extraction : YES
ROM Style : Auto
Resource Sharing : YES
Asynchronous To Synchronous : NO
Shift Register Minimum Size : 2
Use DSP Block : Auto
Automatic Register Balancing : No

-- -- Target Options

LUT Combining : Auto
Reduce Control Sets : Auto
Add IO Buffers : YES
Global Maximum Fanout : 100000
Add Generic Clock Buffer(BUFG) : 16
Register Duplication : YES
Optimize Instantiated Primitives : NO
Use Clock Enable : Auto
Use Synchronous Set : Auto
Use Synchronous Reset : Auto
Pack IO Registers into IOBs : Auto
Equivalent register Removal : YES

-- -- General Options

Optimization Goal : Speed
Optimization Effort : 1
Power Reduction : NO
Keep Hierarchy : No
Netlist Hierarchy : As_Optimized
RTL Output : Yes
Global Optimization : AllClockNets
Read Cores : YES
Write Timing Constraints : NO
Cross Clock Analysis : NO
Hierarchy Separator : /
Bus Delimiter : <>
Case Specifier : Maintain
Slice Utilization Ratio : 100
BRAM Utilization Ratio : 100
DSP48 Utilization Ratio : 100
Auto BRAM Packing : NO
Slice Utilization Ratio Delta : 5

=====

=====

* HDL Parsing *

=====

Parsing VHDL file "64200385\cla_gp.vhd" into library work
Parsing entity <cla_gp>.

```

Parsing architecture <ideal> of entity <cla_gp>.
Parsing VHDL file "64200385\cla_add_n_bit.vhd" into library work
Parsing entity <cla_add_n_bit>.
Parsing architecture <arch> of entity <cla_add_n_bit>.
Parsing VHDL file "64200385\alu_cla.vhd" into library work
Parsing entity <alu_cla>.
Parsing architecture <NDV> of entity <alu_cla>.
Parsing VHDL file "64200385\alu_cla_tb_FLAGS_IDEAL.vhd" into library work
Parsing entity <alu_cla_flags_tb>.
Parsing architecture <test_alu_flags> of entity <alu_cla_flags_tb>.

=====
* HDL Elaboration *
=====

Elaborating entity <alu_cla_flags_tb> ( architecture <test_alu_flags> ) with
generics from library <work>.

Elaborating entity <alu_cla> ( architecture <NDV> ) with generics from library
<work>.

Elaborating entity <cla_add_n_bit> ( architecture <arch> ) with generics from
library <work>.
ERROR:HDLCompiler:890 - "64200385\alu_cla_tb_FLAGS_IDEAL.vhd" Line 144: wait
statement without UNTIL clause not supported for synthesis
Netlist alu_cla_flags_tb( 8 )( test_alu_flags ) remains a blackbox, due to errors
in its contents
-- >

Total memory usage is 4466680 kilobytes

Number of errors : 1 ( 0 filtered )
Number of warnings : 0 ( 0 filtered )
Number of infos : 0 ( 0 filtered )

64200385>fuse -incremental -o alu_cla_flags_tb_isim_beh.exe -prj
alu_cla_flags_tb.prj -top alu_cla_flags_tb
Running: \unwrapped\fuse.exe -incremental -o alu_cla_flags_tb_isim_beh.exe -prj
alu_cla_flags_tb.prj -top alu_cla_flags_tb
ISim P.20131013 ( signature 0x7708f090 )
Number of CPUs detected in this system: 8
Turning on mult-threading, number of parallel sub-compilation jobs: 16
Determining compilation order of HDL files
Parsing VHDL file "cla_gp.vhd" into library work
Parsing VHDL file "cla_add_n_bit.vhd" into library work
Parsing VHDL file "alu_cla.vhd" into library work
Parsing VHDL file "alu_cla_tb_FLAGS_IDEAL.vhd" into library work
Starting static elaboration
Completed static elaboration
Compiling package standard
Compiling package std_logic_1164
Compiling package textio
Compiling package std_logic_textio
Compiling package numeric_std
Compiling package attributes
Compiling package std_logic_misc
Compiling architecture arch of entity cla_add_n_bit [\cla_add_n_bit( 8 )\]
Compiling architecture ndv of entity alu_cla [\alu_cla( 8 )\]
Compiling architecture test_alu_flags of entity alu_cla_flags_tb

```

Time Resolution for simulation is 1ps.
Waiting for 1 sub-compilation(s) to finish...
Compiled 12 VHDL Units
Built simulation executable alu_cla_flags_tb_isim_beh.exe
Fuse Memory Usage: 37460 KB
Fuse CPU Usage: 999 ms

64200385>alu_cla_flags_tb_isim_beh.exe -tclbatch isim.tcl -wdb
alu_cla_flags_tb_isim_beh.wdb
ISim P.20131013 (signature 0x7708f090)
WARNING: A WEBPACK license was found.
WARNING: Please use Xilinx License Configuration Manager to check out a full ISim license.
WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for more information on the differences between the Lite and the Full version.
This is a Lite version of ISim.
Time resolution is 1 ps
Simulator is doing circuit initialization process.
Finished circuit initialization process.

```
-- *****
-- **** STUDENT: 64210113
-- *****
-- KOMENTARJI K OCENI NALOGE
-- Matej Možek: Ni pripomb
-- *****
```

```
64210113>rem ***** test cla adder
```

```
64210113>if not exist "xst" mkdir xst
```

```
64210113>cd XST
```

```
64210113\xst>if not exist "projnav.tmp" mkdir "projnav.tmp"
```

```
64210113\xst>cd ..
```

```
64210113>rem ***** test cla operations
```

```
64210113>xst -ifn cla_add_n_bit.xst
Release 14.7 - xst P.20131013 ( nt64 )
Copyright ( c ) 1995-2013 Xilinx, Inc. All rights reserved.
-- > Parameter TMPDIR set to xst/projnav.tmp
```

```
Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.24 secs
```

```
-- > Parameter xsthdpdir set to xst
```

```
Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.24 secs
```

```
-- >
```

```
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- 8.4.5) Cross Clock Domains Report

```
=====
* Synthesis Options Summary *
```

```
=====
-- -- Source Parameters
```

```
Input File Name : "cla_add_n_bit.prj"
```

Ignore Synthesis Constraint File : NO

-- -- Target Parameters

Output File Name : "cla_add_n_bit"

Output Format : NGC

Target Device : xc6slx4-3-tqg144

-- -- Source Options

Top Module Name : cla_add_n_bit

Automatic FSM Extraction : YES

FSM Encoding Algorithm : Auto

Safe Implementation : No

FSM Style : LUT

RAM Extraction : Yes

RAM Style : Auto

ROM Extraction : Yes

Shift Register Extraction : YES

ROM Style : Auto

Resource Sharing : YES

Asynchronous To Synchronous : NO

Shift Register Minimum Size : 2

Use DSP Block : Auto

Automatic Register Balancing : No

-- -- Target Options

LUT Combining : Auto

Reduce Control Sets : Auto

Add IO Buffers : YES

Global Maximum Fanout : 100000

Add Generic Clock Buffer(BUFG) : 16

Register Duplication : YES

Optimize Instantiated Primitives : NO

Use Clock Enable : Auto

Use Synchronous Set : Auto

Use Synchronous Reset : Auto

Pack IO Registers into IOBs : Auto

Equivalent register Removal : YES

-- -- General Options

Optimization Goal : Speed

Optimization Effort : 1

Power Reduction : NO

Keep Hierarchy : No

Netlist Hierarchy : As_Optimized

RTL Output : Yes

Global Optimization : AllClockNets

Read Cores : YES

Write Timing Constraints : NO

Cross Clock Analysis : NO

Hierarchy Separator : /

Bus Delimiter : <>

Case Specifier : Maintain

Slice Utilization Ratio : 100

BRAM Utilization Ratio : 100

DSP48 Utilization Ratio : 100

Auto BRAM Packing : NO

Slice Utilization Ratio Delta : 5

=====

```

=====
* HDL Parsing *
=====
Parsing VHDL file "64210113\cla_gp.vhd" into library work
Parsing entity <cla_gp>.
Parsing architecture <ideal> of entity <cla_gp>.
Parsing VHDL file "64210113\cla_add_n_bit.vhd" into library work
Parsing entity <cla_add_n_bit>.
Parsing architecture <NDV> of entity <cla_add_n_bit>.

=====
* HDL Elaboration *
=====

Elaborating entity <cla_add_n_bit> ( architecture <NDV> ) with generics from
library <work>.

=====
* HDL Synthesis *
=====

Synthesizing Unit <cla_add_n_bit>.
Related source file is "64210113\cla_add_n_bit.vhd".
  n = 8
  Summary:
Unit <cla_add_n_bit> synthesized.

=====
HDL Synthesis Report

Macro Statistics
# Xors : 16
  1-bit xor2 : 16

=====

=====
* Advanced HDL Synthesis *
=====

=====
Advanced HDL Synthesis Report

Macro Statistics
# Xors : 16
  1-bit xor2 : 16

=====

=====
* Low Level Synthesis *
=====

Optimizing unit <cla_add_n_bit> ...

Mapping all equations...
Building and optimizing final netlist ...

```

Found area constraint ratio of 100 (+ 5) on block cla_add_n_bit, actual ratio is 1.

Final Macro Processing ...

=====
Final Register Report

Found no macro

=====
* Partition Report *
=====

Partition Implementation Status

-- -- -- -- -- -- -- -- -- -- -- -- -- --
-- -- -

No Partitions were found in this design.

-- -- -- -- -- -- -- -- -- -- -- -- -- --
-- -- -

=====
* Design Summary *
=====

Top Level Output File Name : cla_add_n_bit.ngc

Primitive and Black Box Usage:

-- -- -- -- -- -- -- -- -- -- -- -- -- --
-- -- -

BELS : 24
LUT2 : 6
LUT3 : 3
LUT5 : 6
LUT6 : 9
IO Buffers : 28
IBUF : 17
OBUF : 11

Device utilization summary:

-- -- -- -- -- -- -- -- -- -- -- -- -- --
-

Selected Device : 6slx4tqg144-3

Slice Logic Utilization:

Number of Slice LUTs: 24 out of 2400 1%
Number used as Logic: 24 out of 2400 1%

Slice Logic Distribution:

Number of LUT Flip Flop pairs used: 24
Number with an unused Flip Flop: 24 out of 24 100%
Number with an unused LUT: 0 out of 24 0%
Number of fully used LUT-FF pairs: 0 out of 24 0%
Number of unique control sets: 0

IO Utilization:

Number of IOs: 28

Number of bonded IOBs: 28 out of 102 27%

Specific Feature Utilization:

```
-- -- -- -- -- -- -- -- -- -- -- -- -- --  
-
```

Partition Resource Summary:

```
-- -- -- -- -- -- -- -- -- -- -- -- -- --  
-
```

No Partitions were found in this design.

```
-- -- -- -- -- -- -- -- -- -- -- -- -- --  
-
```

=====
Timing Report

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.

FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT
GENERATED AFTER PLACE-and-ROUTE.

Clock Information:

```
-- -- -- -- -- -- -- -- -- -- -- -- -- --  
No clock signals found in this design
```

Asynchronous Control Signals Information:

```
-- -- -- -- -- -- -- -- -- -- -- -- -- --  
-- -- -- -- -- -- -- -- -- -- -- -- -- --
```

No asynchronous control signals found in this design

Timing Summary:

```
-- -- -- -- -- -- -- -- -- -- -- -- -- --
```

Speed Grade: -3

Minimum period: No path found

Minimum input arrival time before clock: No path found

Maximum output required time after clock: No path found

Maximum combinational path delay: 9.101ns

Timing Details:

```
-- -- -- -- -- -- -- -- -- -- -- -- -- --
```

All values displayed in nanoseconds (ns)

=====
Timing constraint: Default path analysis

Total number of paths / destination ports: 131 / 11

```
-- -- -- -- -- -- -- -- -- -- -- -- -- --  
-- -- -- -- -- -- -- -- -- -- -- -- -- --  
-- -- -- -- -- -- -- -- -- -- -- -- -- --
```

Delay: 9.101ns (Levels of Logic = 7)

Source: Y<0> (PAD)

Destination: S<7> (PAD)

Data Path: Y<0> to S<7>

Gate Net

Cell:in->out fanout Delay Delay Logical Name (Net Name)


```

--      --      --      --      --      --      --      --      --      --      --
--      --      --      --      --      --      --      --      --      --      --
--      --
IBUF:I->0 6 1.222 0.973 Y_0_IBUF ( Y_0_IBUF )
LUT3:I0->0 2 0.205 0.617 C<3>_SW0 ( N2 )
LUT5:I4->0 3 0.205 0.651 C<3> ( C<3> )
LUT3:I2->0 2 0.205 0.617 C<6>_SW0 ( N4 )
LUT5:I4->0 2 0.205 0.845 C<6> ( C<6> )
LUT5:I2->0 1 0.205 0.579 Mxor_S_sig<7>_xo<0>1 ( S_7_OBUF )
OBUF:I->0 2.571 S_7_OBUF ( S<7> )
--      --      --      --      --      --      --      --      --      --      --
--      --      --      --      --      --      --      --      --      --      --
Total 9.101ns ( 4.818ns logic, 4.283ns route )
( 52.9% logic, 47.1% route )

```

Cross Clock Domains Report:

```

Total REAL time to Xst completion: 9.00 secs
Total CPU time to Xst completion: 9.22 secs

```

```
-- >
```

Total memory usage is 4487500 kilobytes

Number of errors : 0 (0 filtered)

Number of warnings : 0 (0 filtered)

Number of infos : 0 (0 filtered)

```

64210113>fuse -incremental -o cla_add_n_bit_tb_isim_beh.exe -prj
cla_add_n_bit_tb.prj -top cla_add_n_bit_tb
Running: \unwrapped\fuse.exe -incremental -o cla_add_n_bit_tb_isim_beh.exe -prj
cla_add_n_bit_tb.prj -top cla_add_n_bit_tb
ISim P.20131013 ( signature 0x7708f090 )
Number of CPUs detected in this system: 8
Turning on mult-threading, number of parallel sub-compilation jobs: 16
Determining compilation order of HDL files
Parsing VHDL file "cla_gp.vhd" into library work
Parsing VHDL file "cla_add_n_bit.vhd" into library work
Parsing VHDL file "cla_add_n_bit_tb_IDEAL.vhd" into library work
Starting static elaboration
Completed static elaboration
Compiling package standard
Compiling package std_logic_1164
Compiling package textio
Compiling package std_logic_textio
Compiling package numeric_std
Compiling package attributes
Compiling package std_logic_misc
Compiling architecture ndv of entity cla_add_n_bit [\cla_add_n_bit( 8 )\]
Compiling architecture testbench_arch of entity cla_add_n_bit_tb
Time Resolution for simulation is 1ps.
Waiting for 1 sub-compilation( s ) to finish...
Compiled 10 VHDL Units
Built simulation executable cla_add_n_bit_tb_isim_beh.exe

```

Fuse Memory Usage: 37412 KB
Fuse CPU Usage: 858 ms

```
64210113>cla_add_n_bit_tb_isim_beh.exe -tclbatch isim.tcl -wdb
cla_add_n_bit_tb_isim_beh.wdb
ISim P.20131013 ( signature 0x7708f090 )
WARNING: A WEBPACK license was found.
WARNING: Please use Xilinx License Configuration Manager to check out a full ISim
license.
WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for
more information on the differences between the Lite and the Full version.
This is a Lite version of ISim.
Time resolution is 1 ps
Simulator is doing circuit initialization process.
Finished circuit initialization process.
```

```
64210113>rem ***** test cla flags
```

```
64210113>xst -ifn cla_add_n_bit_flags.xst
Release 14.7 - xst P.20131013 ( nt64 )
Copyright ( c ) 1995-2013 Xilinx, Inc. All rights reserved.
-- > Parameter TMPDIR set to xst/projnav.tmp
```

Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.25 secs

```
-- > Parameter xsthdpdir set to xst
```

Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.25 secs

```
-- > ERROR:Xst:438 - Can not open file : cla_add_n_bit_flags.prj
```

Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.27 secs

```
-- >
```

Total memory usage is 4422880 kilobytes

Number of errors : 1 (0 filtered)
Number of warnings : 0 (0 filtered)
Number of infos : 0 (0 filtered)

```
64210113>fuse -incremental -o cla_add_n_bit_tb_flags_isim_beh.exe -prj
cla_add_n_bit_flags_tb.prj -top cla_add_n_bit_flags_tb_IDEAL
Running: \unwrapped\fuse.exe -incremental -o cla_add_n_bit_tb_flags_isim_beh.exe -
prj cla_add_n_bit_flags_tb.prj -top cla_add_n_bit_flags_tb_IDEAL
ISim P.20131013 ( signature 0x7708f090 )
Number of CPUs detected in this system: 8
Turning on mult-threading, number of parallel sub-compilation jobs: 16
Determining compilation order of HDL files
Parsing VHDL file "cla_gp.vhd" into library work
Parsing VHDL file "cla_add_n_bit.vhd" into library work
Parsing VHDL file "cla_add_n_bit_flags_tb_IDEAL.vhd" into library work
Starting static elaboration
Completed static elaboration
Compiling package standard
Compiling package std_logic_1164
```

```

Compiling package textio
Compiling package std_logic_textio
Compiling package numeric_std
Compiling package attributes
Compiling package std_logic_misc
Compiling architecture ndv of entity cla_add_n_bit [\cla_add_n_bit( 8 )\]
Compiling architecture a1 of entity cla_add_n_bit_flags_tb_ideal
Time Resolution for simulation is 1ps.
Waiting for 1 sub-compilation( s ) to finish...
Compiled 10 VHDL Units
Built simulation executable cla_add_n_bit_tb_flags_isim_beh.exe
Fuse Memory Usage: 37436 KB
Fuse CPU Usage: 999 ms

64210113>cla_add_n_bit_tb_flags_isim_beh.exe -tclbatch isim.tcl -wdb
cla_add_n_bit_flags_tb.wdb
ISim P.20131013 ( signature 0x7708f090 )
WARNING: A WEBPACK license was found.
WARNING: Please use Xilinx License Configuration Manager to check out a full ISim
license.
WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for
more information on the differences between the Lite and the Full version.
This is a Lite version of ISim.
Time resolution is 1 ps
Simulator is doing circuit initialization process.
Finished circuit initialization process.

64210113>rem ***** test alu operations

64210113>xst -ifn alu_cla.xst
Release 14.7 - xst P.20131013 ( nt64 )
Copyright ( c ) 1995-2013 Xilinx, Inc. All rights reserved.
-- > Parameter TMPDIR set to xst/projnav.tmp

Total REAL time to Xst completion: 1.00 secs
Total CPU time to Xst completion: 0.25 secs

-- > Parameter xsthdmdir set to xst

Total REAL time to Xst completion: 1.00 secs
Total CPU time to Xst completion: 0.25 secs

-- >
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```

- 8.4.2) Asynchronous Control Signals Information
- 8.4.3) Timing Summary
- 8.4.4) Timing Details
- 8.4.5) Cross Clock Domains [Report](#)

```
=====
* Synthesis Options Summary *
=====
--      -- Source Parameters
Input File Name : "alu_cla.prj"
Ignore Synthesis Constraint File : NO

--      -- Target Parameters
Output File Name : "alu_cla"
Output Format : NGC
Target Device : xc6slx4-3-tqg144

--      -- Source Options
Top Module Name : alu_cla
Automatic FSM Extraction : YES
FSM Encoding Algorithm : Auto
Safe Implementation : No
FSM Style : LUT
RAM Extraction : Yes
RAM Style : Auto
ROM Extraction : Yes
Shift Register Extraction : YES
ROM Style : Auto
Resource Sharing : YES
Asynchronous To Synchronous : NO
Shift Register Minimum Size : 2
Use DSP Block : Auto
Automatic Register Balancing : No

--      -- Target Options
LUT Combining : Auto
Reduce Control Sets : Auto
Add IO Buffers : YES
Global Maximum Fanout : 100000
Add Generic Clock Buffer( BUFG ) : 16
Register Duplication : YES
Optimize Instantiated Primitives : NO
Use Clock Enable : Auto
Use Synchronous Set : Auto
Use Synchronous Reset : Auto
Pack IO Registers into IOBs : Auto
Equivalent register Removal : YES

--      -- General Options
Optimization Goal : Speed
Optimization Effort : 1
Power Reduction : NO
Keep Hierarchy : No
Netlist Hierarchy : As_Optimized
RTL Output : Yes
Global Optimization : AllClockNets
Read Cores : YES
Write Timing Constraints : NO
Cross Clock Analysis : NO
```

Hierarchy Separator : /
Bus Delimiter : <>
Case Specifier : Maintain
Slice Utilization Ratio : 100
BRAM Utilization Ratio : 100
DSP48 Utilization Ratio : 100
Auto BRAM Packing : NO
Slice Utilization Ratio Delta : 5

=====

=====

* HDL Parsing *

=====

Parsing VHDL file "64210113\cla_gp.vhd" into library work
Parsing entity <cla_gp>.
Parsing architecture <ideal> of entity <cla_gp>.
Parsing VHDL file "64210113\cla_add_n_bit.vhd" into library work
Parsing entity <cla_add_n_bit>.
Parsing architecture <NDV> of entity <cla_add_n_bit>.
Parsing VHDL file "64210113\alu_cla.vhd" into library work
Parsing entity <alu_cla>.
Parsing architecture <NDV> of entity <alu_cla>.

=====

* HDL Elaboration *

=====

Elaborating entity <alu_cla> (architecture <NDV>) with generics from library <work>.

Elaborating entity <cla_add_n_bit> (architecture <NDV>) with generics from library <work>.

=====

* HDL Synthesis *

=====

Synthesizing Unit <alu_cla>.
Related source file is "64210113\alu_cla.vhd".
n = 8
Found 8-bit 12-to-1 multiplexer for signal <S> created at line 45.
Summary:
inferred 17 Multiplexer(s).
Unit <alu_cla> synthesized.

Synthesizing Unit <cla_add_n_bit>.
Related source file is "64210113\cla_add_n_bit.vhd".
n = 8
Summary:
Unit <cla_add_n_bit> synthesized.

=====

HDL Synthesis Report

Macro Statistics

Multiplexers : 17
1-bit 2-to-1 multiplexer : 10
8-bit 12-to-1 multiplexer : 1

```
8-bit 2-to-1 multiplexer : 6
# Xors : 17
1-bit xor2 : 16
8-bit xor2 : 1
```

=====

=====

* Advanced HDL Synthesis *

=====

=====

Advanced HDL Synthesis Report

Macro Statistics

```
# Multiplexers : 17
1-bit 2-to-1 multiplexer : 10
8-bit 12-to-1 multiplexer : 1
8-bit 2-to-1 multiplexer : 6
# Xors : 17
1-bit xor2 : 16
8-bit xor2 : 1
```

=====

=====

* Low Level Synthesis *

=====

Optimizing unit <alu_cla> ...

Optimizing unit <cla_add_n_bit> ...

Mapping all equations...

Building and optimizing final netlist ...

Found area constraint ratio of 100 (+ 5) on block alu_cla, actual ratio is 3.

Final Macro Processing ...

=====

Final Register Report

Found no macro

=====

=====

* Partition Report *

=====

Partition Implementation Status

```
--      --      --      --      --      --      --      --      --      --      --      --
--      --      --      --      --      --      --      --      --      --      --      --
```

No Partitions were found in this design.

```
--      --      --      --      --      --      --      --      --      --      --      --
--      --      --      --      --      --      --      --      --      --      --      --
```

=====

* Design Summary *

=====

Top Level Output File Name : alu_cla.ngc

Primitive and Black Box Usage:

```
--      --      --      --      --      --      --      --      --      --      --      --
--      --      --
# BELS : 60
# LUT3 : 4
# LUT5 : 14
# LUT6 : 41
# MUXF7 : 1
# IO Buffers : 34
# IBUF : 20
# OBUF : 14
```

Device utilization summary:

```
--      --      --      --      --      --      --      --      --      --      --      --
-
```

Selected Device : 6slx4tqg144-3

Slice Logic Utilization:

Number of Slice LUTs: 59 out of 2400 2%
Number used as Logic: 59 out of 2400 2%

Slice Logic Distribution:

Number of LUT Flip Flop pairs used: 59
Number with an unused Flip Flop: 59 out of 59 100%
Number with an unused LUT: 0 out of 59 0%
Number of fully used LUT-FF pairs: 0 out of 59 0%
Number of unique control sets: 0

IO Utilization:

Number of IOs: 34
Number of bonded IOBs: 34 out of 102 33%

Specific Feature Utilization:

```
--      --      --      --      --      --      --      --      --      --      --      --
-
```

Partition Resource Summary:

```
--      --      --      --      --      --      --      --      --      --      --      --
-
```

No Partitions were found in this design.

```
--      --      --      --      --      --      --      --      --      --      --      --
-
```

=====

Timing Report

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.
FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT
GENERATED AFTER PLACE-and-ROUTE.

Clock Information:

```

--      --      --      --      --      --      --      --      --
No clock signals found in this design

Asynchronous Control Signals Information:
--      --      --      --      --      --      --      --      --
--      --      --      --      --      --      --      --      --
No asynchronous control signals found in this design

Timing Summary:
--      --      --      --      --      --      --      --
Speed Grade: -3

Minimum period: No path found
Minimum input arrival time before clock: No path found
Maximum output required time after clock: No path found
Maximum combinational path delay: 11.168ns

Timing Details:
--      --      --      --      --      --      --      --
All values displayed in nanoseconds ( ns )

=====
Timing constraint: Default path analysis
Total number of paths / destination ports: 1146 / 14
--      --      --      --      --      --      --      --      --
--      --      --      --      --      --      --      --      --
--      --      --      --      --      --      --      --      --
Delay: 11.168ns ( Levels of Logic = 8 )
Source: F<2> ( PAD )
Destination: Negative ( PAD )

Data Path: F<2> to Negative
Gate Net
Cell:in->out fanout Delay Delay Logical Name ( Net Name )
--      --      --      --      --      --      --      --      --
--      --      --      --      --      --      --      --      --
--      --      --      --      --      --      --      --      --
IBUF:I->O 35 1.222 1.679 F_2_IBUF ( F_2_IBUF )
LUT6:I1->O 6 0.203 0.973 Mmux_Y_sig31 ( Y_sig<1> )
LUT5:I2->O 4 0.205 1.028 U1/C<3>2 ( U1/C<3> )
LUT6:I1->O 1 0.203 0.000 U1/C<6>_G ( N16 )
MUXF7:I1->O 5 0.140 0.943 U1/C<6> ( U1/C<6> )
LUT5:I2->O 3 0.205 1.015 U1/Mxor_S_sig<7>_xo<0>1 ( S_sig<7> )
LUT6:I0->O 1 0.203 0.579 Mmux_Negative1 ( Negative_OBUF )
OBUF:I->O 2.571 Negative_OBUF ( Negative )
--      --      --      --      --      --      --      --      --
--      --      --      --      --      --      --      --      --
Total 11.168ns ( 4.952ns logic, 6.216ns route )
( 44.3% logic, 55.7% route )

=====

Cross Clock Domains Report:
--      --      --      --      --      --      --      --      --
--      --      --      --      --      --      --      --      --
=====

Total REAL time to Xst completion: 11.00 secs
Total CPU time to Xst completion: 10.12 secs

```


-- >

Total memory usage is 4487500 kilobytes

Number of errors : 0 (0 filtered)

Number of warnings : 0 (0 filtered)

Number of infos : 0 (0 filtered)

64210113>fuse -incremental -o alu_cla_tb_isim_beh.exe -prj alu_cla_tb.prj -top alu_cla_tb

Running: \unwrapped\fuse.exe -incremental -o alu_cla_tb_isim_beh.exe -prj alu_cla_tb.prj -top alu_cla_tb

ISim P.20131013 (signature 0x7708f090)

Number of CPUs detected in this system: 8

Turning on mult-threading, number of parallel sub-compilation jobs: 16

Determining compilation order of HDL files

Parsing VHDL file "cla_gp.vhd" into library work

Parsing VHDL file "cla_add_n_bit.vhd" into library work

Parsing VHDL file "alu_cla.vhd" into library work

Parsing VHDL file "alu_cla_tb_IDEAL.vhd" into library work

Starting static elaboration

Completed static elaboration

Compiling package standard

Compiling package std_logic_1164

Compiling package textio

Compiling package std_logic_textio

Compiling package numeric_std

Compiling package attributes

Compiling package std_logic_misc

Compiling architecture ndv of entity cla_add_n_bit [\cla_add_n_bit(8)\]

Compiling architecture ndv of entity alu_cla [\alu_cla(8)\]

Compiling architecture testbench_arch of entity alu_cla_tb

Time Resolution for simulation is 1ps.

Compiled 12 VHDL Units

Built simulation executable alu_cla_tb_isim_beh.exe

Fuse Memory Usage: 37736 KB

Fuse CPU Usage: 1046 ms

64210113>alu_cla_tb_isim_beh.exe -tclbatch isim.tcl -wdb alu_cla_tb_isim_beh.wdb

ISim P.20131013 (signature 0x7708f090)

WARNING: A WEBPACK license was found.

WARNING: Please use Xilinx License Configuration Manager to check out a full ISim license.

WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for more information on the differences between the Lite and the Full version.

This is a Lite version of ISim.

Time resolution is 1 ps

Simulator is doing circuit initialization process.

Finished circuit initialization process.

at 7864320 ns, Instance /alu_cla_tb/ : Warning: NUMERIC_STD.TO_UNSIGNED: vector truncated

at 8847360 ns, Instance /alu_cla_tb/ : Warning: NUMERIC_STD.TO_UNSIGNED: vector truncated

at 9830400 ns, Instance /alu_cla_tb/ : Warning: NUMERIC_STD.TO_UNSIGNED: vector truncated

at 10813440 ns, Instance /alu_cla_tb/ : Warning: NUMERIC_STD.TO_UNSIGNED: vector truncated

at 11796480 ns, Instance /alu_cla_tb/ : Warning: NUMERIC_STD.TO_UNSIGNED: vector truncated
at 12779520 ns, Instance /alu_cla_tb/ : Warning: NUMERIC_STD.TO_UNSIGNED: vector truncated
at 13762560 ns, Instance /alu_cla_tb/ : Warning: NUMERIC_STD.TO_UNSIGNED: vector truncated
at 14745600 ns, Instance /alu_cla_tb/ : Warning: NUMERIC_STD.TO_UNSIGNED: vector truncated

64210113>rem ***** test alu flags

64210113>xst -ifn alu_cla_flags.xst
Release 14.7 - xst P.20131013 (nt64)
Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.
-- > Parameter TMPDIR set to xst/projnav.tmp

Total REAL time to Xst completion: 1.00 secs
Total CPU time to Xst completion: 0.35 secs

-- > Parameter xsthdpdir set to xst

Total REAL time to Xst completion: 1.00 secs
Total CPU time to Xst completion: 0.35 secs

-- >

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=====
* Synthesis Options Summary *

=====

-- -- Source Parameters

Input File Name : "alu_cla_flags_tb.prj"
Ignore Synthesis Constraint File : NO

-- -- Target Parameters

Output File Name : "alu_cla_flags_tb"
Output Format : NGC
Target Device : xc6slx4-3-tqg144

-- -- Source Options

Top Module Name : alu_cla_flags_tb
Automatic FSM Extraction : YES
FSM Encoding Algorithm : Auto
Safe Implementation : No
FSM Style : LUT
RAM Extraction : Yes
RAM Style : Auto
ROM Extraction : Yes
Shift Register Extraction : YES
ROM Style : Auto
Resource Sharing : YES
Asynchronous To Synchronous : NO
Shift Register Minimum Size : 2
Use DSP Block : Auto
Automatic Register Balancing : No

-- -- Target Options

LUT Combining : Auto
Reduce Control Sets : Auto
Add IO Buffers : YES
Global Maximum Fanout : 100000
Add Generic Clock Buffer(BUFG) : 16
Register Duplication : YES
Optimize Instantiated Primitives : NO
Use Clock Enable : Auto
Use Synchronous Set : Auto
Use Synchronous Reset : Auto
Pack IO Registers into IOBs : Auto
Equivalent register Removal : YES

-- -- General Options

Optimization Goal : Speed
Optimization Effort : 1
Power Reduction : NO
Keep Hierarchy : No
Netlist Hierarchy : As_Optimized
RTL Output : Yes
Global Optimization : AllClockNets
Read Cores : YES
Write Timing Constraints : NO
Cross Clock Analysis : NO
Hierarchy Separator : /
Bus Delimiter : <>
Case Specifier : Maintain
Slice Utilization Ratio : 100
BRAM Utilization Ratio : 100
DSP48 Utilization Ratio : 100
Auto BRAM Packing : NO
Slice Utilization Ratio Delta : 5

=====

=====

* HDL Parsing *

=====

Parsing VHDL file "64210113\cla_gp.vhd" into library work
Parsing entity <cla_gp>.
Parsing architecture <ideal> of entity <cla_gp>.
Parsing VHDL file "64210113\cla_add_n_bit.vhd" into library work

```

Parsing entity <cla_add_n_bit>.
Parsing architecture <NDV> of entity <cla_add_n_bit>.
Parsing VHDL file "64210113\alu_cla.vhd" into library work
Parsing entity <alu_cla>.
Parsing architecture <NDV> of entity <alu_cla>.
Parsing VHDL file "64210113\alu_cla_tb_FLAGS_IDEAL.vhd" into library work
Parsing entity <alu_cla_flags_tb>.
Parsing architecture <test_alu_flags> of entity <alu_cla_flags_tb>.

=====
* HDL Elaboration *
=====

Elaborating entity <alu_cla_flags_tb> ( architecture <test_alu_flags> ) with
generics from library <work>.

Elaborating entity <alu_cla> ( architecture <NDV> ) with generics from library
<work>.

Elaborating entity <cla_add_n_bit> ( architecture <NDV> ) with generics from
library <work>.
ERROR:HDLCompiler:890 - "64210113\alu_cla_tb_FLAGS_IDEAL.vhd" Line 144: wait
statement without UNTIL clause not supported for synthesis
Netlist alu_cla_flags_tb( 8 )( test_alu_flags ) remains a blackbox, due to errors
in its contents
-- >

Total memory usage is 4466680 kilobytes

Number of errors : 1 ( 0 filtered )
Number of warnings : 0 ( 0 filtered )
Number of infos : 0 ( 0 filtered )

64210113>fuse -incremental -o alu_cla_flags_tb_isim_beh.exe -prj
alu_cla_flags_tb.prj -top alu_cla_flags_tb
Running: \unwrapped\fuse.exe -incremental -o alu_cla_flags_tb_isim_beh.exe -prj
alu_cla_flags_tb.prj -top alu_cla_flags_tb
ISim P.20131013 ( signature 0x7708f090 )
Number of CPUs detected in this system: 8
Turning on mult-threading, number of parallel sub-compilation jobs: 16
Determining compilation order of HDL files
Parsing VHDL file "cla_gp.vhd" into library work
Parsing VHDL file "cla_add_n_bit.vhd" into library work
Parsing VHDL file "alu_cla.vhd" into library work
Parsing VHDL file "alu_cla_tb_FLAGS_IDEAL.vhd" into library work
Starting static elaboration
Completed static elaboration
Compiling package standard
Compiling package std_logic_1164
Compiling package textio
Compiling package std_logic_textio
Compiling package numeric_std
Compiling package attributes
Compiling package std_logic_misc
Compiling architecture ndv of entity cla_add_n_bit [\cla_add_n_bit( 8 )\]
Compiling architecture ndv of entity alu_cla [\alu_cla( 8 )\]
Compiling architecture test_alu_flags of entity alu_cla_flags_tb
Time Resolution for simulation is 1ps.
Waiting for 1 sub-compilation( s ) to finish...

```

Compiled 12 VHDL Units
Built simulation executable alu_cla_flags_tb_isim_beh.exe
Fuse Memory Usage: 37664 KB
Fuse CPU Usage: 999 ms

```
64210113>alu_cla_flags_tb_isim_beh.exe -tclbatch isim.tcl -wdb
alu_cla_flags_tb_isim_beh.wdb
ISim P.20131013 ( signature 0x7708f090 )
WARNING: A WEBPACK license was found.
WARNING: Please use Xilinx License Configuration Manager to check out a full ISim
license.
WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for
more information on the differences between the Lite and the Full version.
This is a Lite version of ISim.
Time resolution is 1 ps
Simulator is doing circuit initialization process.
Finished circuit initialization process.
```

```
-- *****
-- **** STUDENT: 64210290
-- *****
-- KOMENTARJI K OCENI NALOGE
-- Matej Možek: Ni pripomb
-- *****
```

```
64210290>rem ***** test cla adder
```

```
64210290>if not exist "xst" mkdir xst
```

```
64210290>cd XST
```

```
64210290\xst>if not exist "projnav.tmp" mkdir "projnav.tmp"
```

```
64210290\xst>cd ..
```

```
64210290>rem ***** test cla operations
```

```
64210290>xst -ifn cla_add_n_bit.xst
Release 14.7 - xst P.20131013 ( nt64 )
Copyright ( c ) 1995-2013 Xilinx, Inc. All rights reserved.
-- > Parameter TMPDIR set to xst/projnav.tmp
```

```
Total REAL time to Xst completion: 1.00 secs
Total CPU time to Xst completion: 0.24 secs
```

```
-- > Parameter xsthdpdir set to xst
```

```
Total REAL time to Xst completion: 1.00 secs
Total CPU time to Xst completion: 0.24 secs
```

```
-- >
```

```
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```
=====
* Synthesis Options Summary *
```

```
=====
-- -- Source Parameters
```

```
Input File Name : "cla_add_n_bit.prj"
```

Ignore Synthesis Constraint File : NO

-- -- Target Parameters

Output File Name : "cla_add_n_bit"

Output Format : NGC

Target Device : xc6slx4-3-tqg144

-- -- Source Options

Top Module Name : cla_add_n_bit

Automatic FSM Extraction : YES

FSM Encoding Algorithm : Auto

Safe Implementation : No

FSM Style : LUT

RAM Extraction : Yes

RAM Style : Auto

ROM Extraction : Yes

Shift Register Extraction : YES

ROM Style : Auto

Resource Sharing : YES

Asynchronous To Synchronous : NO

Shift Register Minimum Size : 2

Use DSP Block : Auto

Automatic Register Balancing : No

-- -- Target Options

LUT Combining : Auto

Reduce Control Sets : Auto

Add IO Buffers : YES

Global Maximum Fanout : 100000

Add Generic Clock Buffer(BUFG) : 16

Register Duplication : YES

Optimize Instantiated Primitives : NO

Use Clock Enable : Auto

Use Synchronous Set : Auto

Use Synchronous Reset : Auto

Pack IO Registers into IOBs : Auto

Equivalent register Removal : YES

-- -- General Options

Optimization Goal : Speed

Optimization Effort : 1

Power Reduction : NO

Keep Hierarchy : No

Netlist Hierarchy : As_Optimized

RTL Output : Yes

Global Optimization : AllClockNets

Read Cores : YES

Write Timing Constraints : NO

Cross Clock Analysis : NO

Hierarchy Separator : /

Bus Delimiter : <>

Case Specifier : Maintain

Slice Utilization Ratio : 100

BRAM Utilization Ratio : 100

DSP48 Utilization Ratio : 100

Auto BRAM Packing : NO

Slice Utilization Ratio Delta : 5

=====

```

=====
* HDL Parsing *
=====
Parsing VHDL file "64210290\cla_gp.vhd" into library work
Parsing entity <cla_gp>.
Parsing architecture <ideal> of entity <cla_gp>.
Parsing VHDL file "64210290\cla_add_n_bit.vhd" into library work
Parsing entity <cla_add_n_bit>.
Parsing architecture <NDV> of entity <cla_add_n_bit>.

=====
* HDL Elaboration *
=====

Elaborating entity <cla_add_n_bit> ( architecture <NDV> ) with generics from
library <work>.

=====
* HDL Synthesis *
=====

Synthesizing Unit <cla_add_n_bit>.
Related source file is "64210290\cla_add_n_bit.vhd".
n = 8
Summary:
Unit <cla_add_n_bit> synthesized.

=====
HDL Synthesis Report

Macro Statistics
# Xors : 16
1-bit xor2 : 16

=====

=====
* Advanced HDL Synthesis *
=====

=====
Advanced HDL Synthesis Report

Macro Statistics
# Xors : 16
1-bit xor2 : 16

=====

=====
* Low Level Synthesis *
=====

Optimizing unit <cla_add_n_bit> ...

Mapping all equations...
Building and optimizing final netlist ...

```


Found area constraint ratio of 100 (+ 5) on block cla_add_n_bit, actual ratio is 1.

Final Macro Processing ...

=====
Final Register Report

Found no macro

=====
* Partition Report *
=====

Partition Implementation Status

-- -- -- -- -- -- -- -- -- -- -- -- -- --
-- -- --

No Partitions were found in this design.

-- -- -- -- -- -- -- -- -- -- -- -- -- --
-- -- --

=====
* Design Summary *
=====

Top Level Output File Name : cla_add_n_bit.ngc

Primitive and Black Box Usage:

-- -- -- -- -- -- -- -- -- -- -- -- -- --
-- -- --

BELS : 24
LUT2 : 6
LUT3 : 3
LUT5 : 6
LUT6 : 9
IO Buffers : 28
IBUF : 17
OBUF : 11

Device utilization summary:

-- -- -- -- -- -- -- -- -- -- -- -- -- --
-

Selected Device : 6slx4tqg144-3

Slice Logic Utilization:

Number of Slice LUTs: 24 out of 2400 1%
Number used as Logic: 24 out of 2400 1%

Slice Logic Distribution:

Number of LUT Flip Flop pairs used: 24
Number with an unused Flip Flop: 24 out of 24 100%
Number with an unused LUT: 0 out of 24 0%
Number of fully used LUT-FF pairs: 0 out of 24 0%
Number of unique control sets: 0

IO Utilization:

Number of IOs: 28

Number of bonded IOBs: 28 out of 102 27%

Specific Feature Utilization:

```
-- -- -- -- -- -- -- -- -- -- -- -- -- --  
-
```

Partition Resource Summary:

```
-- -- -- -- -- -- -- -- -- -- -- -- -- --  
-
```

No Partitions were found in this design.

```
-- -- -- -- -- -- -- -- -- -- -- -- -- --  
-
```

=====
Timing Report

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.

FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT
GENERATED AFTER PLACE-and-ROUTE.

Clock Information:

```
-- -- -- -- -- -- -- -- -- -- -- -- -- --  
No clock signals found in this design
```

Asynchronous Control Signals Information:

```
-- -- -- -- -- -- -- -- -- -- -- -- -- --  
-- -- -- -- -- -- -- -- -- -- -- -- -- --
```

No asynchronous control signals found in this design

Timing Summary:

```
-- -- -- -- -- -- -- -- -- -- -- -- -- --
```

Speed Grade: -3

Minimum period: No path found

Minimum input arrival time before clock: No path found

Maximum output required time after clock: No path found

Maximum combinational path delay: 9.101ns

Timing Details:

```
-- -- -- -- -- -- -- -- -- -- -- -- -- --
```

All values displayed in nanoseconds (ns)

=====
Timing constraint: Default path analysis

Total number of paths / destination ports: 131 / 11

```
-- -- -- -- -- -- -- -- -- -- -- -- -- --  
-- -- -- -- -- -- -- -- -- -- -- -- -- --  
-- -- -- -- -- -- -- -- -- -- -- -- -- --
```

Delay: 9.101ns (Levels of Logic = 7)

Source: Y<0> (PAD)

Destination: S<7> (PAD)

Data Path: Y<0> to S<7>

Gate Net

Cell:in->out fanout Delay Delay Logical Name (Net Name)

```

--      --      --      --      --      --      --      --      --      --      --
--      --      --      --      --      --      --      --      --      --      --
--      --
IBUF:I->0 6 1.222 0.973 Y_0_IBUF ( Y_0_IBUF )
LUT3:I0->0 2 0.205 0.617 C<3>_SW0 ( N2 )
LUT5:I4->0 3 0.205 0.651 C<3> ( C<3> )
LUT3:I2->0 2 0.205 0.617 C<6>_SW0 ( N4 )
LUT5:I4->0 2 0.205 0.845 C<6> ( C<6> )
LUT5:I2->0 1 0.205 0.579 Mxor_S_sig<7>_xo<0>1 ( S_7_OBUF )
OBUF:I->0 2.571 S_7_OBUF ( S<7> )
--      --      --      --      --      --      --      --      --      --      --
--      --      --      --      --      --      --      --      --      --      --
Total 9.101ns ( 4.818ns logic, 4.283ns route )
( 52.9% logic, 47.1% route )
=====

```

Cross Clock Domains Report:

```

--      --      --      --      --      --      --      --      --      --      --
=====

```

Total REAL time to Xst completion: 10.00 secs
Total CPU time to Xst completion: 9.28 secs

-- >

Total memory usage is 4487500 kilobytes

Number of errors : 0 (0 filtered)

Number of warnings : 0 (0 filtered)

Number of infos : 0 (0 filtered)

```

64210290>fuse -incremental -o cla_add_n_bit_tb_isim_beh.exe -prj
cla_add_n_bit_tb.prj -top cla_add_n_bit_tb
Running: \unwrapped\fuse.exe -incremental -o cla_add_n_bit_tb_isim_beh.exe -prj
cla_add_n_bit_tb.prj -top cla_add_n_bit_tb
ISim P.20131013 ( signature 0x7708f090 )
Number of CPUs detected in this system: 8
Turning on mult-threading, number of parallel sub-compilation jobs: 16
Determining compilation order of HDL files
Parsing VHDL file "cla_gp.vhd" into library work
Parsing VHDL file "cla_add_n_bit.vhd" into library work
Parsing VHDL file "cla_add_n_bit_tb_IDEAL.vhd" into library work
Starting static elaboration
Completed static elaboration
Compiling package standard
Compiling package std_logic_1164
Compiling package textio
Compiling package std_logic_textio
Compiling package numeric_std
Compiling package attributes
Compiling package std_logic_misc
Compiling architecture ndv of entity cla_add_n_bit [\cla_add_n_bit( 8 )\]
Compiling architecture testbench_arch of entity cla_add_n_bit_tb
Time Resolution for simulation is 1ps.
Waiting for 1 sub-compilation( s ) to finish...
Compiled 10 VHDL Units
Built simulation executable cla_add_n_bit_tb_isim_beh.exe

```

Fuse Memory Usage: 37380 KB
Fuse CPU Usage: 937 ms

```
64210290>cla_add_n_bit_tb_isim_beh.exe -tclbatch isim.tcl -wdb
cla_add_n_bit_tb_isim_beh.wdb
ISim P.20131013 ( signature 0x7708f090 )
WARNING: A WEBPACK license was found.
WARNING: Please use Xilinx License Configuration Manager to check out a full ISim
license.
WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for
more information on the differences between the Lite and the Full version.
This is a Lite version of ISim.
Time resolution is 1 ps
Simulator is doing circuit initialization process.
Finished circuit initialization process.
```

```
64210290>rem ***** test cla flags
```

```
64210290>xst -ifn cla_add_n_bit_flags.xst
Release 14.7 - xst P.20131013 ( nt64 )
Copyright ( c ) 1995-2013 Xilinx, Inc. All rights reserved.
-- > Parameter TMPDIR set to xst/projnav.tmp
```

Total REAL time to Xst completion: 1.00 secs
Total CPU time to Xst completion: 0.23 secs

```
-- > Parameter xsthdpdir set to xst
```

Total REAL time to Xst completion: 1.00 secs
Total CPU time to Xst completion: 0.24 secs

```
-- > ERROR:Xst:438 - Can not open file : cla_add_n_bit_flags.prj
```

Total REAL time to Xst completion: 1.00 secs
Total CPU time to Xst completion: 0.26 secs

```
-- >
```

Total memory usage is 4422880 kilobytes

Number of errors : 1 (0 filtered)
Number of warnings : 0 (0 filtered)
Number of infos : 0 (0 filtered)

```
64210290>fuse -incremental -o cla_add_n_bit_tb_flags_isim_beh.exe -prj
cla_add_n_bit_flags_tb.prj -top cla_add_n_bit_flags_tb_IDEAL
Running: \unwrapped\fuse.exe -incremental -o cla_add_n_bit_tb_flags_isim_beh.exe -
prj cla_add_n_bit_flags_tb.prj -top cla_add_n_bit_flags_tb_IDEAL
ISim P.20131013 ( signature 0x7708f090 )
Number of CPUs detected in this system: 8
Turning on mult-threading, number of parallel sub-compilation jobs: 16
Determining compilation order of HDL files
Parsing VHDL file "cla_gp.vhd" into library work
Parsing VHDL file "cla_add_n_bit.vhd" into library work
Parsing VHDL file "cla_add_n_bit_flags_tb_IDEAL.vhd" into library work
Starting static elaboration
Completed static elaboration
Compiling package standard
Compiling package std_logic_1164
```

```

Compiling package textio
Compiling package std_logic_textio
Compiling package numeric_std
Compiling package attributes
Compiling package std_logic_misc
Compiling architecture ndv of entity cla_add_n_bit [\cla_add_n_bit( 8 )\]
Compiling architecture a1 of entity cla_add_n_bit_flags_tb_ideal
Time Resolution for simulation is 1ps.
Waiting for 1 sub-compilation( s ) to finish...
Compiled 10 VHDL Units
Built simulation executable cla_add_n_bit_tb_flags_isim_beh.exe
Fuse Memory Usage: 37504 KB
Fuse CPU Usage: 983 ms

64210290>cla_add_n_bit_tb_flags_isim_beh.exe -tclbatch isim.tcl -wdb
cla_add_n_bit_flags_tb.wdb
ISim P.20131013 ( signature 0x7708f090 )
WARNING: A WEBPACK license was found.
WARNING: Please use Xilinx License Configuration Manager to check out a full ISim
license.
WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for
more information on the differences between the Lite and the Full version.
This is a Lite version of ISim.
Time resolution is 1 ps
Simulator is doing circuit initialization process.
Finished circuit initialization process.

64210290>rem ***** test alu operations

64210290>xst -ifn alu_cla.xst
Release 14.7 - xst P.20131013 ( nt64 )
Copyright ( c ) 1995-2013 Xilinx, Inc. All rights reserved.
-- > Parameter TMPDIR set to xst/projnav.tmp

Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.24 secs

-- > Parameter xsthdpdir set to xst

Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.24 secs

-- >
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8.4.1 ) Clock Information

```

- 8.4.2) Asynchronous Control Signals Information
- 8.4.3) Timing Summary
- 8.4.4) Timing Details
- 8.4.5) Cross Clock Domains [Report](#)

```
=====
* Synthesis Options Summary *
=====
--      -- Source Parameters
Input File Name : "alu_cla.prj"
Ignore Synthesis Constraint File : NO

--      -- Target Parameters
Output File Name : "alu_cla"
Output Format : NGC
Target Device : xc6slx4-3-tqg144

--      -- Source Options
Top Module Name : alu_cla
Automatic FSM Extraction : YES
FSM Encoding Algorithm : Auto
Safe Implementation : No
FSM Style : LUT
RAM Extraction : Yes
RAM Style : Auto
ROM Extraction : Yes
Shift Register Extraction : YES
ROM Style : Auto
Resource Sharing : YES
Asynchronous To Synchronous : NO
Shift Register Minimum Size : 2
Use DSP Block : Auto
Automatic Register Balancing : No

--      -- Target Options
LUT Combining : Auto
Reduce Control Sets : Auto
Add IO Buffers : YES
Global Maximum Fanout : 100000
Add Generic Clock Buffer( BUFG ) : 16
Register Duplication : YES
Optimize Instantiated Primitives : NO
Use Clock Enable : Auto
Use Synchronous Set : Auto
Use Synchronous Reset : Auto
Pack IO Registers into IOBs : Auto
Equivalent register Removal : YES

--      -- General Options
Optimization Goal : Speed
Optimization Effort : 1
Power Reduction : NO
Keep Hierarchy : No
Netlist Hierarchy : As_Optimized
RTL Output : Yes
Global Optimization : AllClockNets
Read Cores : YES
Write Timing Constraints : NO
Cross Clock Analysis : NO
```

Hierarchy Separator : /
Bus Delimiter : <>
Case Specifier : Maintain
Slice Utilization Ratio : 100
BRAM Utilization Ratio : 100
DSP48 Utilization Ratio : 100
Auto BRAM Packing : NO
Slice Utilization Ratio Delta : 5

=====

=====

* HDL Parsing *

=====

Parsing VHDL file "64210290\cla_gp.vhd" into library work
Parsing entity <cla_gp>.
Parsing architecture <ideal> of entity <cla_gp>.
Parsing VHDL file "64210290\cla_add_n_bit.vhd" into library work
Parsing entity <cla_add_n_bit>.
Parsing architecture <NDV> of entity <cla_add_n_bit>.
Parsing VHDL file "64210290\alu_cla.vhd" into library work
Parsing entity <alu_cla>.
Parsing architecture <NDV> of entity <alu_cla>.

=====

* HDL Elaboration *

=====

Elaborating entity <alu_cla> (architecture <NDV>) with generics from library <work>.

Elaborating entity <cla_add_n_bit> (architecture <NDV>) with generics from library <work>.

=====

* HDL Synthesis *

=====

Synthesizing Unit <alu_cla>.
Related source file is "64210290\alu_cla.vhd".
n = 8
Found 8-bit 12-to-1 multiplexer for signal <S> created at line 58.
Summary:
inferred 19 Multiplexer(s).
Unit <alu_cla> synthesized.

Synthesizing Unit <cla_add_n_bit>.
Related source file is "64210290\cla_add_n_bit.vhd".
n = 8
Summary:
Unit <cla_add_n_bit> synthesized.

=====

HDL Synthesis Report

Macro Statistics

Multiplexers : 19
1-bit 2-to-1 multiplexer : 12
8-bit 12-to-1 multiplexer : 1

```
8-bit 2-to-1 multiplexer : 6
# Xors : 17
1-bit xor2 : 16
8-bit xor2 : 1
```

=====

=====

* Advanced HDL Synthesis *

=====

=====

Advanced HDL Synthesis Report

Macro Statistics

```
# Multiplexers : 19
1-bit 2-to-1 multiplexer : 12
8-bit 12-to-1 multiplexer : 1
8-bit 2-to-1 multiplexer : 6
# Xors : 17
1-bit xor2 : 16
8-bit xor2 : 1
```

=====

=====

* Low Level Synthesis *

=====

Optimizing unit <alu_cla> ...

Optimizing unit <cla_add_n_bit> ...

Mapping all equations...

Building and optimizing final netlist ...

Found area constraint ratio of 100 (+ 5) on block alu_cla, actual ratio is 4.

Final Macro Processing ...

=====

Final Register Report

Found no macro

=====

=====

* Partition Report *

=====

Partition Implementation Status

```
--      --      --      --      --      --      --      --      --      --      --      --
--      --      --      --      --      --      --      --      --      --      --      --
```

No Partitions were found in this design.

```
--      --      --      --      --      --      --      --      --      --      --      --
--      --      --      --      --      --      --      --      --      --      --      --
```

=====

* Design Summary *

=====

Top Level Output File Name : alu_cla.ngc

Primitive and Black Box Usage:

```
--      --      --      --      --      --      --      --      --      --      --      --
--      --      --
# BELS : 59
# LUT3 : 3
# LUT5 : 15
# LUT6 : 40
# MUXF7 : 1
# IO Buffers : 34
# IBUF : 20
# OBUF : 14
```

Device utilization summary:

```
--      --      --      --      --      --      --      --      --      --      --      --
-
```

Selected Device : 6slx4tqg144-3

Slice Logic Utilization:

Number of Slice LUTs: 58 out of 2400 2%
Number used as Logic: 58 out of 2400 2%

Slice Logic Distribution:

Number of LUT Flip Flop pairs used: 58
Number with an unused Flip Flop: 58 out of 58 100%
Number with an unused LUT: 0 out of 58 0%
Number of fully used LUT-FF pairs: 0 out of 58 0%
Number of unique control sets: 0

IO Utilization:

Number of IOs: 34
Number of bonded IOBs: 34 out of 102 33%

Specific Feature Utilization:

```
--      --      --      --      --      --      --      --      --      --      --      --
-
```

Partition Resource Summary:

```
--      --      --      --      --      --      --      --      --      --      --      --
-
```

No Partitions were found in this design.

```
--      --      --      --      --      --      --      --      --      --      --      --
-
```

=====

Timing Report

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.
FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT
GENERATED AFTER PLACE-and-ROUTE.

Clock Information:

```

--      --      --      --      --      --      --      --      --
No clock signals found in this design

Asynchronous Control Signals Information:
--      --      --      --      --      --      --      --      --
--      --      --      --      --      --      --      --      --
No asynchronous control signals found in this design

Timing Summary:
--      --      --      --      --      --      --      --
Speed Grade: -3

Minimum period: No path found
Minimum input arrival time before clock: No path found
Maximum output required time after clock: No path found
Maximum combinational path delay: 11.892ns

Timing Details:
--      --      --      --      --      --      --      --
All values displayed in nanoseconds ( ns )

=====
Timing constraint: Default path analysis
Total number of paths / destination ports: 1241 / 14
--      --      --      --      --      --      --      --      --
--      --      --      --      --      --      --      --      --
--      --      --      --      --      --      --      --      --
Delay: 11.892ns ( Levels of Logic = 9 )
Source: M ( PAD )
Destination: Overflow ( PAD )

Data Path: M to Overflow
Gate Net
Cell:in->out fanout Delay Delay Logical Name ( Net Name )
--      --      --      --      --      --      --      --      --
--      --      --      --      --      --      --      --      --
--      --      --      --      --      --      --      --      --
IBUF:I->O 27 1.222 1.585 M_IBUF ( M_IBUF )
LUT6:I0->O 6 0.203 0.973 Y_sig<1>1 ( Y_sig<1> )
LUT5:I2->O 4 0.205 1.028 U1/C<3>2 ( U1/C<3> )
LUT6:I1->O 1 0.203 0.000 U1/C<6>_G ( N14 )
MUXF7:I1->O 4 0.140 0.912 U1/C<6> ( U1/C<6> )
LUT5:I2->O 5 0.205 1.079 U1/Mxor_S_sig<7>_xo<0>1 ( S_sig<7> )
LUT6:I0->O 1 0.203 0.580 Overflow11 ( Overflow1 )
LUT5:I4->O 1 0.205 0.579 Overflow12 ( Overflow_OBUF )
OBUF:I->O 2.571 Overflow_OBUF ( Overflow )
--      --      --      --      --      --      --      --      --
--      --      --      --      --      --      --      --      --
Total 11.892ns ( 5.157ns logic, 6.735ns route )
( 43.4% logic, 56.6% route )

=====

Cross Clock Domains Report:
--      --      --      --      --      --      --      --      --
--      --      --      --      --      --      --      --      --
=====

Total REAL time to Xst completion: 9.00 secs

```

Total CPU time to Xst completion: 9.68 secs

-- >

Total memory usage is 4487500 kilobytes

Number of errors : 0 (0 filtered)

Number of warnings : 0 (0 filtered)

Number of infos : 0 (0 filtered)

64210290>fuse -incremental -o alu_cla_tb_isim_beh.exe -prj alu_cla_tb.prj -top alu_cla_tb

Running: \unwrapped\fuse.exe -incremental -o alu_cla_tb_isim_beh.exe -prj alu_cla_tb.prj -top alu_cla_tb

ISim P.20131013 (signature 0x7708f090)

Number of CPUs detected in this system: 8

Turning on mult-threading, number of parallel sub-compilation jobs: 16

Determining compilation order of HDL files

Parsing VHDL file "cla_gp.vhd" into library work

Parsing VHDL file "cla_add_n_bit.vhd" into library work

Parsing VHDL file "alu_cla.vhd" into library work

Parsing VHDL file "alu_cla_tb_IDEAL.vhd" into library work

Starting static elaboration

Completed static elaboration

Compiling package standard

Compiling package std_logic_1164

Compiling package textio

Compiling package std_logic_textio

Compiling package numeric_std

Compiling package attributes

Compiling package std_logic_misc

Compiling architecture ndv of entity cla_add_n_bit [\cla_add_n_bit(8)\]

Compiling architecture ndv of entity alu_cla [\alu_cla(8)\]

Compiling architecture testbench_arch of entity alu_cla_tb

Time Resolution for simulation is 1ps.

Waiting for 1 sub-compilation(s) to finish...

Compiled 12 VHDL Units

Built simulation executable alu_cla_tb_isim_beh.exe

Fuse Memory Usage: 37752 KB

Fuse CPU Usage: 937 ms

64210290>alu_cla_tb_isim_beh.exe -tclbatch isim.tcl -wdb alu_cla_tb_isim_beh.wdb

ISim P.20131013 (signature 0x7708f090)

WARNING: A WEBPACK license was found.

WARNING: Please use Xilinx License Configuration Manager to check out a full ISim license.

WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for more information on the differences between the Lite and the Full version.

This is a Lite version of ISim.

Time resolution is 1 ps

Simulator is doing circuit initialization process.

Finished circuit initialization process.

at 5898270 ns, Instance /alu_cla_tb/ : Warning: NUMERIC_STD.TO_UNSIGNED: vector truncated

at 6881310 ns, Instance /alu_cla_tb/ : Warning: NUMERIC_STD.TO_UNSIGNED: vector truncated

at 7864350 ns, Instance /alu_cla_tb/ : Warning: NUMERIC_STD.TO_UNSIGNED: vector truncated

at 8847390 ns, Instance /alu_cla_tb/ : Warning: NUMERIC_STD.TO_UNSIGNED: vector truncated
at 9830430 ns, Instance /alu_cla_tb/ : Warning: NUMERIC_STD.TO_UNSIGNED: vector truncated
at 10813470 ns, Instance /alu_cla_tb/ : Warning: NUMERIC_STD.TO_UNSIGNED: vector truncated
at 11796510 ns, Instance /alu_cla_tb/ : Warning: NUMERIC_STD.TO_UNSIGNED: vector truncated
at 12779550 ns, Instance /alu_cla_tb/ : Warning: NUMERIC_STD.TO_UNSIGNED: vector truncated

64210290>rem ***** test alu flags

64210290>xst -ifn alu_cla_flags.xst
Release 14.7 - xst P.20131013 (nt64)
Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.
-- > Parameter TMPDIR set to xst/projnav.tmp

Total REAL time to Xst completion: 1.00 secs
Total CPU time to Xst completion: 0.25 secs

-- > Parameter xsthdpdir set to xst

Total REAL time to Xst completion: 1.00 secs
Total CPU time to Xst completion: 0.25 secs

-- >

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 - 8.4.5) Cross Clock Domains Report

=====
* Synthesis Options Summary *

-- -- Source Parameters

Input File Name : "alu_cla_flags_tb.prj"
Ignore Synthesis Constraint File : NO

-- -- Target Parameters

Output File Name : "alu_cla_flags_tb"
Output Format : NGC
Target Device : xc6slx4-3-tqg144

-- -- Source Options

Top Module Name : alu_cla_flags_tb
Automatic FSM Extraction : YES
FSM Encoding Algorithm : Auto
Safe Implementation : No
FSM Style : LUT
RAM Extraction : Yes
RAM Style : Auto
ROM Extraction : Yes
Shift Register Extraction : YES
ROM Style : Auto
Resource Sharing : YES
Asynchronous To Synchronous : NO
Shift Register Minimum Size : 2
Use DSP Block : Auto
Automatic Register Balancing : No

-- -- Target Options

LUT Combining : Auto
Reduce Control Sets : Auto
Add IO Buffers : YES
Global Maximum Fanout : 100000
Add Generic Clock Buffer(BUFG) : 16
Register Duplication : YES
Optimize Instantiated Primitives : NO
Use Clock Enable : Auto
Use Synchronous Set : Auto
Use Synchronous Reset : Auto
Pack IO Registers into IOBs : Auto
Equivalent register Removal : YES

-- -- General Options

Optimization Goal : Speed
Optimization Effort : 1
Power Reduction : NO
Keep Hierarchy : No
Netlist Hierarchy : As_Optimized
RTL Output : Yes
Global Optimization : AllClockNets
Read Cores : YES
Write Timing Constraints : NO
Cross Clock Analysis : NO
Hierarchy Separator : /
Bus Delimiter : <>
Case Specifier : Maintain
Slice Utilization Ratio : 100
BRAM Utilization Ratio : 100
DSP48 Utilization Ratio : 100
Auto BRAM Packing : NO
Slice Utilization Ratio Delta : 5

=====

=====

* HDL Parsing *

=====

Parsing VHDL file "64210290\cla_gp.vhd" into library work
Parsing entity <cla_gp>.

```

Parsing architecture <ideal> of entity <cla_gp>.
Parsing VHDL file "64210290\cla_add_n_bit.vhd" into library work
Parsing entity <cla_add_n_bit>.
Parsing architecture <NDV> of entity <cla_add_n_bit>.
Parsing VHDL file "64210290\alu_cla.vhd" into library work
Parsing entity <alu_cla>.
Parsing architecture <NDV> of entity <alu_cla>.
Parsing VHDL file "64210290\alu_cla_tb_FLAGS_IDEAL.vhd" into library work
Parsing entity <alu_cla_flags_tb>.
Parsing architecture <test_alu_flags> of entity <alu_cla_flags_tb>.

=====
* HDL Elaboration *
=====

Elaborating entity <alu_cla_flags_tb> ( architecture <test_alu_flags> ) with
generics from library <work>.

Elaborating entity <alu_cla> ( architecture <NDV> ) with generics from library
<work>.

Elaborating entity <cla_add_n_bit> ( architecture <NDV> ) with generics from
library <work>.
ERROR:HDLCompiler:890 - "64210290\alu_cla_tb_FLAGS_IDEAL.vhd" Line 144: wait
statement without UNTIL clause not supported for synthesis
Netlist alu_cla_flags_tb( 8 )( test_alu_flags ) remains a blackbox, due to errors
in its contents
-- >

Total memory usage is 4466680 kilobytes

Number of errors : 1 ( 0 filtered )
Number of warnings : 0 ( 0 filtered )
Number of infos : 0 ( 0 filtered )

64210290>fuse -incremental -o alu_cla_flags_tb_isim_beh.exe -prj
alu_cla_flags_tb.prj -top alu_cla_flags_tb
Running: \unwrapped\fuse.exe -incremental -o alu_cla_flags_tb_isim_beh.exe -prj
alu_cla_flags_tb.prj -top alu_cla_flags_tb
ISim P.20131013 ( signature 0x7708f090 )
Number of CPUs detected in this system: 8
Turning on mult-threading, number of parallel sub-compilation jobs: 16
Determining compilation order of HDL files
Parsing VHDL file "cla_gp.vhd" into library work
Parsing VHDL file "cla_add_n_bit.vhd" into library work
Parsing VHDL file "alu_cla.vhd" into library work
Parsing VHDL file "alu_cla_tb_FLAGS_IDEAL.vhd" into library work
Starting static elaboration
Completed static elaboration
Compiling package standard
Compiling package std_logic_1164
Compiling package textio
Compiling package std_logic_textio
Compiling package numeric_std
Compiling package attributes
Compiling package std_logic_misc
Compiling architecture ndv of entity cla_add_n_bit [\cla_add_n_bit( 8 )\]
Compiling architecture ndv of entity alu_cla [\alu_cla( 8 )\]
Compiling architecture test_alu_flags of entity alu_cla_flags_tb

```

Time Resolution for simulation is 1ps.
Waiting for 1 sub-compilation(s) to finish...
Compiled 12 VHDL Units
Built simulation executable alu_cla_flags_tb_isim_beh.exe
Fuse Memory Usage: 37728 KB
Fuse CPU Usage: 968 ms

64210290>alu_cla_flags_tb_isim_beh.exe -tclbatch isim.tcl -wdb
alu_cla_flags_tb_isim_beh.wdb
ISim P.20131013 (signature 0x7708f090)
WARNING: A WEBPACK license was found.
WARNING: Please use Xilinx License Configuration Manager to check out a full ISim license.
WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for more information on the differences between the Lite and the Full version.
This is a Lite version of ISim.
Time resolution is 1 ps
Simulator is doing circuit initialization process.
Finished circuit initialization process.

```
-- *****
-- **** STUDENT: 64210382
-- *****
-- KOMENTARJI K OCENI NALOGE
-- Matej Možek: Ni pripomb
-- *****
```

```
64210382>rem ***** test cla adder
```

```
64210382>if not exist "xst" mkdir xst
```

```
64210382>cd XST
```

```
64210382\xst>if not exist "projnav.tmp" mkdir "projnav.tmp"
```

```
64210382\xst>cd ..
```

```
64210382>rem ***** test cla operations
```

```
64210382>xst -ifn cla_add_n_bit.xst
Release 14.7 - xst P.20131013 ( nt64 )
Copyright ( c ) 1995-2013 Xilinx, Inc. All rights reserved.
-- > Parameter TMPDIR set to xst/projnav.tmp
```

```
Total REAL time to Xst completion: 1.00 secs
Total CPU time to Xst completion: 0.25 secs
```

```
-- > Parameter xsthdpdir set to xst
```

```
Total REAL time to Xst completion: 1.00 secs
Total CPU time to Xst completion: 0.26 secs
```

```
-- >
```

```
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```
=====
* Synthesis Options Summary *
=====
```

```
-- -- Source Parameters
```

```
Input File Name : "cla_add_n_bit.prj"
```


Ignore Synthesis Constraint File : NO

-- -- Target Parameters

Output File Name : "cla_add_n_bit"

Output Format : NGC

Target Device : xc6slx4-3-tqg144

-- -- Source Options

Top Module Name : cla_add_n_bit

Automatic FSM Extraction : YES

FSM Encoding Algorithm : Auto

Safe Implementation : No

FSM Style : LUT

RAM Extraction : Yes

RAM Style : Auto

ROM Extraction : Yes

Shift Register Extraction : YES

ROM Style : Auto

Resource Sharing : YES

Asynchronous To Synchronous : NO

Shift Register Minimum Size : 2

Use DSP Block : Auto

Automatic Register Balancing : No

-- -- Target Options

LUT Combining : Auto

Reduce Control Sets : Auto

Add IO Buffers : YES

Global Maximum Fanout : 100000

Add Generic Clock Buffer(BUFG) : 16

Register Duplication : YES

Optimize Instantiated Primitives : NO

Use Clock Enable : Auto

Use Synchronous Set : Auto

Use Synchronous Reset : Auto

Pack IO Registers into IOBs : Auto

Equivalent register Removal : YES

-- -- General Options

Optimization Goal : Speed

Optimization Effort : 1

Power Reduction : NO

Keep Hierarchy : No

Netlist Hierarchy : As_Optimized

RTL Output : Yes

Global Optimization : AllClockNets

Read Cores : YES

Write Timing Constraints : NO

Cross Clock Analysis : NO

Hierarchy Separator : /

Bus Delimiter : <>

Case Specifier : Maintain

Slice Utilization Ratio : 100

BRAM Utilization Ratio : 100

DSP48 Utilization Ratio : 100

Auto BRAM Packing : NO

Slice Utilization Ratio Delta : 5

=====

```

=====
* HDL Parsing *
=====
Parsing VHDL file "64210382\cla_gp.vhd" into library work
Parsing entity <cla_gp>.
Parsing architecture <ideal> of entity <cla_gp>.
Parsing VHDL file "64210382\cla_add_n_bit.vhd" into library work
Parsing entity <cla_add_n_bit>.
Parsing architecture <arch> of entity <cla_add_n_bit>.

=====
* HDL Elaboration *
=====

Elaborating entity <cla_add_n_bit> ( architecture <arch> ) with generics from
library <work>.

=====
* HDL Synthesis *
=====

Synthesizing Unit <cla_add_n_bit>.
Related source file is "64210382\cla_add_n_bit.vhd".
  n = 8
  Summary:
Unit <cla_add_n_bit> synthesized.

=====
HDL Synthesis Report

Macro Statistics
# Xors : 16
  1-bit xor2 : 16

=====

=====
* Advanced HDL Synthesis *
=====

=====
Advanced HDL Synthesis Report

Macro Statistics
# Xors : 16
  1-bit xor2 : 16

=====

=====
* Low Level Synthesis *
=====

Optimizing unit <cla_add_n_bit> ...

Mapping all equations...
Building and optimizing final netlist ...

```

Found area constraint ratio of 100 (+ 5) on block cla_add_n_bit, actual ratio is 1.

Final Macro Processing ...

=====
Final Register Report

Found no macro

=====
* Partition Report *
=====

Partition Implementation Status

-- -- -- -- -- -- -- -- -- -- -- -- -- --
-- -- -

No Partitions were found in this design.

-- -- -- -- -- -- -- -- -- -- -- -- -- --
-- -- -

=====
* Design Summary *
=====

Top Level Output File Name : cla_add_n_bit.ngc

Primitive and Black Box Usage:

-- -- -- -- -- -- -- -- -- -- -- -- -- --
-- --

BELS : 24
LUT2 : 6
LUT3 : 3
LUT5 : 6
LUT6 : 9
IO Buffers : 28
IBUF : 17
OBUF : 11

Device utilization summary:

-- -- -- -- -- -- -- -- -- -- -- -- -- --
-

Selected Device : 6slx4tqg144-3

Slice Logic Utilization:

Number of Slice LUTs: 24 out of 2400 1%
Number used as Logic: 24 out of 2400 1%

Slice Logic Distribution:

Number of LUT Flip Flop pairs used: 24
Number with an unused Flip Flop: 24 out of 24 100%
Number with an unused LUT: 0 out of 24 0%
Number of fully used LUT-FF pairs: 0 out of 24 0%
Number of unique control sets: 0

IO Utilization:

Number of IOs: 28

Number of bonded IOBs: 28 out of 102 27%

Specific Feature Utilization:

```
-- -- -- -- -- -- -- -- -- -- -- -- -- --  
-
```

Partition Resource Summary:

```
-- -- -- -- -- -- -- -- -- -- -- -- -- --  
-
```

No Partitions were found in this design.

```
-- -- -- -- -- -- -- -- -- -- -- -- -- --  
-
```

=====
Timing Report

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.

FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT
GENERATED AFTER PLACE-and-ROUTE.

Clock Information:

```
-- -- -- -- -- -- -- -- -- -- -- -- -- --  
No clock signals found in this design
```

Asynchronous Control Signals Information:

```
-- -- -- -- -- -- -- -- -- -- -- -- -- --  
-- -- -- -- -- -- -- -- -- -- -- -- -- --
```

No asynchronous control signals found in this design

Timing Summary:

```
-- -- -- -- -- -- -- -- -- -- -- -- -- --
```

Speed Grade: -3

Minimum period: No path found

Minimum input arrival time before clock: No path found

Maximum output required time after clock: No path found

Maximum combinational path delay: 9.101ns

Timing Details:

```
-- -- -- -- -- -- -- -- -- -- -- -- -- --
```

All values displayed in nanoseconds (ns)

=====
Timing constraint: Default path analysis

Total number of paths / destination ports: 131 / 11

```
-- -- -- -- -- -- -- -- -- -- -- -- -- --  
-- -- -- -- -- -- -- -- -- -- -- -- -- --  
-- -- -- -- -- -- -- -- -- -- -- -- -- --
```

Delay: 9.101ns (Levels of Logic = 7)

Source: Y<0> (PAD)

Destination: S<7> (PAD)

Data Path: Y<0> to S<7>

Gate Net

Cell:in->out fanout Delay Delay Logical Name (Net Name)

```

--      --      --      --      --      --      --      --      --      --      --
--      --      --      --      --      --      --      --      --      --      --
--      --
IBUF:I->0 6 1.222 0.973 Y_0_IBUF ( Y_0_IBUF )
LUT3:I0->0 2 0.205 0.617 C<3>_SW0 ( N2 )
LUT5:I4->0 3 0.205 0.651 C<3> ( C<3> )
LUT3:I2->0 2 0.205 0.617 C<6>_SW0 ( N4 )
LUT5:I4->0 2 0.205 0.845 C<6> ( C<6> )
LUT5:I2->0 1 0.205 0.579 Mxor_S_sig<7>_xo<0>1 ( S_7_OBUF )
OBUF:I->0 2.571 S_7_OBUF ( S<7> )
--      --      --      --      --      --      --      --      --      --      --
--      --      --      --      --      --      --      --      --      --      --
Total 9.101ns ( 4.818ns logic, 4.283ns route )
( 52.9% logic, 47.1% route )

```

Cross Clock Domains Report:

```

Total REAL time to Xst completion: 10.00 secs
Total CPU time to Xst completion: 9.22 secs

```

```
-- >
```

Total memory usage is 4487500 kilobytes

Number of errors : 0 (0 filtered)

Number of warnings : 0 (0 filtered)

Number of infos : 0 (0 filtered)

```

64210382>fuse -incremental -o cla_add_n_bit_tb_isim_beh.exe -prj
cla_add_n_bit_tb.prj -top cla_add_n_bit_tb
Running: \unwrapped\fuse.exe -incremental -o cla_add_n_bit_tb_isim_beh.exe -prj
cla_add_n_bit_tb.prj -top cla_add_n_bit_tb
ISim P.20131013 ( signature 0x7708f090 )
Number of CPUs detected in this system: 8
Turning on mult-threading, number of parallel sub-compilation jobs: 16
Determining compilation order of HDL files
Parsing VHDL file "cla_gp.vhd" into library work
Parsing VHDL file "cla_add_n_bit.vhd" into library work
Parsing VHDL file "cla_add_n_bit_tb_IDEAL.vhd" into library work
Starting static elaboration
Completed static elaboration
Compiling package standard
Compiling package std_logic_1164
Compiling package textio
Compiling package std_logic_textio
Compiling package numeric_std
Compiling package attributes
Compiling package std_logic_misc
Compiling architecture arch of entity cla_add_n_bit [ \cla_add_n_bit( 8 ) \ ]
Compiling architecture testbench_arch of entity cla_add_n_bit_tb
Time Resolution for simulation is 1ps.
Waiting for 1 sub-compilation( s ) to finish...
Compiled 10 VHDL Units
Built simulation executable cla_add_n_bit_tb_isim_beh.exe

```

Fuse Memory Usage: 37528 KB
Fuse CPU Usage: 936 ms

```
64210382>cla_add_n_bit_tb_isim_beh.exe -tclbatch isim.tcl -wdb
cla_add_n_bit_tb_isim_beh.wdb
ISim P.20131013 ( signature 0x7708f090 )
WARNING: A WEBPACK license was found.
WARNING: Please use Xilinx License Configuration Manager to check out a full ISim
license.
WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for
more information on the differences between the Lite and the Full version.
This is a Lite version of ISim.
Time resolution is 1 ps
Simulator is doing circuit initialization process.
Finished circuit initialization process.
```

```
64210382>rem ***** test cla flags
```

```
64210382>xst -ifn cla_add_n_bit_flags.xst
Release 14.7 - xst P.20131013 ( nt64 )
Copyright ( c ) 1995-2013 Xilinx, Inc. All rights reserved.
-- > Parameter TMPDIR set to xst/projnav.tmp
```

Total REAL time to Xst completion: 1.00 secs
Total CPU time to Xst completion: 0.27 secs

```
-- > Parameter xsthdpdir set to xst
```

Total REAL time to Xst completion: 1.00 secs
Total CPU time to Xst completion: 0.27 secs

```
-- > ERROR:Xst:438 - Can not open file : cla_add_n_bit_flags.prj
```

Total REAL time to Xst completion: 1.00 secs
Total CPU time to Xst completion: 0.31 secs

```
-- >
```

Total memory usage is 4422880 kilobytes

Number of errors : 1 (0 filtered)
Number of warnings : 0 (0 filtered)
Number of infos : 0 (0 filtered)

```
64210382>fuse -incremental -o cla_add_n_bit_tb_flags_isim_beh.exe -prj
cla_add_n_bit_flags_tb.prj -top cla_add_n_bit_flags_tb_IDEAL
Running: \unwrapped\fuse.exe -incremental -o cla_add_n_bit_tb_flags_isim_beh.exe -
prj cla_add_n_bit_flags_tb.prj -top cla_add_n_bit_flags_tb_IDEAL
ISim P.20131013 ( signature 0x7708f090 )
Number of CPUs detected in this system: 8
Turning on mult-threading, number of parallel sub-compilation jobs: 16
Determining compilation order of HDL files
Parsing VHDL file "cla_gp.vhd" into library work
Parsing VHDL file "cla_add_n_bit.vhd" into library work
Parsing VHDL file "cla_add_n_bit_flags_tb_IDEAL.vhd" into library work
Starting static elaboration
Completed static elaboration
Compiling package standard
Compiling package std_logic_1164
```

```

Compiling package textio
Compiling package std_logic_textio
Compiling package numeric_std
Compiling package attributes
Compiling package std_logic_misc
Compiling architecture arch of entity cla_add_n_bit [\cla_add_n_bit( 8 )\]
Compiling architecture a1 of entity cla_add_n_bit_flags_tb_ideal
Time Resolution for simulation is 1ps.
Compiled 10 VHDL Units
Built simulation executable cla_add_n_bit_tb_flags_isim_beh.exe
Fuse Memory Usage: 37460 KB
Fuse CPU Usage: 999 ms

64210382>cla_add_n_bit_tb_flags_isim_beh.exe -tclbatch isim.tcl -wdb
cla_add_n_bit_flags_tb.wdb
ISim P.20131013 ( signature 0x7708f090 )
WARNING: A WEBPACK license was found.
WARNING: Please use Xilinx License Configuration Manager to check out a full ISim
license.
WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for
more information on the differences between the Lite and the Full version.
This is a Lite version of ISim.
Time resolution is 1 ps
Simulator is doing circuit initialization process.
Finished circuit initialization process.

64210382>rem ***** test alu operations

64210382>xst -ifn alu_cla.xst
Release 14.7 - xst P.20131013 ( nt64 )
Copyright ( c ) 1995-2013 Xilinx, Inc. All rights reserved.
-- > Parameter TMPDIR set to xst/projnav.tmp

Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.25 secs

-- > Parameter xsthdpdir set to xst

Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.25 secs

-- >
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```

- 8.4.3) Timing Summary
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- 8.4.5) Cross Clock Domains [Report](#)

```
=====
* Synthesis Options Summary *
=====
--      -- Source Parameters
Input File Name : "alu_cla.prj"
Ignore Synthesis Constraint File : NO

--      -- Target Parameters
Output File Name : "alu_cla"
Output Format : NGC
Target Device : xc6slx4-3-tqg144

--      -- Source Options
Top Module Name : alu_cla
Automatic FSM Extraction : YES
FSM Encoding Algorithm : Auto
Safe Implementation : No
FSM Style : LUT
RAM Extraction : Yes
RAM Style : Auto
ROM Extraction : Yes
Shift Register Extraction : YES
ROM Style : Auto
Resource Sharing : YES
Asynchronous To Synchronous : NO
Shift Register Minimum Size : 2
Use DSP Block : Auto
Automatic Register Balancing : No

--      -- Target Options
LUT Combining : Auto
Reduce Control Sets : Auto
Add IO Buffers : YES
Global Maximum Fanout : 100000
Add Generic Clock Buffer( BUFG ) : 16
Register Duplication : YES
Optimize Instantiated Primitives : NO
Use Clock Enable : Auto
Use Synchronous Set : Auto
Use Synchronous Reset : Auto
Pack IO Registers into IOBs : Auto
Equivalent register Removal : YES

--      -- General Options
Optimization Goal : Speed
Optimization Effort : 1
Power Reduction : NO
Keep Hierarchy : No
Netlist Hierarchy : As_Optimized
RTL Output : Yes
Global Optimization : AllClockNets
Read Cores : YES
Write Timing Constraints : NO
Cross Clock Analysis : NO
Hierarchy Separator : /
```


Bus Delimiter : <>
Case Specifier : Maintain
Slice Utilization Ratio : 100
BRAM Utilization Ratio : 100
DSP48 Utilization Ratio : 100
Auto BRAM Packing : NO
Slice Utilization Ratio Delta : 5

=====

=====

* HDL Parsing *

=====

Parsing VHDL file "64210382\cla_gp.vhd" into library work
Parsing entity <cla_gp>.
Parsing architecture <ideal> of entity <cla_gp>.
Parsing VHDL file "64210382\cla_add_n_bit.vhd" into library work
Parsing entity <cla_add_n_bit>.
Parsing architecture <arch> of entity <cla_add_n_bit>.
Parsing VHDL file "64210382\alu_cla.vhd" into library work
Parsing entity <alu_cla>.
Parsing architecture <NDV> of entity <alu_cla>.

=====

* HDL Elaboration *

=====

Elaborating entity <alu_cla> (architecture <NDV>) with generics from library <work>.

Elaborating entity <cla_add_n_bit> (architecture <arch>) with generics from library <work>.

=====

* HDL Synthesis *

=====

Synthesizing Unit <alu_cla>.
Related source file is "64210382\alu_cla.vhd".
n = 8
Found 8-bit 12-to-1 multiplexer for signal <S> created at line 55.
Summary:
inferred 19 Multiplexer(s).
Unit <alu_cla> synthesized.

Synthesizing Unit <cla_add_n_bit>.
Related source file is "64210382\cla_add_n_bit.vhd".
n = 8
Summary:
Unit <cla_add_n_bit> synthesized.

=====

HDL Synthesis Report

Macro Statistics

Multiplexers : 19
1-bit 2-to-1 multiplexer : 12
8-bit 12-to-1 multiplexer : 1
8-bit 2-to-1 multiplexer : 6

```
# Xors : 17
 1-bit xor2 : 16
 8-bit xor2 : 1
```

=====

=====

```
* Advanced HDL Synthesis *
```

=====

=====

Advanced HDL Synthesis Report

Macro Statistics

```
# Multiplexers : 19
 1-bit 2-to-1 multiplexer : 12
 8-bit 12-to-1 multiplexer : 1
 8-bit 2-to-1 multiplexer : 6
# Xors : 17
 1-bit xor2 : 16
 8-bit xor2 : 1
```

=====

=====

```
* Low Level Synthesis *
```

=====

Optimizing unit <alu_cla> ...

Optimizing unit <cla_add_n_bit> ...

Mapping all equations...

Building and optimizing final netlist ...

Found area constraint ratio of 100 (+ 5) on block alu_cla, actual ratio is 3.

Final Macro Processing ...

=====

Final Register Report

Found no macro

=====

=====

```
* Partition Report *
```

=====

Partition Implementation Status

```
--      --      --      --      --      --      --      --      --      --      --      --
--      --      --      --      --      --      --      --      --      --      --      --
```

No Partitions were found in this design.

```
--      --      --      --      --      --      --      --      --      --      --      --
--      --      --      --      --      --      --      --      --      --      --      --
```

=====

```
* Design Summary *
```

=====

Top Level Output File Name : alu_cla.ngc

Primitive and Black Box Usage:

```
--      --      --      --      --      --      --      --      --      --      --      --
--      --      --
# BELS : 60
# LUT3 : 4
# LUT5 : 14
# LUT6 : 41
# MUXF7 : 1
# IO Buffers : 34
# IBUF : 20
# OBUF : 14
```

Device utilization summary:

```
--      --      --      --      --      --      --      --      --      --      --      --
-
```

Selected Device : 6slx4tqg144-3

Slice Logic Utilization:

Number of Slice LUTs: 59 out of 2400 2%
Number used as Logic: 59 out of 2400 2%

Slice Logic Distribution:

Number of LUT Flip Flop pairs used: 59
Number with an unused Flip Flop: 59 out of 59 100%
Number with an unused LUT: 0 out of 59 0%
Number of fully used LUT-FF pairs: 0 out of 59 0%
Number of unique control sets: 0

IO Utilization:

Number of IOs: 34
Number of bonded IOBs: 34 out of 102 33%

Specific Feature Utilization:

```
--      --      --      --      --      --      --      --      --      --      --      --
-
```

Partition Resource Summary:

```
--      --      --      --      --      --      --      --      --      --      --      --
-
```

No Partitions were found in this design.

```
--      --      --      --      --      --      --      --      --      --      --      --
-
```

=====

Timing Report

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.

FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT
GENERATED AFTER PLACE-and-ROUTE.

Clock Information:

```
--      --      --      --      --      --      --      --
```

No clock signals found in this design

Asynchronous Control Signals Information:

```
-- -- -- -- -- -- -- -- -- -- -- -- -- --
-- -- -- -- -- -- -- -- -- -- -- -- -- --
```

No asynchronous control signals found in this design

Timing Summary:

```
-- -- -- -- -- -- -- -- -- -- -- -- -- --
Speed Grade: -3
```

Minimum period: No path found

Minimum input arrival time before clock: No path found

Maximum output required time after clock: No path found

Maximum combinational path delay: 11.168ns

Timing Details:

```
-- -- -- -- -- -- -- -- -- -- -- -- -- --
All values displayed in nanoseconds ( ns )
```

Timing constraint: Default path analysis

Total number of paths / destination ports: 1146 / 14

```
-- -- -- -- -- -- -- -- -- -- -- -- -- --
-- -- -- -- -- -- -- -- -- -- -- -- -- --
-- -- -- -- -- -- -- -- -- -- -- -- -- --
```

Delay: 11.168ns (Levels of Logic = 8)

Source: F<2> (PAD)

Destination: Negative (PAD)

Data Path: F<2> to Negative

Gate Net

Cell: in->out fanout Delay Delay Logical Name (Net Name)

```
-- -- -- -- -- -- -- -- -- -- -- -- -- --
-- -- -- -- -- -- -- -- -- -- -- -- -- --
-- -- -- -- -- -- -- -- -- -- -- -- -- --
```

IBUF:I->0 35 1.222 1.679 F_2_IBUF (F_2_IBUF)

LUT6:I1->0 6 0.203 0.973 Mmux_Y_sig31 (Y_sig<1>)

LUT5:I2->0 4 0.205 1.028 U1/C<3>2 (U1/C<3>)

LUT6:I1->0 1 0.203 0.000 U1/C<6>_G (N16)

MUXF7:I1->0 5 0.140 0.943 U1/C<6> (U1/C<6>)

LUT5:I2->0 3 0.205 1.015 U1/Mxor_S_sig<7>_xo<0>1 (S_sig<7>)

LUT6:I0->0 1 0.203 0.579 Mmux_Negative1 (Negative_OBUF)

OBUF:I->0 2.571 Negative_OBUF (Negative)

```
-- -- -- -- -- -- -- -- -- -- -- -- -- --
-- -- -- -- -- -- -- -- -- -- -- -- -- --
```

Total 11.168ns (4.952ns logic, 6.216ns route)

(44.3% logic, 55.7% route)

Cross Clock Domains Report:

```
-- -- -- -- -- -- -- -- -- -- -- -- -- --
```

Total REAL time to Xst completion: 10.00 secs

Total CPU time to Xst completion: 10.17 secs

-- >

Total memory usage is 4487500 kilobytes

Number of errors : 0 (0 filtered)

Number of warnings : 0 (0 filtered)

Number of infos : 0 (0 filtered)

64210382>fuse -incremental -o alu_cla_tb_isim_beh.exe -prj alu_cla_tb.prj -top alu_cla_tb

Running: \unwrapped\fuse.exe -incremental -o alu_cla_tb_isim_beh.exe -prj alu_cla_tb.prj -top alu_cla_tb

ISim P.20131013 (signature 0x7708f090)

Number of CPUs detected in this system: 8

Turning on mult-threading, number of parallel sub-compilation jobs: 16

Determining compilation order of HDL files

Parsing VHDL file "cla_gp.vhd" into library work

Parsing VHDL file "cla_add_n_bit.vhd" into library work

Parsing VHDL file "alu_cla.vhd" into library work

Parsing VHDL file "alu_cla_tb_IDEAL.vhd" into library work

Starting static elaboration

Completed static elaboration

Compiling package standard

Compiling package std_logic_1164

Compiling package textio

Compiling package std_logic_textio

Compiling package numeric_std

Compiling package attributes

Compiling package std_logic_misc

Compiling architecture arch of entity cla_add_n_bit [\cla_add_n_bit(8)\]

Compiling architecture ndv of entity alu_cla [\alu_cla(8)\]

Compiling architecture testbench_arch of entity alu_cla_tb

Time Resolution for simulation is 1ps.

Waiting for 1 sub-compilation(s) to finish...

Compiled 12 VHDL Units

Built simulation executable alu_cla_tb_isim_beh.exe

Fuse Memory Usage: 37764 KB

Fuse CPU Usage: 921 ms

64210382>alu_cla_tb_isim_beh.exe -tclbatch isim.tcl -wdb alu_cla_tb_isim_beh.wdb

ISim P.20131013 (signature 0x7708f090)

WARNING: A WEBPACK license was found.

WARNING: Please use Xilinx License Configuration Manager to check out a full ISim license.

WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for more information on the differences between the Lite and the Full version.

This is a Lite version of ISim.

Time resolution is 1 ps

Simulator is doing circuit initialization process.

Finished circuit initialization process.

at 7864320 ns, Instance /alu_cla_tb/ : Warning: NUMERIC_STD.TO_UNSIGNED: vector truncated

at 8847360 ns, Instance /alu_cla_tb/ : Warning: NUMERIC_STD.TO_UNSIGNED: vector truncated

at 9830400 ns, Instance /alu_cla_tb/ : Warning: NUMERIC_STD.TO_UNSIGNED: vector truncated

at 10813440 ns, Instance /alu_cla_tb/ : Warning: NUMERIC_STD.TO_UNSIGNED: vector truncated

at 11796480 ns, Instance /alu_cla_tb/ : Warning: NUMERIC_STD.TO_UNSIGNED: vector truncated
at 12779520 ns, Instance /alu_cla_tb/ : Warning: NUMERIC_STD.TO_UNSIGNED: vector truncated
at 13762560 ns, Instance /alu_cla_tb/ : Warning: NUMERIC_STD.TO_UNSIGNED: vector truncated
at 14745600 ns, Instance /alu_cla_tb/ : Warning: NUMERIC_STD.TO_UNSIGNED: vector truncated

64210382>rem ***** test alu flags

64210382>xst -ifn alu_cla_flags.xst
Release 14.7 - xst P.20131013 (nt64)
Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.
-- > Parameter TMPDIR set to xst/projnav.tmp

Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.24 secs

-- > Parameter xsthdmdir set to xst

Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.25 secs

-- >

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 - 8.4.5) Cross Clock Domains Report

=====
* Synthesis Options Summary *

=====

-- -- Source Parameters

Input File Name : "alu_cla_flags_tb.prj"
Ignore Synthesis Constraint File : NO

-- -- Target Parameters

Output File Name : "alu_cla_flags_tb"
Output Format : NGC
Target Device : xc6slx4-3-tqg144

-- -- Source Options

Top Module Name : alu_cla_flags_tb
Automatic FSM Extraction : YES
FSM Encoding Algorithm : Auto
Safe Implementation : No
FSM Style : LUT
RAM Extraction : Yes
RAM Style : Auto
ROM Extraction : Yes
Shift Register Extraction : YES
ROM Style : Auto
Resource Sharing : YES
Asynchronous To Synchronous : NO
Shift Register Minimum Size : 2
Use DSP Block : Auto
Automatic Register Balancing : No

-- -- Target Options

LUT Combining : Auto
Reduce Control Sets : Auto
Add IO Buffers : YES
Global Maximum Fanout : 100000
Add Generic Clock Buffer(BUFG) : 16
Register Duplication : YES
Optimize Instantiated Primitives : NO
Use Clock Enable : Auto
Use Synchronous Set : Auto
Use Synchronous Reset : Auto
Pack IO Registers into IOBs : Auto
Equivalent register Removal : YES

-- -- General Options

Optimization Goal : Speed
Optimization Effort : 1
Power Reduction : NO
Keep Hierarchy : No
Netlist Hierarchy : As_Optimized
RTL Output : Yes
Global Optimization : AllClockNets
Read Cores : YES
Write Timing Constraints : NO
Cross Clock Analysis : NO
Hierarchy Separator : /
Bus Delimiter : <>
Case Specifier : Maintain
Slice Utilization Ratio : 100
BRAM Utilization Ratio : 100
DSP48 Utilization Ratio : 100
Auto BRAM Packing : NO
Slice Utilization Ratio Delta : 5

=====

=====

* HDL Parsing *

=====

Parsing VHDL file "64210382\cla_gp.vhd" into library work
Parsing entity <cla_gp>.
Parsing architecture <ideal> of entity <cla_gp>.
Parsing VHDL file "64210382\cla_add_n_bit.vhd" into library work

```

Parsing entity <cla_add_n_bit>.
Parsing architecture <arch> of entity <cla_add_n_bit>.
Parsing VHDL file "64210382\alu_cla.vhd" into library work
Parsing entity <alu_cla>.
Parsing architecture <NDV> of entity <alu_cla>.
Parsing VHDL file "64210382\alu_cla_tb_FLAGS_IDEAL.vhd" into library work
Parsing entity <alu_cla_flags_tb>.
Parsing architecture <test_alu_flags> of entity <alu_cla_flags_tb>.

=====
* HDL Elaboration *
=====

Elaborating entity <alu_cla_flags_tb> ( architecture <test_alu_flags> ) with
generics from library <work>.

Elaborating entity <alu_cla> ( architecture <NDV> ) with generics from library
<work>.

Elaborating entity <cla_add_n_bit> ( architecture <arch> ) with generics from
library <work>.
ERROR:HDLCompiler:890 - "64210382\alu_cla_tb_FLAGS_IDEAL.vhd" Line 144: wait
statement without UNTIL clause not supported for synthesis
Netlist alu_cla_flags_tb( 8 )( test_alu_flags ) remains a blackbox, due to errors
in its contents
-- >

```

Total memory usage is 4466680 kilobytes

Number of errors : 1 (0 filtered)

Number of warnings : 0 (0 filtered)

Number of infos : 0 (0 filtered)

```

64210382>fuse -incremental -o alu_cla_flags_tb_isim_beh.exe -prj
alu_cla_flags_tb.prj -top alu_cla_flags_tb
Running: \unwrapped\fuse.exe -incremental -o alu_cla_flags_tb_isim_beh.exe -prj
alu_cla_flags_tb.prj -top alu_cla_flags_tb
ISim P.20131013 ( signature 0x7708f090 )
Number of CPUs detected in this system: 8
Turning on mult-threading, number of parallel sub-compilation jobs: 16
Determining compilation order of HDL files
Parsing VHDL file "cla_gp.vhd" into library work
Parsing VHDL file "cla_add_n_bit.vhd" into library work
Parsing VHDL file "alu_cla.vhd" into library work
Parsing VHDL file "alu_cla_tb_FLAGS_IDEAL.vhd" into library work
Starting static elaboration
Completed static elaboration
Compiling package standard
Compiling package std_logic_1164
Compiling package textio
Compiling package std_logic_textio
Compiling package numeric_std
Compiling package attributes
Compiling package std_logic_misc
Compiling architecture arch of entity cla_add_n_bit [\cla_add_n_bit( 8 )\]
Compiling architecture ndv of entity alu_cla [\alu_cla( 8 )\]
Compiling architecture test_alu_flags of entity alu_cla_flags_tb
Time Resolution for simulation is 1ps.
Waiting for 1 sub-compilation( s ) to finish...

```


Compiled 12 VHDL Units
Built simulation executable alu_cla_flags_tb_isim_beh.exe
Fuse Memory Usage: 37604 KB
Fuse CPU Usage: 937 ms

```
64210382>alu_cla_flags_tb_isim_beh.exe -tclbatch isim.tcl -wdb
alu_cla_flags_tb_isim_beh.wdb
ISim P.20131013 ( signature 0x7708f090 )
WARNING: A WEBPACK license was found.
WARNING: Please use Xilinx License Configuration Manager to check out a full ISim
license.
WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for
more information on the differences between the Lite and the Full version.
This is a Lite version of ISim.
Time resolution is 1 ps
Simulator is doing circuit initialization process.
Finished circuit initialization process.
```

```
-- *****
-- **** STUDENT: 64210384
-- *****
-- KOMENTARJI K OCENI NALOGE
-- Matej Možek: Ni pripomb
-- *****
```

```
64210384>rem ***** test cla adder
```

```
64210384>if not exist "xst" mkdir xst
```

```
64210384>cd XST
```

```
64210384\xst>if not exist "projnav.tmp" mkdir "projnav.tmp"
```

```
64210384\xst>cd ..
```

```
64210384>rem ***** test cla operations
```

```
64210384>xst -ifn cla_add_n_bit.xst
Release 14.7 - xst P.20131013 ( nt64 )
Copyright ( c ) 1995-2013 Xilinx, Inc. All rights reserved.
-- > Parameter TMPDIR set to xst/projnav.tmp
```

```
Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.28 secs
```

```
-- > Parameter xsthdpdir set to xst
```

```
Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.29 secs
```

```
-- >
```

```
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```
=====
* Synthesis Options Summary *
=====
```

```
-- -- Source Parameters
```

```
Input File Name : "cla_add_n_bit.prj"
```

Ignore Synthesis Constraint File : NO

-- -- Target Parameters

Output File Name : "cla_add_n_bit"

Output Format : NGC

Target Device : xc6slx4-3-tqg144

-- -- Source Options

Top Module Name : cla_add_n_bit

Automatic FSM Extraction : YES

FSM Encoding Algorithm : Auto

Safe Implementation : No

FSM Style : LUT

RAM Extraction : Yes

RAM Style : Auto

ROM Extraction : Yes

Shift Register Extraction : YES

ROM Style : Auto

Resource Sharing : YES

Asynchronous To Synchronous : NO

Shift Register Minimum Size : 2

Use DSP Block : Auto

Automatic Register Balancing : No

-- -- Target Options

LUT Combining : Auto

Reduce Control Sets : Auto

Add IO Buffers : YES

Global Maximum Fanout : 100000

Add Generic Clock Buffer(BUFG) : 16

Register Duplication : YES

Optimize Instantiated Primitives : NO

Use Clock Enable : Auto

Use Synchronous Set : Auto

Use Synchronous Reset : Auto

Pack IO Registers into IOBs : Auto

Equivalent register Removal : YES

-- -- General Options

Optimization Goal : Speed

Optimization Effort : 1

Power Reduction : NO

Keep Hierarchy : No

Netlist Hierarchy : As_Optimized

RTL Output : Yes

Global Optimization : AllClockNets

Read Cores : YES

Write Timing Constraints : NO

Cross Clock Analysis : NO

Hierarchy Separator : /

Bus Delimiter : <>

Case Specifier : Maintain

Slice Utilization Ratio : 100

BRAM Utilization Ratio : 100

DSP48 Utilization Ratio : 100

Auto BRAM Packing : NO

Slice Utilization Ratio Delta : 5

=====

```

=====
* HDL Parsing *
=====
Parsing VHDL file "64210384\cla_gp.vhd" into library work
Parsing entity <cla_gp>.
Parsing architecture <ideal> of entity <cla_gp>.
Parsing VHDL file "64210384\cla_add_n_bit.vhd" into library work
Parsing entity <cla_add_n_bit>.
Parsing architecture <NDV> of entity <cla_add_n_bit>.

=====
* HDL Elaboration *
=====

Elaborating entity <cla_add_n_bit> ( architecture <NDV> ) with generics from
library <work>.

=====
* HDL Synthesis *
=====

Synthesizing Unit <cla_add_n_bit>.
Related source file is "64210384\cla_add_n_bit.vhd".
n = 8
Summary:
Unit <cla_add_n_bit> synthesized.

=====
HDL Synthesis Report

Macro Statistics
# Xors : 16
1-bit xor2 : 16

=====

=====
* Advanced HDL Synthesis *
=====

=====
Advanced HDL Synthesis Report

Macro Statistics
# Xors : 16
1-bit xor2 : 16

=====

=====
* Low Level Synthesis *
=====

Optimizing unit <cla_add_n_bit> ...

Mapping all equations...
Building and optimizing final netlist ...

```

Found area constraint ratio of 100 (+ 5) on block cla_add_n_bit, actual ratio is 1.

Final Macro Processing ...

=====
Final Register Report

Found no macro

=====
* Partition Report *
=====

Partition Implementation Status

-- -- -- -- -- -- -- -- -- -- -- -- -- --
-- -- -

No Partitions were found in this design.

-- -- -- -- -- -- -- -- -- -- -- -- -- --
-- -- -

=====
* Design Summary *
=====

Top Level Output File Name : cla_add_n_bit.ngc

Primitive and Black Box Usage:

-- -- -- -- -- -- -- -- -- -- -- -- -- --
-- --

BELS : 24
LUT2 : 6
LUT3 : 5
LUT5 : 6
LUT6 : 7
IO Buffers : 28
IBUF : 17
OBUF : 11

Device utilization summary:

-- -- -- -- -- -- -- -- -- -- -- -- -- --
-

Selected Device : 6slx4tqg144-3

Slice Logic Utilization:

Number of Slice LUTs: 24 out of 2400 1%
Number used as Logic: 24 out of 2400 1%

Slice Logic Distribution:

Number of LUT Flip Flop pairs used: 24
Number with an unused Flip Flop: 24 out of 24 100%
Number with an unused LUT: 0 out of 24 0%
Number of fully used LUT-FF pairs: 0 out of 24 0%
Number of unique control sets: 0

IO Utilization:

Number of IOs: 28

Number of bonded IOBs: 28 out of 102 27%

Specific Feature Utilization:

```
-- -- -- -- -- -- -- -- -- -- -- -- -- --
-
```

Partition Resource Summary:

```
-- -- -- -- -- -- -- -- -- -- -- -- -- --
-
```

No Partitions were found in this design.

```
-- -- -- -- -- -- -- -- -- -- -- -- -- --
-
```

=====
Timing Report

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.

FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT
GENERATED AFTER PLACE-and-ROUTE.

Clock Information:

```
-- -- -- -- -- -- -- -- -- -- -- -- -- --
```

No clock signals found in this design

Asynchronous Control Signals Information:

```
-- -- -- -- -- -- -- -- -- -- -- -- -- --
-- -- -- -- -- -- -- -- -- -- -- -- -- --
```

No asynchronous control signals found in this design

Timing Summary:

```
-- -- -- -- -- -- -- -- -- -- -- -- -- --
```

Speed Grade: -3

Minimum period: No path found

Minimum input arrival time before clock: No path found

Maximum output required time after clock: No path found

Maximum combinational path delay: 9.092ns

Timing Details:

```
-- -- -- -- -- -- -- -- -- -- -- -- -- --
```

All values displayed in nanoseconds (ns)

=====
Timing constraint: Default path analysis

Total number of paths / destination ports: 131 / 11

```
-- -- -- -- -- -- -- -- -- -- -- -- -- --
-- -- -- -- -- -- -- -- -- -- -- -- -- --
-- -- -- -- -- -- -- -- -- -- -- -- -- --
```

Delay: 9.092ns (Levels of Logic = 7)

Source: Y<0> (PAD)

Destination: S<7> (PAD)

Data Path: Y<0> to S<7>

Gate Net

Cell:in->out fanout Delay Delay Logical Name (Net Name)

```

--      --      --      --      --      --      --      --      --      --      --
--      --      --      --      --      --      --      --      --      --      --
--      --
IBUF:I->0 6 1.222 0.973 Y_0_IBUF ( Y_0_IBUF )
LUT3:I0->0 1 0.205 0.580 carry<3>_SW0 ( N2 )
LUT5:I4->0 4 0.205 0.684 carry<3> ( carry<3> )
LUT3:I2->0 1 0.205 0.580 carry<6>_SW0 ( N4 )
LUT5:I4->0 3 0.205 0.879 carry<6> ( carry<6> )
LUT5:I2->0 1 0.205 0.579 Mxor_vsota<7>_xo<0>1 ( S_7_OBUF )
OBUF:I->0 2.571 S_7_OBUF ( S<7> )
--      --      --      --      --      --      --      --      --      --      --
--      --      --      --      --      --      --      --      --      --      --
Total 9.092ns ( 4.818ns logic, 4.274ns route )
( 53.0% logic, 47.0% route )

```

Cross Clock Domains Report:

```

Total REAL time to Xst completion: 9.00 secs
Total CPU time to Xst completion: 9.15 secs

```

```
-- >
```

Total memory usage is 4487500 kilobytes

Number of errors : 0 (0 filtered)

Number of warnings : 0 (0 filtered)

Number of infos : 0 (0 filtered)

```

64210384>fuse -incremental -o cla_add_n_bit_tb_isim_beh.exe -prj
cla_add_n_bit_tb.prj -top cla_add_n_bit_tb
Running: \unwrapped\fuse.exe -incremental -o cla_add_n_bit_tb_isim_beh.exe -prj
cla_add_n_bit_tb.prj -top cla_add_n_bit_tb
ISim P.20131013 ( signature 0x7708f090 )
Number of CPUs detected in this system: 8
Turning on mult-threading, number of parallel sub-compilation jobs: 16
Determining compilation order of HDL files
Parsing VHDL file "cla_gp.vhd" into library work
Parsing VHDL file "cla_add_n_bit.vhd" into library work
Parsing VHDL file "cla_add_n_bit_tb_IDEAL.vhd" into library work
Starting static elaboration
Completed static elaboration
Compiling package standard
Compiling package std_logic_1164
Compiling package textio
Compiling package std_logic_textio
Compiling package numeric_std
Compiling package attributes
Compiling package std_logic_misc
Compiling architecture ndv of entity cla_add_n_bit [\cla_add_n_bit( 8 )\]
Compiling architecture testbench_arch of entity cla_add_n_bit_tb
Time Resolution for simulation is 1ps.
Waiting for 1 sub-compilation( s ) to finish...
Compiled 10 VHDL Units
Built simulation executable cla_add_n_bit_tb_isim_beh.exe

```

Fuse Memory Usage: 37344 KB
Fuse CPU Usage: 921 ms

```
64210384>cla_add_n_bit_tb_isim_beh.exe -tclbatch isim.tcl -wdb
cla_add_n_bit_tb_isim_beh.wdb
ISim P.20131013 ( signature 0x7708f090 )
WARNING: A WEBPACK license was found.
WARNING: Please use Xilinx License Configuration Manager to check out a full ISim
license.
WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for
more information on the differences between the Lite and the Full version.
This is a Lite version of ISim.
Time resolution is 1 ps
Simulator is doing circuit initialization process.
Finished circuit initialization process.
```

```
64210384>rem ***** test cla flags
```

```
64210384>xst -ifn cla_add_n_bit_flags.xst
Release 14.7 - xst P.20131013 ( nt64 )
Copyright ( c ) 1995-2013 Xilinx, Inc. All rights reserved.
-- > Parameter TMPDIR set to xst/projnav.tmp
```

Total REAL time to Xst completion: 1.00 secs
Total CPU time to Xst completion: 0.24 secs

```
-- > Parameter xsthdpdir set to xst
```

Total REAL time to Xst completion: 1.00 secs
Total CPU time to Xst completion: 0.24 secs

```
-- > ERROR:Xst:438 - Can not open file : cla_add_n_bit_flags.prj
```

Total REAL time to Xst completion: 1.00 secs
Total CPU time to Xst completion: 0.28 secs

```
-- >
```

Total memory usage is 4422880 kilobytes

Number of errors : 1 (0 filtered)
Number of warnings : 0 (0 filtered)
Number of infos : 0 (0 filtered)

```
64210384>fuse -incremental -o cla_add_n_bit_tb_flags_isim_beh.exe -prj
cla_add_n_bit_flags_tb.prj -top cla_add_n_bit_flags_tb_IDEAL
Running: \unwrapped\fuse.exe -incremental -o cla_add_n_bit_tb_flags_isim_beh.exe -
prj cla_add_n_bit_flags_tb.prj -top cla_add_n_bit_flags_tb_IDEAL
ISim P.20131013 ( signature 0x7708f090 )
Number of CPUs detected in this system: 8
Turning on mult-threading, number of parallel sub-compilation jobs: 16
Determining compilation order of HDL files
Parsing VHDL file "cla_gp.vhd" into library work
Parsing VHDL file "cla_add_n_bit.vhd" into library work
Parsing VHDL file "cla_add_n_bit_flags_tb_IDEAL.vhd" into library work
Starting static elaboration
Completed static elaboration
Compiling package standard
Compiling package std_logic_1164
```



```

Compiling package textio
Compiling package std_logic_textio
Compiling package numeric_std
Compiling package attributes
Compiling package std_logic_misc
Compiling architecture ndv of entity cla_add_n_bit [\cla_add_n_bit( 8 )\]
Compiling architecture a1 of entity cla_add_n_bit_flags_tb_ideal
Time Resolution for simulation is 1ps.
Waiting for 1 sub-compilation( s ) to finish...
Compiled 10 VHDL Units
Built simulation executable cla_add_n_bit_tb_flags_isim_beh.exe
Fuse Memory Usage: 37520 KB
Fuse CPU Usage: 953 ms

64210384>cla_add_n_bit_tb_flags_isim_beh.exe -tclbatch isim.tcl -wdb
cla_add_n_bit_flags_tb.wdb
ISim P.20131013 ( signature 0x7708f090 )
WARNING: A WEBPACK license was found.
WARNING: Please use Xilinx License Configuration Manager to check out a full ISim
license.
WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for
more information on the differences between the Lite and the Full version.
This is a Lite version of ISim.
Time resolution is 1 ps
Simulator is doing circuit initialization process.
Finished circuit initialization process.

64210384>rem ***** test alu operations

64210384>xst -ifn alu_cla.xst
Release 14.7 - xst P.20131013 ( nt64 )
Copyright ( c ) 1995-2013 Xilinx, Inc. All rights reserved.
-- > Parameter TMPDIR set to xst/projnav.tmp

Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.25 secs

-- > Parameter xsthdpdir set to xst

Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.25 secs

-- >
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```

- 8.4.2) Asynchronous Control Signals Information
- 8.4.3) Timing Summary
- 8.4.4) Timing Details
- 8.4.5) Cross Clock Domains [Report](#)

```
=====
* Synthesis Options Summary *
=====
--      -- Source Parameters
Input File Name : "alu_cla.prj"
Ignore Synthesis Constraint File : NO

--      -- Target Parameters
Output File Name : "alu_cla"
Output Format : NGC
Target Device : xc6slx4-3-tqg144

--      -- Source Options
Top Module Name : alu_cla
Automatic FSM Extraction : YES
FSM Encoding Algorithm : Auto
Safe Implementation : No
FSM Style : LUT
RAM Extraction : Yes
RAM Style : Auto
ROM Extraction : Yes
Shift Register Extraction : YES
ROM Style : Auto
Resource Sharing : YES
Asynchronous To Synchronous : NO
Shift Register Minimum Size : 2
Use DSP Block : Auto
Automatic Register Balancing : No

--      -- Target Options
LUT Combining : Auto
Reduce Control Sets : Auto
Add IO Buffers : YES
Global Maximum Fanout : 100000
Add Generic Clock Buffer( BUFG ) : 16
Register Duplication : YES
Optimize Instantiated Primitives : NO
Use Clock Enable : Auto
Use Synchronous Set : Auto
Use Synchronous Reset : Auto
Pack IO Registers into IOBs : Auto
Equivalent register Removal : YES

--      -- General Options
Optimization Goal : Speed
Optimization Effort : 1
Power Reduction : NO
Keep Hierarchy : No
Netlist Hierarchy : As_Optimized
RTL Output : Yes
Global Optimization : AllClockNets
Read Cores : YES
Write Timing Constraints : NO
Cross Clock Analysis : NO
```

Hierarchy Separator : /
Bus Delimiter : <>
Case Specifier : Maintain
Slice Utilization Ratio : 100
BRAM Utilization Ratio : 100
DSP48 Utilization Ratio : 100
Auto BRAM Packing : NO
Slice Utilization Ratio Delta : 5

=====

=====

* HDL Parsing *

=====

Parsing VHDL file "64210384\cla_gp.vhd" into library work
Parsing entity <cla_gp>.
Parsing architecture <ideal> of entity <cla_gp>.
Parsing VHDL file "64210384\cla_add_n_bit.vhd" into library work
Parsing entity <cla_add_n_bit>.
Parsing architecture <NDV> of entity <cla_add_n_bit>.
Parsing VHDL file "64210384\alu_cla.vhd" into library work
Parsing entity <alu_cla>.
Parsing architecture <NDV> of entity <alu_cla>.

=====

* HDL Elaboration *

=====

Elaborating entity <alu_cla> (architecture <NDV>) with generics from library <work>.

Elaborating entity <cla_add_n_bit> (architecture <NDV>) with generics from library <work>.

=====

* HDL Synthesis *

=====

Synthesizing Unit <alu_cla>.
Related source file is "64210384\alu_cla.vhd".
n = 8
Found 8-bit 12-to-1 multiplexer for signal <S> created at line 61.
Summary:
inferred 8 Multiplexer(s).
Unit <alu_cla> synthesized.

Synthesizing Unit <cla_add_n_bit>.
Related source file is "64210384\cla_add_n_bit.vhd".
n = 8
Summary:
Unit <cla_add_n_bit> synthesized.

=====

HDL Synthesis Report

Macro Statistics

Multiplexers : 8
1-bit 2-to-1 multiplexer : 1
8-bit 12-to-1 multiplexer : 1

```
8-bit 2-to-1 multiplexer : 6
# Xors : 17
1-bit xor2 : 16
8-bit xor2 : 1
```

=====

=====

* Advanced HDL Synthesis *

=====

=====

Advanced HDL Synthesis Report

Macro Statistics

```
# Multiplexers : 8
1-bit 2-to-1 multiplexer : 1
8-bit 12-to-1 multiplexer : 1
8-bit 2-to-1 multiplexer : 6
# Xors : 17
1-bit xor2 : 16
8-bit xor2 : 1
```

=====

=====

* Low Level Synthesis *

=====

Optimizing unit <alu_cla> ...

Optimizing unit <cla_add_n_bit> ...

Mapping all equations...

Building and optimizing final netlist ...

Found area constraint ratio of 100 (+ 5) on block alu_cla, actual ratio is 3.

Final Macro Processing ...

=====

Final Register Report

Found no macro

=====

=====

* Partition Report *

=====

Partition Implementation Status

```
--      --      --      --      --      --      --      --      --      --      --      --
--      --      --      --      --      --      --      --      --      --      --      --
```

No Partitions were found in this design.

```
--      --      --      --      --      --      --      --      --      --      --      --
--      --      --      --      --      --      --      --      --      --      --      --
```

=====

* Design Summary *

=====

Top Level Output File Name : alu_cla.ngc

Primitive and Black Box Usage:

```
--      --      --      --      --      --      --      --      --      --      --      --
--      --      --
# BELS : 52
# LUT3 : 1
# LUT5 : 13
# LUT6 : 34
# MUXF7 : 4
# IO Buffers : 34
# IBUF : 20
# OBUF : 14
```

Device utilization summary:

```
--      --      --      --      --      --      --      --      --      --      --      --
-
```

Selected Device : 6slx4tqg144-3

Slice Logic Utilization:

Number of Slice LUTs: 48 out of 2400 2%
Number used as Logic: 48 out of 2400 2%

Slice Logic Distribution:

Number of LUT Flip Flop pairs used: 48
Number with an unused Flip Flop: 48 out of 48 100%
Number with an unused LUT: 0 out of 48 0%
Number of fully used LUT-FF pairs: 0 out of 48 0%
Number of unique control sets: 0

IO Utilization:

Number of IOs: 34
Number of bonded IOBs: 34 out of 102 33%

Specific Feature Utilization:

```
--      --      --      --      --      --      --      --      --      --      --      --
-
```

Partition Resource Summary:

```
--      --      --      --      --      --      --      --      --      --      --      --
-
```

No Partitions were found in this design.

```
--      --      --      --      --      --      --      --      --      --      --      --
-
```

=====

Timing Report

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.
FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT
GENERATED AFTER PLACE-and-ROUTE.

Clock Information:

```

--      --      --      --      --      --      --      --      --
No clock signals found in this design

Asynchronous Control Signals Information:
--      --      --      --      --      --      --      --      --
--      --      --      --      --      --      --      --      --
No asynchronous control signals found in this design

Timing Summary:
--      --      --      --      --      --      --      --
Speed Grade: -3

Minimum period: No path found
Minimum input arrival time before clock: No path found
Maximum output required time after clock: No path found
Maximum combinational path delay: 12.374ns

Timing Details:
--      --      --      --      --      --      --      --
All values displayed in nanoseconds ( ns )

=====
Timing constraint: Default path analysis
Total number of paths / destination ports: 1306 / 14
--      --      --      --      --      --      --      --      --
--      --      --      --      --      --      --      --      --
--      --      --      --      --      --      --      --      --
Delay: 12.374ns ( Levels of Logic = 10 )
Source: F<2> ( PAD )
Destination: Overflow ( PAD )

Data Path: F<2> to Overflow
Gate Net
Cell:in->out fanout Delay Delay Logical Name ( Net Name )
--      --      --      --      --      --      --      --      --
--      --      --      --      --      --      --      --      --
--      --      --      --      --      --      --      --      --
IBUF:I->0 32 1.222 1.636 F_2_IBUF ( F_2_IBUF )
LUT6:I1->0 5 0.203 0.943 Mmux_y_temp31 ( y_temp<1> )
LUT5:I2->0 5 0.205 1.059 U1/carry<3>2 ( U1/carry<3> )
LUT6:I1->0 1 0.203 0.000 U1/carry<6>_G ( N21 )
MUXF7:I1->0 3 0.140 0.879 U1/carry<6> ( U1/carry<6> )
LUT5:I2->0 1 0.205 0.924 U1/Mxor_vsota<7>_xo<0>1 ( s_temp<7> )
LUT6:I1->0 5 0.203 1.059 Mmux_S22 ( Negative_OBUF )
LUT6:I1->0 1 0.203 0.000 Mmux_Overflow1_G ( N17 )
MUXF7:I1->0 1 0.140 0.579 Mmux_Overflow1 ( Overflow_OBUF )
OBUF:I->0 2.571 Overflow_OBUF ( Overflow )
--      --      --      --      --      --      --      --      --
--      --      --      --      --      --      --      --      --
Total 12.374ns ( 5.295ns logic, 7.079ns route )
( 42.8% logic, 57.2% route )

=====

Cross Clock Domains Report:
--      --      --      --      --      --      --      --      --
--      --      --      --      --      --      --      --      --
=====

```

Total REAL time to Xst completion: 10.00 secs
Total CPU time to Xst completion: 10.25 secs

-- >

Total memory usage is 4487500 kilobytes

Number of errors : 0 (0 filtered)

Number of warnings : 0 (0 filtered)

Number of infos : 0 (0 filtered)

64210384>fuse -incremental -o alu_cla_tb_isim_beh.exe -prj alu_cla_tb.prj -top alu_cla_tb

Running: \unwrapped\fuse.exe -incremental -o alu_cla_tb_isim_beh.exe -prj alu_cla_tb.prj -top alu_cla_tb

ISim P.20131013 (signature 0x7708f090)

Number of CPUs detected in this system: 8

Turning on mult-threading, number of parallel sub-compilation jobs: 16

Determining compilation order of HDL files

Parsing VHDL file "cla_gp.vhd" into library work

Parsing VHDL file "cla_add_n_bit.vhd" into library work

Parsing VHDL file "alu_cla.vhd" into library work

Parsing VHDL file "alu_cla_tb_IDEAL.vhd" into library work

Starting static elaboration

Completed static elaboration

Compiling package standard

Compiling package std_logic_1164

Compiling package textio

Compiling package std_logic_textio

Compiling package numeric_std

Compiling package attributes

Compiling package std_logic_misc

Compiling architecture ndv of entity cla_add_n_bit [\cla_add_n_bit(8)\]

Compiling architecture ndv of entity alu_cla [\alu_cla(8)\]

Compiling architecture testbench_arch of entity alu_cla_tb

Time Resolution for simulation is 1ps.

Waiting for 1 sub-compilation(s) to finish...

Compiled 12 VHDL Units

Built simulation executable alu_cla_tb_isim_beh.exe

Fuse Memory Usage: 37660 KB

Fuse CPU Usage: 984 ms

64210384>alu_cla_tb_isim_beh.exe -tclbatch isim.tcl -wdb alu_cla_tb_isim_beh.wdb

ISim P.20131013 (signature 0x7708f090)

WARNING: A WEBPACK license was found.

WARNING: Please use Xilinx License Configuration Manager to check out a full ISim license.

WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for more information on the differences between the Lite and the Full version.

This is a Lite version of ISim.

Time resolution is 1 ps

Simulator is doing circuit initialization process.

Finished circuit initialization process.

at 7864320 ns, Instance /alu_cla_tb/ : Warning: NUMERIC_STD.TO_UNSIGNED: vector truncated

at 8847360 ns, Instance /alu_cla_tb/ : Warning: NUMERIC_STD.TO_UNSIGNED: vector truncated

at 9830400 ns, Instance /alu_cla_tb/ : Warning: NUMERIC_STD.TO_UNSIGNED: vector truncated

at 10813440 ns, Instance /alu_cla_tb/ : Warning: NUMERIC_STD.TO_UNSIGNED: vector truncated
at 11796480 ns, Instance /alu_cla_tb/ : Warning: NUMERIC_STD.TO_UNSIGNED: vector truncated
at 12779520 ns, Instance /alu_cla_tb/ : Warning: NUMERIC_STD.TO_UNSIGNED: vector truncated
at 13762560 ns, Instance /alu_cla_tb/ : Warning: NUMERIC_STD.TO_UNSIGNED: vector truncated
at 14745600 ns, Instance /alu_cla_tb/ : Warning: NUMERIC_STD.TO_UNSIGNED: vector truncated

64210384>rem ***** test alu flags

64210384>xst -ifn alu_cla_flags.xst
Release 14.7 - xst P.20131013 (nt64)
Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.
-- > Parameter TMPDIR set to xst/projnav.tmp

Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.26 secs

-- > Parameter xsthdpdir set to xst

Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.26 secs

-- >

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=====
* Synthesis Options Summary *

-- -- Source Parameters

Input File Name : "alu_cla_flags_tb.prj"
Ignore Synthesis Constraint File : NO

-- -- Target Parameters

Output File Name : "alu_cla_flags_tb"
Output Format : NGC
Target Device : xc6slx4-3-tqg144

-- -- Source Options

Top Module Name : alu_cla_flags_tb
Automatic FSM Extraction : YES
FSM Encoding Algorithm : Auto
Safe Implementation : No
FSM Style : LUT
RAM Extraction : Yes
RAM Style : Auto
ROM Extraction : Yes
Shift Register Extraction : YES
ROM Style : Auto
Resource Sharing : YES
Asynchronous To Synchronous : NO
Shift Register Minimum Size : 2
Use DSP Block : Auto
Automatic Register Balancing : No

-- -- Target Options

LUT Combining : Auto
Reduce Control Sets : Auto
Add IO Buffers : YES
Global Maximum Fanout : 100000
Add Generic Clock Buffer(BUFG) : 16
Register Duplication : YES
Optimize Instantiated Primitives : NO
Use Clock Enable : Auto
Use Synchronous Set : Auto
Use Synchronous Reset : Auto
Pack IO Registers into IOBs : Auto
Equivalent register Removal : YES

-- -- General Options

Optimization Goal : Speed
Optimization Effort : 1
Power Reduction : NO
Keep Hierarchy : No
Netlist Hierarchy : As_Optimized
RTL Output : Yes
Global Optimization : AllClockNets
Read Cores : YES
Write Timing Constraints : NO
Cross Clock Analysis : NO
Hierarchy Separator : /
Bus Delimiter : <>
Case Specifier : Maintain
Slice Utilization Ratio : 100
BRAM Utilization Ratio : 100
DSP48 Utilization Ratio : 100
Auto BRAM Packing : NO
Slice Utilization Ratio Delta : 5

=====

=====

* HDL Parsing *

=====

Parsing VHDL file "64210384\cla_gp.vhd" into library work
Parsing entity <cla_gp>.

```

Parsing architecture <ideal> of entity <cla_gp>.
Parsing VHDL file "64210384\cla_add_n_bit.vhd" into library work
Parsing entity <cla_add_n_bit>.
Parsing architecture <NDV> of entity <cla_add_n_bit>.
Parsing VHDL file "64210384\alu_cla.vhd" into library work
Parsing entity <alu_cla>.
Parsing architecture <NDV> of entity <alu_cla>.
Parsing VHDL file "64210384\alu_cla_tb_FLAGS_IDEAL.vhd" into library work
Parsing entity <alu_cla_flags_tb>.
Parsing architecture <test_alu_flags> of entity <alu_cla_flags_tb>.

=====
* HDL Elaboration *
=====

Elaborating entity <alu_cla_flags_tb> ( architecture <test_alu_flags> ) with
generics from library <work>.

Elaborating entity <alu_cla> ( architecture <NDV> ) with generics from library
<work>.

Elaborating entity <cla_add_n_bit> ( architecture <NDV> ) with generics from
library <work>.
ERROR:HDLCompiler:890 - "64210384\alu_cla_tb_FLAGS_IDEAL.vhd" Line 144: wait
statement without UNTIL clause not supported for synthesis
Netlist alu_cla_flags_tb( 8 )( test_alu_flags ) remains a blackbox, due to errors
in its contents
-- >

Total memory usage is 4466680 kilobytes

Number of errors : 1 ( 0 filtered )
Number of warnings : 0 ( 0 filtered )
Number of infos : 0 ( 0 filtered )

64210384>fuse -incremental -o alu_cla_flags_tb_isim_beh.exe -prj
alu_cla_flags_tb.prj -top alu_cla_flags_tb
Running: \unwrapped\fuse.exe -incremental -o alu_cla_flags_tb_isim_beh.exe -prj
alu_cla_flags_tb.prj -top alu_cla_flags_tb
ISim P.20131013 ( signature 0x7708f090 )
Number of CPUs detected in this system: 8
Turning on mult-threading, number of parallel sub-compilation jobs: 16
Determining compilation order of HDL files
Parsing VHDL file "cla_gp.vhd" into library work
Parsing VHDL file "cla_add_n_bit.vhd" into library work
Parsing VHDL file "alu_cla.vhd" into library work
Parsing VHDL file "alu_cla_tb_FLAGS_IDEAL.vhd" into library work
Starting static elaboration
Completed static elaboration
Compiling package standard
Compiling package std_logic_1164
Compiling package textio
Compiling package std_logic_textio
Compiling package numeric_std
Compiling package attributes
Compiling package std_logic_misc
Compiling architecture ndv of entity cla_add_n_bit [\cla_add_n_bit( 8 )\]
Compiling architecture ndv of entity alu_cla [\alu_cla( 8 )\]
Compiling architecture test_alu_flags of entity alu_cla_flags_tb

```

Time Resolution for simulation is 1ps.
Waiting for 1 sub-compilation(s) to finish...
Compiled 12 VHDL Units
Built simulation executable alu_cla_flags_tb_isim_beh.exe
Fuse Memory Usage: 37456 KB
Fuse CPU Usage: 905 ms

64210384>alu_cla_flags_tb_isim_beh.exe -tclbatch isim.tcl -wdb
alu_cla_flags_tb_isim_beh.wdb
ISim P.20131013 (signature 0x7708f090)
WARNING: A WEBPACK license was found.
WARNING: Please use Xilinx License Configuration Manager to check out a full ISim license.
WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for more information on the differences between the Lite and the Full version.
This is a Lite version of ISim.
Time resolution is 1 ps
Simulator is doing circuit initialization process.
Finished circuit initialization process.

```
-- *****
-- **** STUDENT: 64210386
-- *****
-- KOMENTARJI K OCENI NALOGE
-- Matej Možek: Ni pripomb
-- *****
```

```
64210386>rem ***** test cla adder
```

```
64210386>if not exist "xst" mkdir xst
```

```
64210386>cd XST
```

```
64210386\xst>if not exist "projnav.tmp" mkdir "projnav.tmp"
```

```
64210386\xst>cd ..
```

```
64210386>rem ***** test cla operations
```

```
64210386>xst -ifn cla_add_n_bit.xst
Release 14.7 - xst P.20131013 ( nt64 )
Copyright ( c ) 1995-2013 Xilinx, Inc. All rights reserved.
-- > Parameter TMPDIR set to xst/projnav.tmp
```

```
Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.25 secs
```

```
-- > Parameter xsthdpdir set to xst
```

```
Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.25 secs
```

```
-- >
```

```
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```
=====
* Synthesis Options Summary *
```

```
=====
-- -- Source Parameters
```

```
Input File Name : "cla_add_n_bit.prj"
```

Ignore Synthesis Constraint File : NO

-- -- Target Parameters

Output File Name : "cla_add_n_bit"

Output Format : NGC

Target Device : xc6slx4-3-tqg144

-- -- Source Options

Top Module Name : cla_add_n_bit

Automatic FSM Extraction : YES

FSM Encoding Algorithm : Auto

Safe Implementation : No

FSM Style : LUT

RAM Extraction : Yes

RAM Style : Auto

ROM Extraction : Yes

Shift Register Extraction : YES

ROM Style : Auto

Resource Sharing : YES

Asynchronous To Synchronous : NO

Shift Register Minimum Size : 2

Use DSP Block : Auto

Automatic Register Balancing : No

-- -- Target Options

LUT Combining : Auto

Reduce Control Sets : Auto

Add IO Buffers : YES

Global Maximum Fanout : 100000

Add Generic Clock Buffer(BUFG) : 16

Register Duplication : YES

Optimize Instantiated Primitives : NO

Use Clock Enable : Auto

Use Synchronous Set : Auto

Use Synchronous Reset : Auto

Pack IO Registers into IOBs : Auto

Equivalent register Removal : YES

-- -- General Options

Optimization Goal : Speed

Optimization Effort : 1

Power Reduction : NO

Keep Hierarchy : No

Netlist Hierarchy : As_Optimized

RTL Output : Yes

Global Optimization : AllClockNets

Read Cores : YES

Write Timing Constraints : NO

Cross Clock Analysis : NO

Hierarchy Separator : /

Bus Delimiter : <>

Case Specifier : Maintain

Slice Utilization Ratio : 100

BRAM Utilization Ratio : 100

DSP48 Utilization Ratio : 100

Auto BRAM Packing : NO

Slice Utilization Ratio Delta : 5

=====

```

=====
* HDL Parsing *
=====
Parsing VHDL file "64210386\cla_gp.vhd" into library work
Parsing entity <cla_gp>.
Parsing architecture <ideal> of entity <cla_gp>.
Parsing VHDL file "64210386\cla_add_n_bit.vhd" into library work
Parsing entity <cla_add_n_bit>.
Parsing architecture <NDV> of entity <cla_add_n_bit>.

=====
* HDL Elaboration *
=====

Elaborating entity <cla_add_n_bit> ( architecture <NDV> ) with generics from
library <work>.
WARNING:HDLCompiler:634 - "64210386\cla_add_n_bit.vhd" Line 14: Net <g_ind[0]>
does not have a driver.

=====
* HDL Synthesis *
=====

Synthesizing Unit <cla_add_n_bit>.
  Related source file is "64210386\cla_add_n_bit.vhd".
  n = 8
WARNING:Xst:653 - Signal      <g_ind<0>> is used but never assigned. This
sourceless signal          will be automatically connected to value GND.
  Summary:
Unit <cla_add_n_bit> synthesized.

=====
HDL Synthesis Report

Macro Statistics
# Xors : 16
  1-bit xor2 : 16

=====

=====
* Advanced HDL Synthesis *
=====

=====
Advanced HDL Synthesis Report

Macro Statistics
# Xors : 16
  1-bit xor2 : 16

=====

=====
* Low Level Synthesis *
=====

Optimizing unit <cla_add_n_bit> ...

```

Mapping all equations...
Building and optimizing final netlist ...
Found area constraint ratio of 100 (+ 5) on block cla_add_n_bit, actual ratio is 1.

Final Macro Processing ...

=====

Final Register Report

Found no macro

=====

=====

* Partition Report *

=====

Partition Implementation Status

```
--      --      --      --      --      --      --      --      --      --      --      --
--      --      --      --      --      --      --      --      --      --      --      --
```

No Partitions were found in this design.

```
--      --      --      --      --      --      --      --      --      --      --      --
--      --      --      --      --      --      --      --      --      --      --      --
```

=====

* Design Summary *

=====

Top Level Output File Name : cla_add_n_bit.ngc

Primitive and Black Box Usage:

```
--      --      --      --      --      --      --      --      --      --      --      --
--      --      --      --      --      --      --      --      --      --      --      --
```

BELS : 23
LUT2 : 6
LUT3 : 4
LUT5 : 8
LUT6 : 5
IO Buffers : 28
IBUF : 17
OBUF : 11

Device utilization summary:

```
--      --      --      --      --      --      --      --      --      --      --      --
-
```

Selected Device : 6slx4tqg144-3

Slice Logic Utilization:

Number of Slice LUTs: 23 out of 2400 0%
Number used as Logic: 23 out of 2400 0%

Slice Logic Distribution:

Number of LUT Flip Flop pairs used: 23
Number with an unused Flip Flop: 23 out of 23 100%
Number with an unused LUT: 0 out of 23 0%

Number of fully used LUT-FF pairs: 0 out of 23 0%
Number of unique control sets: 0

IO Utilization:

Number of IOs: 28
Number of bonded IOBs: 28 out of 102 27%

Specific Feature Utilization:

```
-- -- -- -- -- -- -- -- -- -- -- -- -- --  
-  
Partition Resource Summary:  
-- -- -- -- -- -- -- -- -- -- -- -- -- --  
-
```

No Partitions were found in this design.

```
-- -- -- -- -- -- -- -- -- -- -- -- -- --  
-
```

===== Timing Report

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.
FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT
GENERATED AFTER PLACE-and-ROUTE.

Clock Information:

```
-- -- -- -- -- -- -- -- -- -- -- -- -- --  
No clock signals found in this design
```

Asynchronous Control Signals Information:

```
-- -- -- -- -- -- -- -- -- -- -- -- -- --  
-- -- -- -- -- -- -- -- -- -- -- -- -- --  
No asynchronous control signals found in this design
```

Timing Summary:

```
-- -- -- -- -- -- -- -- -- -- -- -- -- --  
Speed Grade: -3
```

Minimum period: No path found
Minimum input arrival time before clock: No path found
Maximum output required time after clock: No path found
Maximum combinational path delay: 8.399ns

Timing Details:

```
-- -- -- -- -- -- -- -- -- -- -- -- -- --  
All values displayed in nanoseconds ( ns )
```

===== Timing constraint: Default path analysis

Total number of paths / destination ports: 131 / 11

```
-- -- -- -- -- -- -- -- -- -- -- -- -- --  
-- -- -- -- -- -- -- -- -- -- -- -- -- --  
-- -- -- -- -- -- -- -- -- -- -- -- -- --
```

Delay: 8.399ns (Levels of Logic = 6)

Source: X<1> (PAD)

Destination: S<7> (PAD)

Data Path: X<1> to S<7>

Gate Net

Cell:in->out fanout Delay Delay Logical Name (Net Name)

```
--      --      --      --      --      --      --      --      --      --      --
--      --      --      --      --      --      --      --      --      --      --
--      --
IBUF:I->0 4 1.222 1.028 X_1_IBUF ( X_1_IBUF )
LUT5:I0->0 3 0.203 0.651 c_p<2>1 ( c_p<2> )
LUT5:I4->0 3 0.205 0.651 c_p<4>1 ( c_p<4> )
LUT5:I4->0 3 0.205 0.879 c_p<6>1 ( c_p<6> )
LUT3:I0->0 1 0.205 0.579 Mxor_s_sig<6>_xo<0>1 ( S_6_OBUF )
OBUF:I->0 2.571 S_6_OBUF ( S<6> )
--      --      --      --      --      --      --      --      --      --      --
--      --      --      --      --      --      --      --      --      --      --

Total 8.399ns ( 4.611ns logic, 3.788ns route )
( 54.9% logic, 45.1% route )
```

=====

Cross Clock Domains Report:

```
--      --      --      --      --      --      --      --      --      --      --
```

=====

Total REAL time to Xst completion: 9.00 secs

Total CPU time to Xst completion: 8.84 secs

-- >

Total memory usage is 4487500 kilobytes

Number of errors : 0 (0 filtered)

Number of warnings : 2 (0 filtered)

Number of infos : 0 (0 filtered)

```
64210386>fuse -incremental -o cla_add_n_bit_tb_isim_beh.exe -prj
cla_add_n_bit_tb.prj -top cla_add_n_bit_tb
Running: \unwrapped\fuse.exe -incremental -o cla_add_n_bit_tb_isim_beh.exe -prj
cla_add_n_bit_tb.prj -top cla_add_n_bit_tb
ISim P.20131013 ( signature 0x7708f090 )
Number of CPUs detected in this system: 8
Turning on mult-threading, number of parallel sub-compilation jobs: 16
Determining compilation order of HDL files
Parsing VHDL file "cla_gp.vhd" into library work
Parsing VHDL file "cla_add_n_bit.vhd" into library work
Parsing VHDL file "cla_add_n_bit_tb_IDEAL.vhd" into library work
Starting static elaboration
Completed static elaboration
Compiling package standard
Compiling package std_logic_1164
Compiling package textio
Compiling package std_logic_textio
Compiling package numeric_std
Compiling package attributes
Compiling package std_logic_misc
Compiling architecture ndv of entity cla_add_n_bit [\cla_add_n_bit( 8 )\]
Compiling architecture testbench_arch of entity cla_add_n_bit_tb
Time Resolution for simulation is 1ps.
Waiting for 1 sub-compilation( s ) to finish...
```

Compiled 10 VHDL Units
Built simulation executable cla_add_n_bit_tb_isim_beh.exe
Fuse Memory Usage: 37396 KB
Fuse CPU Usage: 921 ms

```
64210386>cla_add_n_bit_tb_isim_beh.exe -tclbatch isim.tcl -wdb
cla_add_n_bit_tb_isim_beh.wdb
ISim P.20131013 ( signature 0x7708f090 )
WARNING: A WEBPACK license was found.
WARNING: Please use Xilinx License Configuration Manager to check out a full ISim
license.
WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for
more information on the differences between the Lite and the Full version.
This is a Lite version of ISim.
Time resolution is 1 ps
Simulator is doing circuit initialization process.
Finished circuit initialization process.
```

```
64210386>rem ***** test cla flags
```

```
64210386>xst -ifn cla_add_n_bit_flags.xst
Release 14.7 - xst P.20131013 ( nt64 )
Copyright ( c ) 1995-2013 Xilinx, Inc. All rights reserved.
-- > Parameter TMPDIR set to xst/projnav.tmp
```

```
Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.24 secs
```

```
-- > Parameter xsthdpdir set to xst
```

```
Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.24 secs
```

```
-- > ERROR:Xst:438 - Can not open file : cla_add_n_bit_flags.prj
```

```
Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.27 secs
```

```
-- >
```

```
Total memory usage is 4422880 kilobytes
```

```
Number of errors : 1 ( 0 filtered )
```

```
Number of warnings : 0 ( 0 filtered )
```

```
Number of infos : 0 ( 0 filtered )
```

```
64210386>fuse -incremental -o cla_add_n_bit_tb_flags_isim_beh.exe -prj
cla_add_n_bit_flags_tb.prj -top cla_add_n_bit_flags_tb_IDEAL
Running: \unwrapped\fuse.exe -incremental -o cla_add_n_bit_tb_flags_isim_beh.exe -
prj cla_add_n_bit_flags_tb.prj -top cla_add_n_bit_flags_tb_IDEAL
ISim P.20131013 ( signature 0x7708f090 )
Number of CPUs detected in this system: 8
Turning on mult-threading, number of parallel sub-compilation jobs: 16
Determining compilation order of HDL files
Parsing VHDL file "cla_gp.vhd" into library work
Parsing VHDL file "cla_add_n_bit.vhd" into library work
Parsing VHDL file "cla_add_n_bit_flags_tb_IDEAL.vhd" into library work
Starting static elaboration
Completed static elaboration
```

```

Compiling package standard
Compiling package std_logic_1164
Compiling package textio
Compiling package std_logic_textio
Compiling package numeric_std
Compiling package attributes
Compiling package std_logic_misc
Compiling architecture ndv of entity cla_add_n_bit [\cla_add_n_bit( 8 )\]
Compiling architecture a1 of entity cla_add_n_bit_flags_tb_ideal
Time Resolution for simulation is 1ps.
Waiting for 1 sub-compilation( s ) to finish...
Compiled 10 VHDL Units
Built simulation executable cla_add_n_bit_tb_flags_isim_beh.exe
Fuse Memory Usage: 37360 KB
Fuse CPU Usage: 1030 ms

64210386>cla_add_n_bit_tb_flags_isim_beh.exe -tclbatch isim.tcl -wdb
cla_add_n_bit_flags_tb.wdb
ISim P.20131013 ( signature 0x7708f090 )
WARNING: A WEBPACK license was found.
WARNING: Please use Xilinx License Configuration Manager to check out a full ISim
license.
WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for
more information on the differences between the Lite and the Full version.
This is a Lite version of ISim.
Time resolution is 1 ps
Simulator is doing circuit initialization process.
Finished circuit initialization process.

64210386>rem ***** test alu operations

64210386>xst -ifn alu_cla.xst
Release 14.7 - xst P.20131013 ( nt64 )
Copyright ( c ) 1995-2013 Xilinx, Inc. All rights reserved.
-- > Parameter TMPDIR set to xst/projnav.tmp

Total REAL time to Xst completion: 1.00 secs
Total CPU time to Xst completion: 0.24 secs

-- > Parameter xsthdpdir set to xst

Total REAL time to Xst completion: 1.00 secs
Total CPU time to Xst completion: 0.24 secs

-- >
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```
=====
* Synthesis Options Summary *
=====
--      -- Source Parameters
Input File Name : "alu_cla.prj"
Ignore Synthesis Constraint File : NO

--      -- Target Parameters
Output File Name : "alu_cla"
Output Format : NGC
Target Device : xc6slx4-3-tqg144

--      -- Source Options
Top Module Name : alu_cla
Automatic FSM Extraction : YES
FSM Encoding Algorithm : Auto
Safe Implementation : No
FSM Style : LUT
RAM Extraction : Yes
RAM Style : Auto
ROM Extraction : Yes
Shift Register Extraction : YES
ROM Style : Auto
Resource Sharing : YES
Asynchronous To Synchronous : NO
Shift Register Minimum Size : 2
Use DSP Block : Auto
Automatic Register Balancing : No

--      -- Target Options
LUT Combining : Auto
Reduce Control Sets : Auto
Add IO Buffers : YES
Global Maximum Fanout : 100000
Add Generic Clock Buffer( BUFG ) : 16
Register Duplication : YES
Optimize Instantiated Primitives : NO
Use Clock Enable : Auto
Use Synchronous Set : Auto
Use Synchronous Reset : Auto
Pack IO Registers into IOBs : Auto
Equivalent register Removal : YES

--      -- General Options
Optimization Goal : Speed
Optimization Effort : 1
Power Reduction : NO
Keep Hierarchy : No
Netlist Hierarchy : As_Optimized
RTL Output : Yes
Global Optimization : AllClockNets
Read Cores : YES
```

Write Timing Constraints : NO

Cross Clock Analysis : NO

Hierarchy Separator : /

Bus Delimiter : <>

Case Specifier : Maintain

Slice Utilization Ratio : 100

BRAM Utilization Ratio : 100

DSP48 Utilization Ratio : 100

Auto BRAM Packing : NO

Slice Utilization Ratio Delta : 5

=====

=====

* HDL Parsing *

=====

Parsing VHDL file "64210386\cla_gp.vhd" into library work

Parsing entity <cla_gp>.

Parsing architecture <ideal> of entity <cla_gp>.

Parsing VHDL file "64210386\cla_add_n_bit.vhd" into library work

Parsing entity <cla_add_n_bit>.

Parsing architecture <NDV> of entity <cla_add_n_bit>.

Parsing VHDL file "64210386\alu_cla.vhd" into library work

Parsing entity <alu_cla>.

Parsing architecture <NDV> of entity <alu_cla>.

=====

* HDL Elaboration *

=====

Elaborating entity <alu_cla> (architecture <NDV>) with generics from library <work>.

Elaborating entity <cla_add_n_bit> (architecture <NDV>) with generics from library <work>.

WARNING:HDLCompiler:634 - "64210386\cla_add_n_bit.vhd" Line 14: Net <g_ind[0]> does not have a driver.

=====

* HDL Synthesis *

=====

Synthesizing Unit <alu_cla>.

Related source file is "64210386\alu_cla.vhd".

n = 8

Found 8-bit 12-to-1 multiplexer for signal <S> created at line 60.

Summary:

inferred 19 Multiplexer(s).

Unit <alu_cla> synthesized.

Synthesizing Unit <cla_add_n_bit>.

Related source file is "64210386\cla_add_n_bit.vhd".

n = 8

WARNING:Xst:653 - Signal <g_ind<0>> is used but never assigned. This sourceless signal will be automatically connected to value GND.

Summary:

Unit <cla_add_n_bit> synthesized.

=====

No Partitions were found in this design.

```
--      --      --      --      --      --      --      --      --      --      --      --
--      --      --
```

```
=====
* Design Summary *
=====
```

Top Level Output File Name : alu_cla.ngc

Primitive and Black Box Usage:

```
--      --      --      --      --      --      --      --      --      --      --      --
--      --      --
```

```
# BELS : 60
# LUT3 : 6
# LUT5 : 16
# LUT6 : 37
# MUXF7 : 1
# IO Buffers : 34
# IBUF : 20
# OBUF : 14
```

Device utilization summary:

```
--      --      --      --      --      --      --      --      --      --      --      --
-
```

Selected Device : 6slx4tqg144-3

Slice Logic Utilization:

Number of Slice LUTs: 59 out of 2400 2%
Number used as Logic: 59 out of 2400 2%

Slice Logic Distribution:

Number of LUT Flip Flop pairs used: 59
Number with an unused Flip Flop: 59 out of 59 100%
Number with an unused LUT: 0 out of 59 0%
Number of fully used LUT-FF pairs: 0 out of 59 0%
Number of unique control sets: 0

IO Utilization:

Number of IOs: 34
Number of bonded IOBs: 34 out of 102 33%

Specific Feature Utilization:

```
--      --      --      --      --      --      --      --      --      --      --      --
-
```

Partition Resource Summary:

```
--      --      --      --      --      --      --      --      --      --      --      --
-
```

No Partitions were found in this design.

```
--      --      --      --      --      --      --      --      --      --      --      --
-
```

```
=====
Timing Report
=====
```

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.
FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT
GENERATED AFTER PLACE-and-ROUTE.

Clock Information:

-- -- -- -- --
No clock signals found in this design

Asynchronous Control Signals Information:

-- -- -- -- --
-- -- -- -- --
No asynchronous control signals found in this design

Timing Summary:

-- -- -- -- --
Speed Grade: -3

Minimum period: No path found
Minimum input arrival time before clock: No path found
Maximum output required time after clock: No path found
Maximum combinational path delay: 11.632ns

Timing Details:

-- -- -- -- --
All values displayed in nanoseconds (ns)

=====
Timing constraint: Default path analysis

Total number of paths / destination ports: 966 / 14

-- -- -- -- --
-- -- -- -- --
-- -- -- -- --

Delay: 11.632ns (Levels of Logic = 9)

Source: F<2> (PAD)

Destination: Overflow (PAD)

Data Path: F<2> to Overflow

Gate Net

Cell:in->out fanout Delay Delay Logical Name (Net Name)

-- -- -- -- --
-- -- -- -- --
-- -- -- -- --

IBUF:I->0 36 1.222 1.693 F_2_IBUF (F_2_IBUF)
LUT6:I1->0 4 0.203 0.931 Mmux_y_sig31 (y_sig<1>)
LUT5:I1->0 3 0.203 0.651 U1/c_p<2>1 (U1/c_p<2>)
LUT5:I4->0 3 0.205 0.651 U1/c_p<4>1 (U1/c_p<4>)
LUT5:I4->0 4 0.205 0.912 U1/c_p<6>1 (U1/c_p<6>)
LUT5:I2->0 5 0.205 1.059 U1/Mxor_s_sig<7>_xo<0>1 (s_sig<7>)
LUT6:I1->0 1 0.203 0.000 Overflow_G (N16)
MUXF7:I1->0 1 0.140 0.579 Overflow (Overflow_OBUF)
OBUF:I->0 2.571 Overflow_OBUF (Overflow)

-- -- -- -- --
-- -- -- -- --

Total 11.632ns (5.157ns logic, 6.475ns route)
(44.3% logic, 55.7% route)

=====

Cross Clock Domains Report:

-- -- -- -- -- -- -- -- -- -- -- -- -- --
=====

Total REAL time to Xst completion: 10.00 secs

Total CPU time to Xst completion: 9.88 secs

-- >

Total memory usage is 4487500 kilobytes

Number of errors : 0 (0 filtered)

Number of warnings : 2 (0 filtered)

Number of infos : 0 (0 filtered)

64210386>fuse -incremental -o alu_cla_tb_isim_beh.exe -prj alu_cla_tb.prj -top alu_cla_tb

Running: \unwrapped\fuse.exe -incremental -o alu_cla_tb_isim_beh.exe -prj alu_cla_tb.prj -top alu_cla_tb

ISim P.20131013 (signature 0x7708f090)

Number of CPUs detected in this system: 8

Turning on mult-threading, number of parallel sub-compilation jobs: 16

Determining compilation order of HDL files

Parsing VHDL file "cla_gp.vhd" into library work

Parsing VHDL file "cla_add_n_bit.vhd" into library work

Parsing VHDL file "alu_cla.vhd" into library work

Parsing VHDL file "alu_cla_tb_IDEAL.vhd" into library work

Starting static elaboration

Completed static elaboration

Compiling package standard

Compiling package std_logic_1164

Compiling package textio

Compiling package std_logic_textio

Compiling package numeric_std

Compiling package attributes

Compiling package std_logic_misc

Compiling architecture ndv of entity cla_add_n_bit [\cla_add_n_bit(8)\]

Compiling architecture ndv of entity alu_cla [\alu_cla(8)\]

Compiling architecture testbench_arch of entity alu_cla_tb

Time Resolution for simulation is 1ps.

Waiting for 1 sub-compilation(s) to finish...

Compiled 12 VHDL Units

Built simulation executable alu_cla_tb_isim_beh.exe

Fuse Memory Usage: 37708 KB

Fuse CPU Usage: 921 ms

64210386>alu_cla_tb_isim_beh.exe -tclbatch isim.tcl -wdb alu_cla_tb_isim_beh.wdb

ISim P.20131013 (signature 0x7708f090)

WARNING: A WEBPACK license was found.

WARNING: Please use Xilinx License Configuration Manager to check out a full ISim license.

WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for more information on the differences between the Lite and the Full version.

This is a Lite version of ISim.

Time resolution is 1 ps

Simulator is doing circuit initialization process.

Finished circuit initialization process.

```

at 7864320 ns, Instance /alu_cla_tb/ : Warning: NUMERIC_STD.TO_UNSIGNED: vector
truncated
at 8847360 ns, Instance /alu_cla_tb/ : Warning: NUMERIC_STD.TO_UNSIGNED: vector
truncated
at 9830400 ns, Instance /alu_cla_tb/ : Warning: NUMERIC_STD.TO_UNSIGNED: vector
truncated
at 10813440 ns, Instance /alu_cla_tb/ : Warning: NUMERIC_STD.TO_UNSIGNED: vector
truncated
at 11796480 ns, Instance /alu_cla_tb/ : Warning: NUMERIC_STD.TO_UNSIGNED: vector
truncated
at 12779520 ns, Instance /alu_cla_tb/ : Warning: NUMERIC_STD.TO_UNSIGNED: vector
truncated
at 13762560 ns, Instance /alu_cla_tb/ : Warning: NUMERIC_STD.TO_UNSIGNED: vector
truncated
at 14745600 ns, Instance /alu_cla_tb/ : Warning: NUMERIC_STD.TO_UNSIGNED: vector
truncated

```

```

64210386>rem ***** test alu flags

```

```

64210386>xst -ifn alu_cla_flags.xst
Release 14.7 - xst P.20131013 ( nt64 )
Copyright ( c ) 1995-2013 Xilinx, Inc. All rights reserved.
-- > Parameter TMPDIR set to xst/projnav.tmp

```

```

Total REAL time to Xst completion: 1.00 secs
Total CPU time to Xst completion: 0.40 secs

```

```

-- > Parameter xsthdpdir set to xst

```

```

Total REAL time to Xst completion: 1.00 secs
Total CPU time to Xst completion: 0.40 secs

```

```

-- >

```

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```

=====
* Synthesis Options Summary *
=====

```

```

-- -- Source Parameters

```

```

Input File Name : "alu_cla_flags_tb.prj"

```

Ignore Synthesis Constraint File : NO

-- -- Target Parameters

Output File Name : "alu_cla_flags_tb"

Output Format : NGC

Target Device : xc6slx4-3-tqg144

-- -- Source Options

Top Module Name : alu_cla_flags_tb

Automatic FSM Extraction : YES

FSM Encoding Algorithm : Auto

Safe Implementation : No

FSM Style : LUT

RAM Extraction : Yes

RAM Style : Auto

ROM Extraction : Yes

Shift Register Extraction : YES

ROM Style : Auto

Resource Sharing : YES

Asynchronous To Synchronous : NO

Shift Register Minimum Size : 2

Use DSP Block : Auto

Automatic Register Balancing : No

-- -- Target Options

LUT Combining : Auto

Reduce Control Sets : Auto

Add IO Buffers : YES

Global Maximum Fanout : 100000

Add Generic Clock Buffer(BUFG) : 16

Register Duplication : YES

Optimize Instantiated Primitives : NO

Use Clock Enable : Auto

Use Synchronous Set : Auto

Use Synchronous Reset : Auto

Pack IO Registers into IOBs : Auto

Equivalent register Removal : YES

-- -- General Options

Optimization Goal : Speed

Optimization Effort : 1

Power Reduction : NO

Keep Hierarchy : No

Netlist Hierarchy : As_Optimized

RTL Output : Yes

Global Optimization : AllClockNets

Read Cores : YES

Write Timing Constraints : NO

Cross Clock Analysis : NO

Hierarchy Separator : /

Bus Delimiter : <>

Case Specifier : Maintain

Slice Utilization Ratio : 100

BRAM Utilization Ratio : 100

DSP48 Utilization Ratio : 100

Auto BRAM Packing : NO

Slice Utilization Ratio Delta : 5

=====

```

=====
* HDL Parsing *
=====
Parsing VHDL file "64210386\cla_gp.vhd" into library work
Parsing entity <cla_gp>.
Parsing architecture <ideal> of entity <cla_gp>.
Parsing VHDL file "64210386\cla_add_n_bit.vhd" into library work
Parsing entity <cla_add_n_bit>.
Parsing architecture <NDV> of entity <cla_add_n_bit>.
Parsing VHDL file "64210386\alu_cla.vhd" into library work
Parsing entity <alu_cla>.
Parsing architecture <NDV> of entity <alu_cla>.
Parsing VHDL file "64210386\alu_cla_tb_FLAGS_IDEAL.vhd" into library work
Parsing entity <alu_cla_flags_tb>.
Parsing architecture <test_alu_flags> of entity <alu_cla_flags_tb>.

=====
* HDL Elaboration *
=====

Elaborating entity <alu_cla_flags_tb> ( architecture <test_alu_flags> ) with
generics from library <work>.

Elaborating entity <alu_cla> ( architecture <NDV> ) with generics from library
<work>.

Elaborating entity <cla_add_n_bit> ( architecture <NDV> ) with generics from
library <work>.
WARNING:HDLCompiler:634 - "64210386\cla_add_n_bit.vhd" Line 14: Net <g_ind[0]>
does not have a driver.
ERROR:HDLCompiler:890 - "64210386\alu_cla_tb_FLAGS_IDEAL.vhd" Line 144: wait
statement without UNTIL clause not supported for synthesis
Netlist alu_cla_flags_tb( 8 )( test_alu_flags ) remains a blackbox, due to errors
in its contents
-- >

Total memory usage is 4466680 kilobytes

Number of errors : 1 ( 0 filtered )
Number of warnings : 1 ( 0 filtered )
Number of infos : 0 ( 0 filtered )

64210386>fuse -incremental -o alu_cla_flags_tb_isim_beh.exe -prj
alu_cla_flags_tb.prj -top alu_cla_flags_tb
Running: \unwrapped\fuse.exe -incremental -o alu_cla_flags_tb_isim_beh.exe -prj
alu_cla_flags_tb.prj -top alu_cla_flags_tb
ISim P.20131013 ( signature 0x7708f090 )
Number of CPUs detected in this system: 8
Turning on mult-threading, number of parallel sub-compilation jobs: 16
Determining compilation order of HDL files
Parsing VHDL file "cla_gp.vhd" into library work
Parsing VHDL file "cla_add_n_bit.vhd" into library work
Parsing VHDL file "alu_cla.vhd" into library work
Parsing VHDL file "alu_cla_tb_FLAGS_IDEAL.vhd" into library work
Starting static elaboration
Completed static elaboration
Compiling package standard
Compiling package std_logic_1164

```

```
Compiling package textio
Compiling package std_logic_textio
Compiling package numeric_std
Compiling package attributes
Compiling package std_logic_misc
Compiling architecture ndv of entity cla_add_n_bit [\cla_add_n_bit( 8 )\]
Compiling architecture ndv of entity alu_cla [\alu_cla( 8 )\]
Compiling architecture test_alu_flags of entity alu_cla_flags_tb
Time Resolution for simulation is 1ps.
Waiting for 1 sub-compilation( s ) to finish...
Compiled 12 VHDL Units
Built simulation executable alu_cla_flags_tb_isim_beh.exe
Fuse Memory Usage: 37576 KB
Fuse CPU Usage: 1015 ms

64210386>alu_cla_flags_tb_isim_beh.exe -tclbatch isim.tcl -wdb
alu_cla_flags_tb_isim_beh.wdb
ISim P.20131013 ( signature 0x7708f090 )
WARNING: A WEBPACK license was found.
WARNING: Please use Xilinx License Configuration Manager to check out a full ISim
license.
WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for
more information on the differences between the Lite and the Full version.
This is a Lite version of ISim.
Time resolution is 1 ps
Simulator is doing circuit initialization process.
Finished circuit initialization process.
```

```
-- *****
-- **** STUDENT: 64210445
-- *****
-- KOMENTARJI K OCENI NALOGE
-- Matej Možek: Ni pripomb
-- *****
```

```
64210445>rem ***** test cla adder
```

```
64210445>if not exist "xst" mkdir xst
```

```
64210445>cd XST
```

```
64210445\xst>if not exist "projnav.tmp" mkdir "projnav.tmp"
```

```
64210445\xst>cd ..
```

```
64210445>rem ***** test cla operations
```

```
64210445>xst -ifn cla_add_n_bit.xst
Release 14.7 - xst P.20131013 ( nt64 )
Copyright ( c ) 1995-2013 Xilinx, Inc. All rights reserved.
-- > Parameter TMPDIR set to xst/projnav.tmp
```

```
Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.28 secs
```

```
-- > Parameter xsthdpdir set to xst
```

```
Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.28 secs
```

```
-- >
```

```
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```
=====
* Synthesis Options Summary *
```

```
=====
-- -- Source Parameters
```

```
Input File Name : "cla_add_n_bit.prj"
```

Ignore Synthesis Constraint File : NO

-- -- Target Parameters

Output File Name : "cla_add_n_bit"

Output Format : NGC

Target Device : xc6slx4-3-tqg144

-- -- Source Options

Top Module Name : cla_add_n_bit

Automatic FSM Extraction : YES

FSM Encoding Algorithm : Auto

Safe Implementation : No

FSM Style : LUT

RAM Extraction : Yes

RAM Style : Auto

ROM Extraction : Yes

Shift Register Extraction : YES

ROM Style : Auto

Resource Sharing : YES

Asynchronous To Synchronous : NO

Shift Register Minimum Size : 2

Use DSP Block : Auto

Automatic Register Balancing : No

-- -- Target Options

LUT Combining : Auto

Reduce Control Sets : Auto

Add IO Buffers : YES

Global Maximum Fanout : 100000

Add Generic Clock Buffer(BUFG) : 16

Register Duplication : YES

Optimize Instantiated Primitives : NO

Use Clock Enable : Auto

Use Synchronous Set : Auto

Use Synchronous Reset : Auto

Pack IO Registers into IOBs : Auto

Equivalent register Removal : YES

-- -- General Options

Optimization Goal : Speed

Optimization Effort : 1

Power Reduction : NO

Keep Hierarchy : No

Netlist Hierarchy : As_Optimized

RTL Output : Yes

Global Optimization : AllClockNets

Read Cores : YES

Write Timing Constraints : NO

Cross Clock Analysis : NO

Hierarchy Separator : /

Bus Delimiter : <>

Case Specifier : Maintain

Slice Utilization Ratio : 100

BRAM Utilization Ratio : 100

DSP48 Utilization Ratio : 100

Auto BRAM Packing : NO

Slice Utilization Ratio Delta : 5

=====

```

=====
* HDL Parsing *
=====
Parsing VHDL file "64210445\cla_gp.vhd" into library work
Parsing entity <cla_gp>.
Parsing architecture <ideal> of entity <cla_gp>.
Parsing VHDL file "64210445\cla_add_n_bit.vhd" into library work
Parsing entity <cla_add_n_bit>.
Parsing architecture <NDV> of entity <cla_add_n_bit>.

=====
* HDL Elaboration *
=====

Elaborating entity <cla_add_n_bit> ( architecture <NDV> ) with generics from
library <work>.
WARNING:HDLCompiler:634 - "64210445\cla_add_n_bit.vhd" Line 14: Net <g_i[0]> does
not have a driver.

=====
* HDL Synthesis *
=====

Synthesizing Unit <cla_add_n_bit>.
  Related source file is "64210445\cla_add_n_bit.vhd".
  n = 8
WARNING:Xst:653 - Signal      <g_i<0>> is used but never assigned. This
sourceless signal          will be automatically connected to value GND.
  Summary:
Unit <cla_add_n_bit> synthesized.

=====
HDL Synthesis Report

Macro Statistics
# Xors : 16
  1-bit xor2 : 16

=====

=====
* Advanced HDL Synthesis *
=====

=====
Advanced HDL Synthesis Report

Macro Statistics
# Xors : 16
  1-bit xor2 : 16

=====

=====
* Low Level Synthesis *
=====

Optimizing unit <cla_add_n_bit> ...

```


Mapping all equations...
Building and optimizing final netlist ...
Found area constraint ratio of 100 (+ 5) on block cla_add_n_bit, actual ratio is 1.

Final Macro Processing ...

=====

Final Register Report

Found no macro

=====

=====

* Partition Report *

=====

Partition Implementation Status

```
--      --      --      --      --      --      --      --      --      --      --      --
--      --      --      --      --      --      --      --      --      --      --      --
```

No Partitions were found in this design.

```
--      --      --      --      --      --      --      --      --      --      --      --
--      --      --      --      --      --      --      --      --      --      --      --
```

=====

* Design Summary *

=====

Top Level Output File Name : cla_add_n_bit.ngc

Primitive and Black Box Usage:

```
--      --      --      --      --      --      --      --      --      --      --      --
--      --      --      --      --      --      --      --      --      --      --      --
```

BELS : 24
LUT2 : 6
LUT3 : 3
LUT5 : 6
LUT6 : 9
IO Buffers : 28
IBUF : 17
OBUF : 11

Device utilization summary:

```
--      --      --      --      --      --      --      --      --      --      --      --
-
```

Selected Device : 6slx4tqg144-3

Slice Logic Utilization:

Number of Slice LUTs: 24 out of 2400 1%
Number used as Logic: 24 out of 2400 1%

Slice Logic Distribution:

Number of LUT Flip Flop pairs used: 24
Number with an unused Flip Flop: 24 out of 24 100%
Number with an unused LUT: 0 out of 24 0%

Number of fully used LUT-FF pairs: 0 out of 24 0%
Number of unique control sets: 0

IO Utilization:

Number of IOs: 28
Number of bonded IOBs: 28 out of 102 27%

Specific Feature Utilization:

```
-- -- -- -- -- -- -- -- -- -- -- -- -- --  
-  
Partition Resource Summary:  
-- -- -- -- -- -- -- -- -- -- -- -- -- --  
-
```

No Partitions were found in this design.

```
-- -- -- -- -- -- -- -- -- -- -- -- -- --  
-
```

=====
Timing Report

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.
FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT
GENERATED AFTER PLACE-and-ROUTE.

Clock Information:

```
-- -- -- -- -- -- -- -- -- -- -- -- -- --  
No clock signals found in this design
```

Asynchronous Control Signals Information:

```
-- -- -- -- -- -- -- -- -- -- -- -- -- --  
-- -- -- -- -- -- -- -- -- -- -- -- -- --  
No asynchronous control signals found in this design
```

Timing Summary:

```
-- -- -- -- -- -- -- -- -- -- -- -- -- --  
Speed Grade: -3
```

Minimum period: No path found
Minimum input arrival time before clock: No path found
Maximum output required time after clock: No path found
Maximum combinational path delay: 9.101ns

Timing Details:

```
-- -- -- -- -- -- -- -- -- -- -- -- -- --  
All values displayed in nanoseconds ( ns )
```

=====
Timing constraint: Default path analysis

Total number of paths / destination ports: 131 / 11

```
-- -- -- -- -- -- -- -- -- -- -- -- -- --  
-- -- -- -- -- -- -- -- -- -- -- -- -- --  
-- -- -- -- -- -- -- -- -- -- -- -- -- --
```

Delay: 9.101ns (Levels of Logic = 7)

Source: Y<0> (PAD)

Destination: S<7> (PAD)

Data Path: Y<0> to S<7>

Gate Net

Cell:in->out fanout Delay Delay Logical Name (Net Name)

```
--      --      --      --      --      --      --      --      --      --      --
--      --      --      --      --      --      --      --      --      --      --
--      --
IBUF:I->0 6 1.222 0.973 Y_0_IBUF ( Y_0_IBUF )
LUT3:I0->0 2 0.205 0.617 c_sig<3>_SW0 ( N2 )
LUT5:I4->0 3 0.205 0.651 c_sig<3> ( c_sig<3> )
LUT3:I2->0 2 0.205 0.617 c_sig<6>_SW0 ( N4 )
LUT5:I4->0 2 0.205 0.845 c_sig<6> ( c_sig<6> )
LUT5:I2->0 1 0.205 0.579 Mxor_s_sig<7>_xo<0>1 ( S_7_OBUF )
OBUF:I->0 2.571 S_7_OBUF ( S<7> )
--      --      --      --      --      --      --      --      --      --      --
--      --      --      --      --      --      --      --      --      --      --
Total 9.101ns ( 4.818ns logic, 4.283ns route )
( 52.9% logic, 47.1% route )
```

=====

Cross Clock Domains Report:

```
--      --      --      --      --      --      --      --      --      --      --
--      --      --      --      --      --      --      --      --      --      --
=====
```

Total REAL time to Xst completion: 10.00 secs

Total CPU time to Xst completion: 10.23 secs

-- >

Total memory usage is 4487500 kilobytes

Number of errors : 0 (0 filtered)

Number of warnings : 2 (0 filtered)

Number of infos : 0 (0 filtered)

```
64210445>fuse -incremental -o cla_add_n_bit_tb_isim_beh.exe -prj
cla_add_n_bit_tb.prj -top cla_add_n_bit_tb
Running: \unwrapped\fuse.exe -incremental -o cla_add_n_bit_tb_isim_beh.exe -prj
cla_add_n_bit_tb.prj -top cla_add_n_bit_tb
ISim P.20131013 ( signature 0x7708f090 )
Number of CPUs detected in this system: 8
Turning on mult-threading, number of parallel sub-compilation jobs: 16
Determining compilation order of HDL files
Parsing VHDL file "cla_gp.vhd" into library work
Parsing VHDL file "cla_add_n_bit.vhd" into library work
Parsing VHDL file "cla_add_n_bit_tb_IDEAL.vhd" into library work
Starting static elaboration
Completed static elaboration
Compiling package standard
Compiling package std_logic_1164
Compiling package textio
Compiling package std_logic_textio
Compiling package numeric_std
Compiling package attributes
Compiling package std_logic_misc
Compiling architecture ndv of entity cla_add_n_bit [\cla_add_n_bit( 8 )\]
Compiling architecture testbench_arch of entity cla_add_n_bit_tb
Time Resolution for simulation is 1ps.
```

Waiting for 1 sub-compilation(s) to finish...

Compiled 10 VHDL Units

Built simulation executable cla_add_n_bit_tb_isim_beh.exe

Fuse Memory Usage: 37380 KB

Fuse CPU Usage: 999 ms

64210445>cla_add_n_bit_tb_isim_beh.exe -tclbatch isim.tcl -wdb

cla_add_n_bit_tb_isim_beh.wdb

ISim P.20131013 (signature 0x7708f090)

WARNING: A WEBPACK license was found.

WARNING: Please use Xilinx License Configuration Manager to check out a full ISim license.

WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for more information on the differences between the Lite and the Full version.

This is a Lite version of ISim.

Time resolution is 1 ps

Simulator is doing circuit initialization process.

Finished circuit initialization process.

64210445>rem ***** test cla flags

64210445>xst -ifn cla_add_n_bit_flags.xst

Release 14.7 - xst P.20131013 (nt64)

Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.

-- > Parameter TMPDIR set to xst/projnav.tmp

Total REAL time to Xst completion: 0.00 secs

Total CPU time to Xst completion: 0.25 secs

-- > Parameter xsthdpdir set to xst

Total REAL time to Xst completion: 0.00 secs

Total CPU time to Xst completion: 0.25 secs

-- > ERROR:Xst:438 - Can not open file : cla_add_n_bit_flags.prj

Total REAL time to Xst completion: 0.00 secs

Total CPU time to Xst completion: 0.28 secs

-- >

Total memory usage is 4422880 kilobytes

Number of errors : 1 (0 filtered)

Number of warnings : 0 (0 filtered)

Number of infos : 0 (0 filtered)

64210445>fuse -incremental -o cla_add_n_bit_tb_flags_isim_beh.exe -prj

cla_add_n_bit_flags_tb.prj -top cla_add_n_bit_flags_tb_IDEAL

Running: \unwrapped\fuse.exe -incremental -o cla_add_n_bit_tb_flags_isim_beh.exe -prj cla_add_n_bit_flags_tb.prj -top cla_add_n_bit_flags_tb_IDEAL

ISim P.20131013 (signature 0x7708f090)

Number of CPUs detected in this system: 8

Turning on mult-threading, number of parallel sub-compilation jobs: 16

Determining compilation order of HDL files

Parsing VHDL file "cla_gp.vhd" into library work

Parsing VHDL file "cla_add_n_bit.vhd" into library work

Parsing VHDL file "cla_add_n_bit_flags_tb_IDEAL.vhd" into library work

Starting static elaboration

```

Completed static elaboration
Compiling package standard
Compiling package std_logic_1164
Compiling package textio
Compiling package std_logic_textio
Compiling package numeric_std
Compiling package attributes
Compiling package std_logic_misc
Compiling architecture ndv of entity cla_add_n_bit [\cla_add_n_bit( 8 )\]
Compiling architecture a1 of entity cla_add_n_bit_flags_tb_ideal
Time Resolution for simulation is 1ps.
Waiting for 1 sub-compilation( s ) to finish...
Compiled 10 VHDL Units
Built simulation executable cla_add_n_bit_tb_flags_isim_beh.exe
Fuse Memory Usage: 37804 KB
Fuse CPU Usage: 968 ms

64210445>cla_add_n_bit_tb_flags_isim_beh.exe -tclbatch isim.tcl -wdb
cla_add_n_bit_flags_tb.wdb
ISim P.20131013 ( signature 0x7708f090 )
WARNING: A WEBPACK license was found.
WARNING: Please use Xilinx License Configuration Manager to check out a full ISim
license.
WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for
more information on the differences between the Lite and the Full version.
This is a Lite version of ISim.
Time resolution is 1 ps
Simulator is doing circuit initialization process.
Finished circuit initialization process.

64210445>rem ***** test alu operations

64210445>xst -ifn alu_cla.xst
Release 14.7 - xst P.20131013 ( nt64 )
Copyright ( c ) 1995-2013 Xilinx, Inc. All rights reserved.
-- > Parameter TMPDIR set to xst/projnav.tmp

Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.31 secs

-- > Parameter xsthdpdir set to xst

Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.31 secs

-- >
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```

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8.4.5) Cross Clock Domains Report

=====
* Synthesis Options Summary *
=====

-- -- Source Parameters

Input File Name : "alu_cla.prj"
Ignore Synthesis Constraint File : NO

-- -- Target Parameters

Output File Name : "alu_cla"
Output Format : NGC
Target Device : xc6slx4-3-tqg144

-- -- Source Options

Top Module Name : alu_cla
Automatic FSM Extraction : YES
FSM Encoding Algorithm : Auto
Safe Implementation : No
FSM Style : LUT
RAM Extraction : Yes
RAM Style : Auto
ROM Extraction : Yes
Shift Register Extraction : YES
ROM Style : Auto
Resource Sharing : YES
Asynchronous To Synchronous : NO
Shift Register Minimum Size : 2
Use DSP Block : Auto
Automatic Register Balancing : No

-- -- Target Options

LUT Combining : Auto
Reduce Control Sets : Auto
Add IO Buffers : YES
Global Maximum Fanout : 100000
Add Generic Clock Buffer(BUFG) : 16
Register Duplication : YES
Optimize Instantiated Primitives : NO
Use Clock Enable : Auto
Use Synchronous Set : Auto
Use Synchronous Reset : Auto
Pack IO Registers into IOBs : Auto
Equivalent register Removal : YES

-- -- General Options

Optimization Goal : Speed
Optimization Effort : 1
Power Reduction : NO
Keep Hierarchy : No
Netlist Hierarchy : As_Optimized
RTL Output : Yes
Global Optimization : AllClockNets

Read Cores : YES
Write Timing Constraints : NO
Cross Clock Analysis : NO
Hierarchy Separator : /
Bus Delimiter : <>
Case Specifier : Maintain
Slice Utilization Ratio : 100
BRAM Utilization Ratio : 100
DSP48 Utilization Ratio : 100
Auto BRAM Packing : NO
Slice Utilization Ratio Delta : 5

=====

=====

* HDL Parsing *

=====

Parsing VHDL file "64210445\cla_gp.vhd" into library work
Parsing entity <cla_gp>.
Parsing architecture <ideal> of entity <cla_gp>.
Parsing VHDL file "64210445\cla_add_n_bit.vhd" into library work
Parsing entity <cla_add_n_bit>.
Parsing architecture <NDV> of entity <cla_add_n_bit>.
Parsing VHDL file "64210445\alu_cla.vhd" into library work
Parsing entity <alu_cla>.
Parsing architecture <NDV> of entity <alu_cla>.

=====

* HDL Elaboration *

=====

Elaborating entity <alu_cla> (architecture <NDV>) with generics from library <work>.

Elaborating entity <cla_add_n_bit> (architecture <NDV>) with generics from library <work>.

WARNING:HDLCompiler:634 - "64210445\cla_add_n_bit.vhd" Line 14: Net <g_i[0]> does not have a driver.

=====

* HDL Synthesis *

=====

Synthesizing Unit <alu_cla>.

Related source file is "64210445\alu_cla.vhd".

n = 8

Found 8-bit 12-to-1 multiplexer for signal <S> created at line 67.

Summary:

inferred 19 Multiplexer(s).

Unit <alu_cla> synthesized.

Synthesizing Unit <cla_add_n_bit>.

Related source file is "64210445\cla_add_n_bit.vhd".

n = 8

WARNING:Xst:653 - Signal <g_i<0>> is used but never assigned. This sourceless signal will be automatically connected to value GND.

Summary:

Unit <cla_add_n_bit> synthesized.

```
=====
HDL Synthesis Report

Macro Statistics
# Multiplexers : 19
  1-bit 2-to-1 multiplexer : 12
  8-bit 12-to-1 multiplexer : 1
  8-bit 2-to-1 multiplexer : 6
# Xors : 17
  1-bit xor2 : 16
  8-bit xor2 : 1

=====
* Advanced HDL Synthesis *
=====

Advanced HDL Synthesis Report

Macro Statistics
# Multiplexers : 19
  1-bit 2-to-1 multiplexer : 12
  8-bit 12-to-1 multiplexer : 1
  8-bit 2-to-1 multiplexer : 6
# Xors : 17
  1-bit xor2 : 16
  8-bit xor2 : 1

=====
* Low Level Synthesis *
=====

Optimizing unit <alu_cla> ...
Optimizing unit <cla_add_n_bit> ...

Mapping all equations...
Building and optimizing final netlist ...
Found area constraint ratio of 100 ( + 5 ) on block alu_cla, actual ratio is 3.

Final Macro Processing ...

=====
Final Register Report

Found no macro

=====
* Partition Report *
=====

Partition Implementation Status
```


No Partitions were found in this design.

```
--      --      --      --      --      --      --      --      --      --      --      --
--      --      --
```

```
=====
* Design Summary *
=====
```

Top Level Output File Name : alu_cla.ngc

Primitive and Black Box Usage:

```
--      --      --      --      --      --      --      --      --      --      --      --
--      --      --
```

```
# BELS : 60
# LUT3 : 4
# LUT5 : 14
# LUT6 : 41
# MUXF7 : 1
# IO Buffers : 34
# IBUF : 20
# OBUF : 14
```

Device utilization summary:

```
--      --      --      --      --      --      --      --      --      --      --      --
-
```

Selected Device : 6slx4tqg144-3

Slice Logic Utilization:

Number of Slice LUTs: 59 out of 2400 2%
Number used as Logic: 59 out of 2400 2%

Slice Logic Distribution:

Number of LUT Flip Flop pairs used: 59
Number with an unused Flip Flop: 59 out of 59 100%
Number with an unused LUT: 0 out of 59 0%
Number of fully used LUT-FF pairs: 0 out of 59 0%
Number of unique control sets: 0

IO Utilization:

Number of IOs: 34
Number of bonded IOBs: 34 out of 102 33%

Specific Feature Utilization:

```
--      --      --      --      --      --      --      --      --      --      --      --
-
```

Partition Resource Summary:

```
--      --      --      --      --      --      --      --      --      --      --      --
-
```

No Partitions were found in this design.

```
--      --      --      --      --      --      --      --      --      --      --      --
-
```

```
=====
```

Timing Report

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.

FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT
GENERATED AFTER PLACE-and-ROUTE.

Clock Information:

-- -- -- -- --
No clock signals found in this design

Asynchronous Control Signals Information:

-- -- -- -- --
No asynchronous control signals found in this design

Timing Summary:

-- -- -- -- --
Speed Grade: -3

Minimum period: No path found

Minimum input arrival time before clock: No path found

Maximum output required time after clock: No path found

Maximum combinational path delay: 11.168ns

Timing Details:

-- -- -- -- --
All values displayed in nanoseconds (ns)

=====
Timing constraint: Default path analysis

Total number of paths / destination ports: 1146 / 14

-- -- -- -- --
-- -- -- -- --
-- -- -- -- --

Delay: 11.168ns (Levels of Logic = 8)

Source: F<2> (PAD)

Destination: Negative (PAD)

Data Path: F<2> to Negative

Gate Net

Cell: in->out fanout Delay Delay Logical Name (Net Name)

-- -- -- -- --
-- -- -- -- --
-- -- -- -- --

IBUF:I->O 35 1.222 1.679 F_2_IBUF (F_2_IBUF)

LUT6:I1->O 6 0.203 0.973 Mmux_y_sig31 (y_sig<1>)

LUT5:I2->O 4 0.205 1.028 U1/c_sig<3>2 (U1/c_sig<3>)

LUT6:I1->O 1 0.203 0.000 U1/c_sig<6>_G (N16)

MUXF7:I1->O 5 0.140 0.943 U1/c_sig<6> (U1/c_sig<6>)

LUT5:I2->O 3 0.205 1.015 U1/Mxor_s_sig<7>_xo<0>1 (s_sig<7>)

LUT6:I0->O 1 0.203 0.579 Mmux_Negative1 (Negative_OBUF)

OBUF:I->O 2.571 Negative_OBUF (Negative)

-- -- -- -- --
-- -- -- -- --

Total 11.168ns (4.952ns logic, 6.216ns route)

(44.3% logic, 55.7% route)

=====

Cross Clock Domains Report:

-- -- -- -- -- -- -- -- -- -- -- -- -- --
=====

Total REAL time to Xst completion: 10.00 secs

Total CPU time to Xst completion: 9.74 secs

-- >

Total memory usage is 4487500 kilobytes

Number of errors : 0 (0 filtered)

Number of warnings : 2 (0 filtered)

Number of infos : 0 (0 filtered)

64210445>fuse -incremental -o alu_cla_tb_isim_beh.exe -prj alu_cla_tb.prj -top alu_cla_tb

Running: \unwrapped\fuse.exe -incremental -o alu_cla_tb_isim_beh.exe -prj alu_cla_tb.prj -top alu_cla_tb

ISim P.20131013 (signature 0x7708f090)

Number of CPUs detected in this system: 8

Turning on mult-threading, number of parallel sub-compilation jobs: 16

Determining compilation order of HDL files

Parsing VHDL file "cla_gp.vhd" into library work

Parsing VHDL file "cla_add_n_bit.vhd" into library work

Parsing VHDL file "alu_cla.vhd" into library work

Parsing VHDL file "alu_cla_tb_IDEAL.vhd" into library work

Starting static elaboration

Completed static elaboration

Compiling package standard

Compiling package std_logic_1164

Compiling package textio

Compiling package std_logic_textio

Compiling package numeric_std

Compiling package attributes

Compiling package std_logic_misc

Compiling architecture ndv of entity cla_add_n_bit [\cla_add_n_bit(8)\]

Compiling architecture ndv of entity alu_cla [\alu_cla(8)\]

Compiling architecture testbench_arch of entity alu_cla_tb

Time Resolution for simulation is 1ps.

Compiled 12 VHDL Units

Built simulation executable alu_cla_tb_isim_beh.exe

Fuse Memory Usage: 37600 KB

Fuse CPU Usage: 967 ms

64210445>alu_cla_tb_isim_beh.exe -tclbatch isim.tcl -wdb alu_cla_tb_isim_beh.wdb

ISim P.20131013 (signature 0x7708f090)

WARNING: A WEBPACK license was found.

WARNING: Please use Xilinx License Configuration Manager to check out a full ISim license.

WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for more information on the differences between the Lite and the Full version.

This is a Lite version of ISim.

Time resolution is 1 ps

Simulator is doing circuit initialization process.

Finished circuit initialization process.

at 7864320 ns, Instance /alu_cla_tb/ : Warning: NUMERIC_STD.TO_UNSIGNED: vector truncated

at 8847360 ns, Instance /alu_cla_tb/ : Warning: NUMERIC_STD.TO_UNSIGNED: vector truncated
at 9830400 ns, Instance /alu_cla_tb/ : Warning: NUMERIC_STD.TO_UNSIGNED: vector truncated
at 10813440 ns, Instance /alu_cla_tb/ : Warning: NUMERIC_STD.TO_UNSIGNED: vector truncated
at 11796480 ns, Instance /alu_cla_tb/ : Warning: NUMERIC_STD.TO_UNSIGNED: vector truncated
at 12779520 ns, Instance /alu_cla_tb/ : Warning: NUMERIC_STD.TO_UNSIGNED: vector truncated
at 13762560 ns, Instance /alu_cla_tb/ : Warning: NUMERIC_STD.TO_UNSIGNED: vector truncated
at 14745600 ns, Instance /alu_cla_tb/ : Warning: NUMERIC_STD.TO_UNSIGNED: vector truncated

64210445>rem ***** test alu flags

64210445>xst -ifn alu_cla_flags.xst
Release 14.7 - xst P.20131013 (nt64)
Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.
-- > Parameter TMPDIR set to xst/projnav.tmp

Total REAL time to Xst completion: 1.00 secs
Total CPU time to Xst completion: 0.25 secs

-- > Parameter xsthdpdir set to xst

Total REAL time to Xst completion: 1.00 secs
Total CPU time to Xst completion: 0.25 secs

-- >

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 - 8.4.5) Cross Clock Domains Report

=====

* Synthesis Options Summary *

=====

-- -- Source Parameters

Input File Name : "alu_cla_flags_tb.prj"

Ignore Synthesis Constraint File : NO

```
--      -- Target Parameters
Output File Name : "alu_cla_flags_tb"
Output Format : NGC
Target Device : xc6slx4-3-tqg144
```

```
--      -- Source Options
Top Module Name : alu_cla_flags_tb
Automatic FSM Extraction : YES
FSM Encoding Algorithm : Auto
Safe Implementation : No
FSM Style : LUT
RAM Extraction : Yes
RAM Style : Auto
ROM Extraction : Yes
Shift Register Extraction : YES
ROM Style : Auto
Resource Sharing : YES
Asynchronous To Synchronous : NO
Shift Register Minimum Size : 2
Use DSP Block : Auto
Automatic Register Balancing : No
```

```
--      -- Target Options
LUT Combining : Auto
Reduce Control Sets : Auto
Add IO Buffers : YES
Global Maximum Fanout : 100000
Add Generic Clock Buffer( BUFG ) : 16
Register Duplication : YES
Optimize Instantiated Primitives : NO
Use Clock Enable : Auto
Use Synchronous Set : Auto
Use Synchronous Reset : Auto
Pack IO Registers into IOBs : Auto
Equivalent register Removal : YES
```

```
--      -- General Options
Optimization Goal : Speed
Optimization Effort : 1
Power Reduction : NO
Keep Hierarchy : No
Netlist Hierarchy : As_Optimized
RTL Output : Yes
Global Optimization : AllClockNets
Read Cores : YES
Write Timing Constraints : NO
Cross Clock Analysis : NO
Hierarchy Separator : /
Bus Delimiter : <>
Case Specifier : Maintain
Slice Utilization Ratio : 100
BRAM Utilization Ratio : 100
DSP48 Utilization Ratio : 100
Auto BRAM Packing : NO
Slice Utilization Ratio Delta : 5
```

=====

=====

* HDL Parsing *

```
=====
Parsing VHDL file "64210445\cla_gp.vhd" into library work
Parsing entity <cla_gp>.
Parsing architecture <ideal> of entity <cla_gp>.
Parsing VHDL file "64210445\cla_add_n_bit.vhd" into library work
Parsing entity <cla_add_n_bit>.
Parsing architecture <NDV> of entity <cla_add_n_bit>.
Parsing VHDL file "64210445\alu_cla.vhd" into library work
Parsing entity <alu_cla>.
Parsing architecture <NDV> of entity <alu_cla>.
Parsing VHDL file "64210445\alu_cla_tb_FLAGS_IDEAL.vhd" into library work
Parsing entity <alu_cla_flags_tb>.
Parsing architecture <test_alu_flags> of entity <alu_cla_flags_tb>.
```

* HDL Elaboration *

```
=====
Elaborating entity <alu_cla_flags_tb> ( architecture <test_alu_flags> ) with
generics from library <work>.
```

```
Elaborating entity <alu_cla> ( architecture <NDV> ) with generics from library
<work>.
```

```
Elaborating entity <cla_add_n_bit> ( architecture <NDV> ) with generics from
library <work>.
```

WARNING:HDLCompiler:634 - "64210445\cla_add_n_bit.vhd" Line 14: Net <g_i[0]> does not have a driver.

ERROR:HDLCompiler:890 - "64210445\alu_cla_tb_FLAGS_IDEAL.vhd" Line 144: wait statement without UNTIL clause not supported for synthesis

Netlist alu_cla_flags_tb(8)(test_alu_flags) remains a blackbox, due to errors in its contents

-- >

Total memory usage is 4466680 kilobytes

Number of errors : 1 (0 filtered)

Number of warnings : 1 (0 filtered)

Number of infos : 0 (0 filtered)

```
64210445>fuse -incremental -o alu_cla_flags_tb_isim_beh.exe -prj
alu_cla_flags_tb.prj -top alu_cla_flags_tb
Running: \unwrapped\fuse.exe -incremental -o alu_cla_flags_tb_isim_beh.exe -prj
alu_cla_flags_tb.prj -top alu_cla_flags_tb
ISim P.20131013 ( signature 0x7708f090 )
```

Number of CPUs detected in this system: 8

Turning on mult-threading, number of parallel sub-compilation jobs: 16

Determining compilation order of HDL files

Parsing VHDL file "cla_gp.vhd" into library work

Parsing VHDL file "cla_add_n_bit.vhd" into library work

Parsing VHDL file "alu_cla.vhd" into library work

Parsing VHDL file "alu_cla_tb_FLAGS_IDEAL.vhd" into library work

Starting static elaboration

Completed static elaboration

Compiling package standard

Compiling package std_logic_1164

Compiling package textio

Compiling package std_logic_textio

```
Compiling package numeric_std
Compiling package attributes
Compiling package std_logic_misc
Compiling architecture ndv of entity cla_add_n_bit [\cla_add_n_bit( 8 )\]
Compiling architecture ndv of entity alu_cla [\alu_cla( 8 )\]
Compiling architecture test_alu_flags of entity alu_cla_flags_tb
Time Resolution for simulation is 1ps.
Waiting for 1 sub-compilation( s ) to finish...
Compiled 12 VHDL Units
Built simulation executable alu_cla_flags_tb_isim_beh.exe
Fuse Memory Usage: 37544 KB
Fuse CPU Usage: 952 ms

64210445>alu_cla_flags_tb_isim_beh.exe -tclbatch isim.tcl -wdb
alu_cla_flags_tb_isim_beh.wdb
ISim P.20131013 ( signature 0x7708f090 )
WARNING: A WEBPACK license was found.
WARNING: Please use Xilinx License Configuration Manager to check out a full ISim
license.
WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for
more information on the differences between the Lite and the Full version.
This is a Lite version of ISim.
Time resolution is 1 ps
Simulator is doing circuit initialization process.
Finished circuit initialization process.
```

```
-- *****
-- **** STUDENT: 64210455
-- *****
-- KOMENTARJI K OCENI NALOGE
-- Matej Možek: Ni pripomb
-- *****
```

```
64210455>rem ***** test cla adder
```

```
64210455>if not exist "xst" mkdir xst
```

```
64210455>cd XST
```

```
64210455\xst>if not exist "projnav.tmp" mkdir "projnav.tmp"
```

```
64210455\xst>cd ..
```

```
64210455>rem ***** test cla operations
```

```
64210455>xst -ifn cla_add_n_bit.xst
Release 14.7 - xst P.20131013 ( nt64 )
Copyright ( c ) 1995-2013 Xilinx, Inc. All rights reserved.
-- > Parameter TMPDIR set to xst/projnav.tmp
```

```
Total REAL time to Xst completion: 1.00 secs
Total CPU time to Xst completion: 0.29 secs
```

```
-- > Parameter xsthdpdir set to xst
```

```
Total REAL time to Xst completion: 1.00 secs
Total CPU time to Xst completion: 0.30 secs
```

```
-- >
```

```
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```
=====
* Synthesis Options Summary *
```

```
=====
-- -- Source Parameters
```

```
Input File Name : "cla_add_n_bit.prj"
```


Ignore Synthesis Constraint File : NO

-- -- Target Parameters

Output File Name : "cla_add_n_bit"

Output Format : NGC

Target Device : xc6slx4-3-tqg144

-- -- Source Options

Top Module Name : cla_add_n_bit

Automatic FSM Extraction : YES

FSM Encoding Algorithm : Auto

Safe Implementation : No

FSM Style : LUT

RAM Extraction : Yes

RAM Style : Auto

ROM Extraction : Yes

Shift Register Extraction : YES

ROM Style : Auto

Resource Sharing : YES

Asynchronous To Synchronous : NO

Shift Register Minimum Size : 2

Use DSP Block : Auto

Automatic Register Balancing : No

-- -- Target Options

LUT Combining : Auto

Reduce Control Sets : Auto

Add IO Buffers : YES

Global Maximum Fanout : 100000

Add Generic Clock Buffer(BUFG) : 16

Register Duplication : YES

Optimize Instantiated Primitives : NO

Use Clock Enable : Auto

Use Synchronous Set : Auto

Use Synchronous Reset : Auto

Pack IO Registers into IOBs : Auto

Equivalent register Removal : YES

-- -- General Options

Optimization Goal : Speed

Optimization Effort : 1

Power Reduction : NO

Keep Hierarchy : No

Netlist Hierarchy : As_Optimized

RTL Output : Yes

Global Optimization : AllClockNets

Read Cores : YES

Write Timing Constraints : NO

Cross Clock Analysis : NO

Hierarchy Separator : /

Bus Delimiter : <>

Case Specifier : Maintain

Slice Utilization Ratio : 100

BRAM Utilization Ratio : 100

DSP48 Utilization Ratio : 100

Auto BRAM Packing : NO

Slice Utilization Ratio Delta : 5

=====

```

=====
* HDL Parsing *
=====
Parsing VHDL file "64210455\cla_gp.vhd" into library work
Parsing entity <cla_gp>.
Parsing architecture <ideal> of entity <cla_gp>.
Parsing VHDL file "64210455\cla_add_n_bit.vhd" into library work
Parsing entity <cla_add_n_bit>.
Parsing architecture <arch> of entity <cla_add_n_bit>.
ERROR:HDLCompiler:806 - "64210455\cla_add_n_bit.vhd" Line 59: Syntax error near
". ".
ERROR:HDLCompiler:854 - "64210455\cla_add_n_bit.vhd" Line 18: Unit <arch> ignored
due to previous errors.
VHDL file 64210455\cla_add_n_bit.vhd ignored due to errors
-- >

```

Total memory usage is 4450488 kilobytes

Number of errors : 2 (0 filtered)

Number of warnings : 0 (0 filtered)

Number of infos : 0 (0 filtered)

```

64210455>fuse -incremental -o cla_add_n_bit_tb_isim_beh.exe -prj
cla_add_n_bit_tb.prj -top cla_add_n_bit_tb
Running: \unwrapped\fuse.exe -incremental -o cla_add_n_bit_tb_isim_beh.exe -prj
cla_add_n_bit_tb.prj -top cla_add_n_bit_tb
ISim P.20131013 ( signature 0x7708f090 )
Number of CPUs detected in this system: 8
Turning on mult-threading, number of parallel sub-compilation jobs: 16
Determining compilation order of HDL files
Parsing VHDL file "cla_gp.vhd" into library work
Parsing VHDL file "cla_add_n_bit.vhd" into library work
VHDL file cla_add_n_bit.vhd ignored due to errors

```

```

64210455>cla_add_n_bit_tb_isim_beh.exe -tclbatch isim.tcl -wdb
cla_add_n_bit_tb_isim_beh.wdb

```

```

64210455>rem ***** test cla flags

```

```

64210455>xst -ifn cla_add_n_bit_flags.xst
Release 14.7 - xst P.20131013 ( nt64 )
Copyright ( c ) 1995-2013 Xilinx, Inc. All rights reserved.
-- > Parameter TMPDIR set to xst/projnav.tmp

```

```

Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.37 secs

```

```

-- > Parameter xsthdpdir set to xst

```

```

Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.37 secs

```

```

-- > ERROR:Xst:438 - Can not open file : cla_add_n_bit_flags.prj

```

```

Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.42 secs

```

```

-- >

```

Total memory usage is 4422880 kilobytes

Number of errors : 1 (0 filtered)

Number of warnings : 0 (0 filtered)

Number of infos : 0 (0 filtered)

```
64210455>fuse -incremental -o cla_add_n_bit_tb_flags_isim_beh.exe -prj
cla_add_n_bit_flags_tb.prj -top cla_add_n_bit_flags_tb_IDEAL
Running: \unwrapped\fuse.exe -incremental -o cla_add_n_bit_tb_flags_isim_beh.exe -
prj cla_add_n_bit_flags_tb.prj -top cla_add_n_bit_flags_tb_IDEAL
ISim P.20131013 ( signature 0x7708f090 )
Number of CPUs detected in this system: 8
Turning on mult-threading, number of parallel sub-compilation jobs: 16
Determining compilation order of HDL files
Parsing VHDL file "cla_gp.vhd" into library work
Parsing VHDL file "cla_add_n_bit.vhd" into library work
VHDL file cla_add_n_bit.vhd ignored due to errors
```

```
64210455>cla_add_n_bit_tb_flags_isim_beh.exe -tclbatch isim.tcl -wdb
cla_add_n_bit_flags_tb.wdb
```

```
64210455>rem ***** test alu operations
```

```
64210455>xst -ifn alu_cla.xst
Release 14.7 - xst P.20131013 ( nt64 )
Copyright ( c ) 1995-2013 Xilinx, Inc. All rights reserved.
-- > Parameter TMPDIR set to xst/projnav.tmp
```

```
Total REAL time to Xst completion: 1.00 secs
Total CPU time to Xst completion: 0.26 secs
```

```
-- > Parameter xsthdpdir set to xst
```

```
Total REAL time to Xst completion: 1.00 secs
Total CPU time to Xst completion: 0.27 secs
```

```
-- >
```

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 - 8.4.4) Timing Details
 - 8.4.5) Cross Clock Domains Report

```

=====
* Synthesis Options Summary *
=====
--      -- Source Parameters
Input File Name : "alu_cla.prj"
Ignore Synthesis Constraint File : NO

--      -- Target Parameters
Output File Name : "alu_cla"
Output Format : NGC
Target Device : xc6slx4-3-tqg144

--      -- Source Options
Top Module Name : alu_cla
Automatic FSM Extraction : YES
FSM Encoding Algorithm : Auto
Safe Implementation : No
FSM Style : LUT
RAM Extraction : Yes
RAM Style : Auto
ROM Extraction : Yes
Shift Register Extraction : YES
ROM Style : Auto
Resource Sharing : YES
Asynchronous To Synchronous : NO
Shift Register Minimum Size : 2
Use DSP Block : Auto
Automatic Register Balancing : No

--      -- Target Options
LUT Combining : Auto
Reduce Control Sets : Auto
Add IO Buffers : YES
Global Maximum Fanout : 100000
Add Generic Clock Buffer( BUFG ) : 16
Register Duplication : YES
Optimize Instantiated Primitives : NO
Use Clock Enable : Auto
Use Synchronous Set : Auto
Use Synchronous Reset : Auto
Pack IO Registers into IOBs : Auto
Equivalent register Removal : YES

--      -- General Options
Optimization Goal : Speed
Optimization Effort : 1
Power Reduction : NO
Keep Hierarchy : No
Netlist Hierarchy : As_Optimized
RTL Output : Yes
Global Optimization : AllClockNets
Read Cores : YES
Write Timing Constraints : NO
Cross Clock Analysis : NO
Hierarchy Separator : /
Bus Delimiter : <>
Case Specifier : Maintain
Slice Utilization Ratio : 100
BRAM Utilization Ratio : 100

```

DSP48 Utilization Ratio : 100
Auto BRAM Packing : NO
Slice Utilization Ratio Delta : 5

```
=====
=====
* HDL Parsing *
=====
Parsing VHDL file "64210455\cla_gp.vhd" into library work
Parsing entity <cla_gp>.
Parsing architecture <ideal> of entity <cla_gp>.
Parsing VHDL file "64210455\cla_add_n_bit.vhd" into library work
Parsing entity <cla_add_n_bit>.
Parsing architecture <arch> of entity <cla_add_n_bit>.
ERROR:HDLCompiler:806 - "64210455\cla_add_n_bit.vhd" Line 59: Syntax error near
".".
ERROR:HDLCompiler:854 - "64210455\cla_add_n_bit.vhd" Line 18: Unit <arch> ignored
due to previous errors.
VHDL file 64210455\cla_add_n_bit.vhd ignored due to errors
-- >
```

Total memory usage is 4450488 kilobytes

Number of errors : 2 (0 filtered)

Number of warnings : 0 (0 filtered)

Number of infos : 0 (0 filtered)

64210455>fuse -incremental -o alu_cla_tb_isim_beh.exe -prj alu_cla_tb.prj -top
alu_cla_tb

Running: \unwrapped\fuse.exe -incremental -o alu_cla_tb_isim_beh.exe -prj
alu_cla_tb.prj -top alu_cla_tb

ISim P.20131013 (signature 0x7708f090)

Number of CPUs detected in this system: 8

Turning on mult-threading, number of parallel sub-compilation jobs: 16

Determining compilation order of HDL files

Parsing VHDL file "cla_gp.vhd" into library work

Parsing VHDL file "cla_add_n_bit.vhd" into library work

VHDL file cla_add_n_bit.vhd ignored due to errors

64210455>alu_cla_tb_isim_beh.exe -tclbatch isim.tcl -wdb alu_cla_tb_isim_beh.wdb

64210455>rem ***** test alu flags

64210455>xst -ifn alu_cla_flags.xst

Release 14.7 - xst P.20131013 (nt64)

Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.

-- > Parameter TMPDIR set to xst/projnav.tmp

Total REAL time to Xst completion: 0.00 secs

Total CPU time to Xst completion: 0.25 secs

-- > Parameter xsthdpdir set to xst

Total REAL time to Xst completion: 0.00 secs

Total CPU time to Xst completion: 0.25 secs

-- >

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 - 8.4.4) Timing Details
 - 8.4.5) Cross Clock Domains Report

```
=====
* Synthesis Options Summary *
=====
--      -- Source Parameters
Input File Name : "alu_cla_flags_tb.prj"
Ignore Synthesis Constraint File : NO

--      -- Target Parameters
Output File Name : "alu_cla_flags_tb"
Output Format : NGC
Target Device : xc6slx4-3-tqg144

--      -- Source Options
Top Module Name : alu_cla_flags_tb
Automatic FSM Extraction : YES
FSM Encoding Algorithm : Auto
Safe Implementation : No
FSM Style : LUT
RAM Extraction : Yes
RAM Style : Auto
ROM Extraction : Yes
Shift Register Extraction : YES
ROM Style : Auto
Resource Sharing : YES
Asynchronous To Synchronous : NO
Shift Register Minimum Size : 2
Use DSP Block : Auto
Automatic Register Balancing : No

--      -- Target Options
LUT Combining : Auto
Reduce Control Sets : Auto
Add IO Buffers : YES
Global Maximum Fanout : 100000
Add Generic Clock Buffer( BUFG ) : 16
Register Duplication : YES
Optimize Instantiated Primitives : NO
Use Clock Enable : Auto
Use Synchronous Set : Auto
```

Use Synchronous Reset : Auto
Pack IO Registers into IOBs : Auto
Equivalent register Removal : YES

-- -- **General Options**

Optimization Goal : Speed
Optimization Effort : 1
Power Reduction : NO
Keep Hierarchy : No
Netlist Hierarchy : As_Optimized
RTL Output : Yes
Global Optimization : AllClockNets
Read Cores : YES
Write Timing Constraints : NO
Cross Clock Analysis : NO
Hierarchy Separator : /
Bus Delimiter : <>
Case Specifier : Maintain
Slice Utilization Ratio : 100
BRAM Utilization Ratio : 100
DSP48 Utilization Ratio : 100
Auto BRAM Packing : NO
Slice Utilization Ratio Delta : 5

=====

=====

* HDL Parsing *

=====

Parsing VHDL file "64210455\cla_gp.vhd" into library work
Parsing entity <cla_gp>.
Parsing architecture <ideal> of entity <cla_gp>.
Parsing VHDL file "64210455\cla_add_n_bit.vhd" into library work
Parsing entity <cla_add_n_bit>.
Parsing architecture <arch> of entity <cla_add_n_bit>.
ERROR:HDLCompiler:806 - "64210455\cla_add_n_bit.vhd" Line 59: Syntax error near
".".
ERROR:HDLCompiler:854 - "64210455\cla_add_n_bit.vhd" Line 18: Unit <arch> ignored
due to previous errors.
VHDL file 64210455\cla_add_n_bit.vhd ignored due to errors
-- >

Total memory usage is 4450488 kilobytes

Number of errors : 2 (0 filtered)

Number of warnings : 0 (0 filtered)

Number of infos : 0 (0 filtered)

64210455>fuse -incremental -o alu_cla_flags_tb_isim_beh.exe -prj
alu_cla_flags_tb.prj -top alu_cla_flags_tb
Running: \unwrapped\fuse.exe -incremental -o alu_cla_flags_tb_isim_beh.exe -prj
alu_cla_flags_tb.prj -top alu_cla_flags_tb
ISim P.20131013 (signature 0x7708f090)
Number of CPUs detected in this system: 8
Turning on mult-threading, number of parallel sub-compilation jobs: 16
Determining compilation order of HDL files
Parsing VHDL file "cla_gp.vhd" into library work
Parsing VHDL file "cla_add_n_bit.vhd" into library work
VHDL file cla_add_n_bit.vhd ignored due to errors

```
64210455>alu_cla_flags_tb_isim_beh.exe -tclbatch isim.tcl -wdb  
alu_cla_flags_tb_isim_beh.wdb
```



```
-- *****
-- **** STUDENT: 64210457
-- *****
-- KOMENTARJI K OCENI NALOGE
-- Matej Možek: Ni pripomb
-- *****
```

```
64210457>rem ***** test cla adder
```

```
64210457>if not exist "xst" mkdir xst
```

```
64210457>cd XST
```

```
64210457\xst>if not exist "projnav.tmp" mkdir "projnav.tmp"
```

```
64210457\xst>cd ..
```

```
64210457>rem ***** test cla operations
```

```
64210457>xst -ifn cla_add_n_bit.xst
Release 14.7 - xst P.20131013 ( nt64 )
Copyright ( c ) 1995-2013 Xilinx, Inc. All rights reserved.
-- > Parameter TMPDIR set to xst/projnav.tmp
```

```
Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.28 secs
```

```
-- > Parameter xsthdpdir set to xst
```

```
Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.29 secs
```

```
-- >
```

```
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 - 8.4.4) Timing Details
 - 8.4.5) Cross Clock Domains Report

```
=====
* Synthesis Options Summary *
```

```
-- -- Source Parameters
```

```
Input File Name : "cla_add_n_bit.prj"
```

Ignore Synthesis Constraint File : NO

-- -- Target Parameters

Output File Name : "cla_add_n_bit"

Output Format : NGC

Target Device : xc6slx4-3-tqg144

-- -- Source Options

Top Module Name : cla_add_n_bit

Automatic FSM Extraction : YES

FSM Encoding Algorithm : Auto

Safe Implementation : No

FSM Style : LUT

RAM Extraction : Yes

RAM Style : Auto

ROM Extraction : Yes

Shift Register Extraction : YES

ROM Style : Auto

Resource Sharing : YES

Asynchronous To Synchronous : NO

Shift Register Minimum Size : 2

Use DSP Block : Auto

Automatic Register Balancing : No

-- -- Target Options

LUT Combining : Auto

Reduce Control Sets : Auto

Add IO Buffers : YES

Global Maximum Fanout : 100000

Add Generic Clock Buffer(BUFG) : 16

Register Duplication : YES

Optimize Instantiated Primitives : NO

Use Clock Enable : Auto

Use Synchronous Set : Auto

Use Synchronous Reset : Auto

Pack IO Registers into IOBs : Auto

Equivalent register Removal : YES

-- -- General Options

Optimization Goal : Speed

Optimization Effort : 1

Power Reduction : NO

Keep Hierarchy : No

Netlist Hierarchy : As_Optimized

RTL Output : Yes

Global Optimization : AllClockNets

Read Cores : YES

Write Timing Constraints : NO

Cross Clock Analysis : NO

Hierarchy Separator : /

Bus Delimiter : <>

Case Specifier : Maintain

Slice Utilization Ratio : 100

BRAM Utilization Ratio : 100

DSP48 Utilization Ratio : 100

Auto BRAM Packing : NO

Slice Utilization Ratio Delta : 5

=====

```

=====
* HDL Parsing *
=====
Parsing VHDL file "64210457\cla_gp.vhd" into library work
Parsing entity <cla_gp>.
Parsing architecture <ideal> of entity <cla_gp>.
Parsing VHDL file "64210457\cla_add_n_bit.vhd" into library work
Parsing entity <cla_add_n_bit>.
Parsing architecture <NDV> of entity <cla_add_n_bit>.

=====
* HDL Elaboration *
=====

Elaborating entity <cla_add_n_bit> ( architecture <NDV> ) with generics from
library <work>.

=====
* HDL Synthesis *
=====

Synthesizing Unit <cla_add_n_bit>.
Related source file is "64210457\cla_add_n_bit.vhd".
  n = 8
  Summary:
Unit <cla_add_n_bit> synthesized.

=====
HDL Synthesis Report

Macro Statistics
# Xors : 16
  1-bit xor2 : 16

=====

=====
* Advanced HDL Synthesis *
=====

=====
Advanced HDL Synthesis Report

Macro Statistics
# Xors : 16
  1-bit xor2 : 16

=====

=====
* Low Level Synthesis *
=====

Optimizing unit <cla_add_n_bit> ...

Mapping all equations...
Building and optimizing final netlist ...

```

Found area constraint ratio of 100 (+ 5) on block cla_add_n_bit, actual ratio is 1.

Final Macro Processing ...

=====
Final Register Report

Found no macro

=====
* Partition Report *
=====

Partition Implementation Status

-- -- -- -- -- -- -- -- -- -- -- -- -- --
-- -- -

No Partitions were found in this design.

-- -- -- -- -- -- -- -- -- -- -- -- -- --
-- -- -

=====
* Design Summary *
=====

Top Level Output File Name : cla_add_n_bit.ngc

Primitive and Black Box Usage:

-- -- -- -- -- -- -- -- -- -- -- -- -- --
-- -- -

BELS : 24
LUT2 : 6
LUT3 : 3
LUT5 : 6
LUT6 : 9
IO Buffers : 28
IBUF : 17
OBUF : 11

Device utilization summary:

-- -- -- -- -- -- -- -- -- -- -- -- -- --
-

Selected Device : 6slx4tqg144-3

Slice Logic Utilization:

Number of Slice LUTs: 24 out of 2400 1%
Number used as Logic: 24 out of 2400 1%

Slice Logic Distribution:

Number of LUT Flip Flop pairs used: 24
Number with an unused Flip Flop: 24 out of 24 100%
Number with an unused LUT: 0 out of 24 0%
Number of fully used LUT-FF pairs: 0 out of 24 0%
Number of unique control sets: 0

IO Utilization:

Number of IOs: 28

Number of bonded IOBs: 28 out of 102 27%

Specific Feature Utilization:

```
-- -- -- -- -- -- -- -- -- -- -- -- -- --
-
```

Partition Resource Summary:

```
-- -- -- -- -- -- -- -- -- -- -- -- -- --
-
```

No Partitions were found in this design.

```
-- -- -- -- -- -- -- -- -- -- -- -- -- --
-
```

=====
Timing Report

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.

FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT
GENERATED AFTER PLACE-and-ROUTE.

Clock Information:

```
-- -- -- -- -- -- -- -- -- -- -- -- -- --
```

No clock signals found in this design

Asynchronous Control Signals Information:

```
-- -- -- -- -- -- -- -- -- -- -- -- -- --
-- -- -- -- -- -- -- -- -- -- -- -- -- --
```

No asynchronous control signals found in this design

Timing Summary:

```
-- -- -- -- -- -- -- -- -- -- -- -- -- --
```

Speed Grade: -3

Minimum period: No path found

Minimum input arrival time before clock: No path found

Maximum output required time after clock: No path found

Maximum combinational path delay: 9.101ns

Timing Details:

```
-- -- -- -- -- -- -- -- -- -- -- -- -- --
```

All values displayed in nanoseconds (ns)

=====
Timing constraint: Default path analysis

Total number of paths / destination ports: 131 / 11

```
-- -- -- -- -- -- -- -- -- -- -- -- -- --
-- -- -- -- -- -- -- -- -- -- -- -- -- --
-- -- -- -- -- -- -- -- -- -- -- -- -- --
```

Delay: 9.101ns (Levels of Logic = 7)

Source: Y<0> (PAD)

Destination: S<7> (PAD)

Data Path: Y<0> to S<7>

Gate Net

Cell:in->out fanout Delay Delay Logical Name (Net Name)

```

--      --      --      --      --      --      --      --      --      --      --
--      --      --      --      --      --      --      --      --      --      --
--      --
IBUF:I->0 6 1.222 0.973 Y_0_IBUF ( Y_0_IBUF )
LUT3:I0->0 2 0.205 0.617 C<3>_SW0 ( N2 )
LUT5:I4->0 3 0.205 0.651 C<3> ( C<3> )
LUT3:I2->0 2 0.205 0.617 C<6>_SW0 ( N4 )
LUT5:I4->0 2 0.205 0.845 C<6> ( C<6> )
LUT5:I2->0 1 0.205 0.579 Mxor_S_sig<7>_xo<0>1 ( S_7_OBUF )
OBUF:I->0 2.571 S_7_OBUF ( S<7> )
--      --      --      --      --      --      --      --      --      --      --
--      --      --      --      --      --      --      --      --      --      --
Total 9.101ns ( 4.818ns logic, 4.283ns route )
( 52.9% logic, 47.1% route )

```

Cross Clock Domains Report:

```

Total REAL time to Xst completion: 9.00 secs
Total CPU time to Xst completion: 9.11 secs

```

```
-- >
```

Total memory usage is 4487500 kilobytes

Number of errors : 0 (0 filtered)

Number of warnings : 0 (0 filtered)

Number of infos : 0 (0 filtered)

```

64210457>fuse -incremental -o cla_add_n_bit_tb_isim_beh.exe -prj
cla_add_n_bit_tb.prj -top cla_add_n_bit_tb
Running: \unwrapped\fuse.exe -incremental -o cla_add_n_bit_tb_isim_beh.exe -prj
cla_add_n_bit_tb.prj -top cla_add_n_bit_tb
ISim P.20131013 ( signature 0x7708f090 )
Number of CPUs detected in this system: 8
Turning on mult-threading, number of parallel sub-compilation jobs: 16
Determining compilation order of HDL files
Parsing VHDL file "cla_gp.vhd" into library work
Parsing VHDL file "cla_add_n_bit.vhd" into library work
Parsing VHDL file "cla_add_n_bit_tb_IDEAL.vhd" into library work
Starting static elaboration
Completed static elaboration
Compiling package standard
Compiling package std_logic_1164
Compiling package textio
Compiling package std_logic_textio
Compiling package numeric_std
Compiling package attributes
Compiling package std_logic_misc
Compiling architecture ndv of entity cla_add_n_bit [\cla_add_n_bit( 8 )\]
Compiling architecture testbench_arch of entity cla_add_n_bit_tb
Time Resolution for simulation is 1ps.
Waiting for 1 sub-compilation( s ) to finish...
Compiled 10 VHDL Units
Built simulation executable cla_add_n_bit_tb_isim_beh.exe

```

Fuse Memory Usage: 37360 KB
Fuse CPU Usage: 921 ms

```
64210457>cla_add_n_bit_tb_isim_beh.exe -tclbatch isim.tcl -wdb
cla_add_n_bit_tb_isim_beh.wdb
ISim P.20131013 ( signature 0x7708f090 )
WARNING: A WEBPACK license was found.
WARNING: Please use Xilinx License Configuration Manager to check out a full ISim
license.
WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for
more information on the differences between the Lite and the Full version.
This is a Lite version of ISim.
Time resolution is 1 ps
Simulator is doing circuit initialization process.
Finished circuit initialization process.
```

```
64210457>rem ***** test cla flags
```

```
64210457>xst -ifn cla_add_n_bit_flags.xst
Release 14.7 - xst P.20131013 ( nt64 )
Copyright ( c ) 1995-2013 Xilinx, Inc. All rights reserved.
-- > Parameter TMPDIR set to xst/projnav.tmp
```

Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.24 secs

```
-- > Parameter xsthdpdir set to xst
```

Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.25 secs

```
-- > ERROR:Xst:438 - Can not open file : cla_add_n_bit_flags.prj
```

Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.28 secs

```
-- >
```

Total memory usage is 4422880 kilobytes

Number of errors : 1 (0 filtered)
Number of warnings : 0 (0 filtered)
Number of infos : 0 (0 filtered)

```
64210457>fuse -incremental -o cla_add_n_bit_tb_flags_isim_beh.exe -prj
cla_add_n_bit_flags_tb.prj -top cla_add_n_bit_flags_tb_IDEAL
Running: \unwrapped\fuse.exe -incremental -o cla_add_n_bit_tb_flags_isim_beh.exe -
prj cla_add_n_bit_flags_tb.prj -top cla_add_n_bit_flags_tb_IDEAL
ISim P.20131013 ( signature 0x7708f090 )
Number of CPUs detected in this system: 8
Turning on mult-threading, number of parallel sub-compilation jobs: 16
Determining compilation order of HDL files
Parsing VHDL file "cla_gp.vhd" into library work
Parsing VHDL file "cla_add_n_bit.vhd" into library work
Parsing VHDL file "cla_add_n_bit_flags_tb_IDEAL.vhd" into library work
Starting static elaboration
Completed static elaboration
Compiling package standard
Compiling package std_logic_1164
```

```

Compiling package textio
Compiling package std_logic_textio
Compiling package numeric_std
Compiling package attributes
Compiling package std_logic_misc
Compiling architecture ndv of entity cla_add_n_bit [\cla_add_n_bit( 8 )\]
Compiling architecture a1 of entity cla_add_n_bit_flags_tb_ideal
Time Resolution for simulation is 1ps.
Waiting for 1 sub-compilation( s ) to finish...
Compiled 10 VHDL Units
Built simulation executable cla_add_n_bit_tb_flags_isim_beh.exe
Fuse Memory Usage: 37568 KB
Fuse CPU Usage: 952 ms

64210457>cla_add_n_bit_tb_flags_isim_beh.exe -tclbatch isim.tcl -wdb
cla_add_n_bit_flags_tb.wdb
ISim P.20131013 ( signature 0x7708f090 )
WARNING: A WEBPACK license was found.
WARNING: Please use Xilinx License Configuration Manager to check out a full ISim
license.
WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for
more information on the differences between the Lite and the Full version.
This is a Lite version of ISim.
Time resolution is 1 ps
Simulator is doing circuit initialization process.
Finished circuit initialization process.

64210457>rem ***** test alu operations

64210457>xst -ifn alu_cla.xst
Release 14.7 - xst P.20131013 ( nt64 )
Copyright ( c ) 1995-2013 Xilinx, Inc. All rights reserved.
-- > Parameter TMPDIR set to xst/projnav.tmp

Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.24 secs

-- > Parameter xsthdpdir set to xst

Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.24 secs

-- >
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8.4.1 ) Clock Information

```


- 8.4.2) Asynchronous Control Signals Information
- 8.4.3) Timing Summary
- 8.4.4) Timing Details
- 8.4.5) Cross Clock Domains [Report](#)

```

=====
* Synthesis Options Summary *
=====
--      -- Source Parameters
Input File Name : "alu_cla.prj"
Ignore Synthesis Constraint File : NO

--      -- Target Parameters
Output File Name : "alu_cla"
Output Format : NGC
Target Device : xc6slx4-3-tqg144

--      -- Source Options
Top Module Name : alu_cla
Automatic FSM Extraction : YES
FSM Encoding Algorithm : Auto
Safe Implementation : No
FSM Style : LUT
RAM Extraction : Yes
RAM Style : Auto
ROM Extraction : Yes
Shift Register Extraction : YES
ROM Style : Auto
Resource Sharing : YES
Asynchronous To Synchronous : NO
Shift Register Minimum Size : 2
Use DSP Block : Auto
Automatic Register Balancing : No

--      -- Target Options
LUT Combining : Auto
Reduce Control Sets : Auto
Add IO Buffers : YES
Global Maximum Fanout : 100000
Add Generic Clock Buffer( BUFG ) : 16
Register Duplication : YES
Optimize Instantiated Primitives : NO
Use Clock Enable : Auto
Use Synchronous Set : Auto
Use Synchronous Reset : Auto
Pack IO Registers into IOBs : Auto
Equivalent register Removal : YES

--      -- General Options
Optimization Goal : Speed
Optimization Effort : 1
Power Reduction : NO
Keep Hierarchy : No
Netlist Hierarchy : As_Optimized
RTL Output : Yes
Global Optimization : AllClockNets
Read Cores : YES
Write Timing Constraints : NO
Cross Clock Analysis : NO

```

Hierarchy Separator : /
Bus Delimiter : <>
Case Specifier : Maintain
Slice Utilization Ratio : 100
BRAM Utilization Ratio : 100
DSP48 Utilization Ratio : 100
Auto BRAM Packing : NO
Slice Utilization Ratio Delta : 5

=====

=====

* HDL Parsing *

=====

Parsing VHDL file "64210457\cla_gp.vhd" into library work
Parsing entity <cla_gp>.
Parsing architecture <ideal> of entity <cla_gp>.
Parsing VHDL file "64210457\cla_add_n_bit.vhd" into library work
Parsing entity <cla_add_n_bit>.
Parsing architecture <NDV> of entity <cla_add_n_bit>.
Parsing VHDL file "64210457\alu_cla.vhd" into library work
Parsing entity <alu_cla>.
Parsing architecture <NDV> of entity <alu_cla>.

=====

* HDL Elaboration *

=====

Elaborating entity <alu_cla> (architecture <NDV>) with generics from library <work>.

Elaborating entity <cla_add_n_bit> (architecture <NDV>) with generics from library <work>.

=====

* HDL Synthesis *

=====

Synthesizing Unit <alu_cla>.
Related source file is "64210457\alu_cla.vhd".
n = 8
Found 8-bit 12-to-1 multiplexer for signal <S> created at line 75.
Summary:
inferred 19 Multiplexer(s).
Unit <alu_cla> synthesized.

Synthesizing Unit <cla_add_n_bit>.
Related source file is "64210457\cla_add_n_bit.vhd".
n = 8
Summary:
Unit <cla_add_n_bit> synthesized.

=====

HDL Synthesis Report

Macro Statistics

Multiplexers : 19
1-bit 2-to-1 multiplexer : 12
8-bit 12-to-1 multiplexer : 1

```
8-bit 2-to-1 multiplexer : 6
# Xors : 17
1-bit xor2 : 16
8-bit xor2 : 1
```

=====

=====

* Advanced HDL Synthesis *

=====

=====

Advanced HDL Synthesis Report

Macro Statistics

```
# Multiplexers : 19
1-bit 2-to-1 multiplexer : 12
8-bit 12-to-1 multiplexer : 1
8-bit 2-to-1 multiplexer : 6
# Xors : 17
1-bit xor2 : 16
8-bit xor2 : 1
```

=====

=====

* Low Level Synthesis *

=====

Optimizing unit <alu_cla> ...

Optimizing unit <cla_add_n_bit> ...

Mapping all equations...

Building and optimizing final netlist ...

Found area constraint ratio of 100 (+ 5) on block alu_cla, actual ratio is 3.

Final Macro Processing ...

=====

Final Register Report

Found no macro

=====

=====

* Partition Report *

=====

Partition Implementation Status

```
--      --      --      --      --      --      --      --      --      --      --      --
--      --      --      --      --      --      --      --      --      --      --      --
```

No Partitions were found in this design.

```
--      --      --      --      --      --      --      --      --      --      --      --
--      --      --      --      --      --      --      --      --      --      --      --
```

=====

* Design Summary *

=====

Top Level Output File Name : alu_cla.ngc

Primitive and Black Box Usage:

```
--      --      --      --      --      --      --      --      --      --      --      --
--      --      --
# BELS : 60
# LUT3 : 4
# LUT5 : 14
# LUT6 : 41
# MUXF7 : 1
# IO Buffers : 34
# IBUF : 20
# OBUF : 14
```

Device utilization summary:

```
--      --      --      --      --      --      --      --      --      --      --      --
-
```

Selected Device : 6slx4tqg144-3

Slice Logic Utilization:

Number of Slice LUTs: 59 out of 2400 2%
Number used as Logic: 59 out of 2400 2%

Slice Logic Distribution:

Number of LUT Flip Flop pairs used: 59
Number with an unused Flip Flop: 59 out of 59 100%
Number with an unused LUT: 0 out of 59 0%
Number of fully used LUT-FF pairs: 0 out of 59 0%
Number of unique control sets: 0

IO Utilization:

Number of IOs: 34
Number of bonded IOBs: 34 out of 102 33%

Specific Feature Utilization:

```
--      --      --      --      --      --      --      --      --      --      --      --
-
```

Partition Resource Summary:

```
--      --      --      --      --      --      --      --      --      --      --      --
-
```

No Partitions were found in this design.

```
--      --      --      --      --      --      --      --      --      --      --      --
-
```

=====

Timing Report

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.
FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT
GENERATED AFTER PLACE-and-ROUTE.

Clock Information:

```

--      --      --      --      --      --      --      --      --
No clock signals found in this design

Asynchronous Control Signals Information:
--      --      --      --      --      --      --      --      --
--      --      --      --      --      --      --      --      --
No asynchronous control signals found in this design

Timing Summary:
--      --      --      --      --      --      --      --
Speed Grade: -3

Minimum period: No path found
Minimum input arrival time before clock: No path found
Maximum output required time after clock: No path found
Maximum combinational path delay: 11.168ns

Timing Details:
--      --      --      --      --      --      --      --
All values displayed in nanoseconds ( ns )

=====
Timing constraint: Default path analysis
Total number of paths / destination ports: 1146 / 14
--      --      --      --      --      --      --      --      --
--      --      --      --      --      --      --      --      --
--      --      --      --      --      --      --      --      --
Delay: 11.168ns ( Levels of Logic = 8 )
Source: F<2> ( PAD )
Destination: Negative ( PAD )

Data Path: F<2> to Negative
Gate Net
Cell:in->out fanout Delay Delay Logical Name ( Net Name )
--      --      --      --      --      --      --      --      --
--      --      --      --      --      --      --      --      --
--      --      --      --      --      --      --      --      --
IBUF:I->O 35 1.222 1.679 F_2_IBUF ( F_2_IBUF )
LUT6:I1->O 6 0.203 0.973 Mmux_Y_sig31 ( Y_sig<1> )
LUT5:I2->O 4 0.205 1.028 U1/C<3>2 ( U1/C<3> )
LUT6:I1->O 1 0.203 0.000 U1/C<6>_G ( N16 )
MUXF7:I1->O 5 0.140 0.943 U1/C<6> ( U1/C<6> )
LUT5:I2->O 3 0.205 1.015 U1/Mxor_S_sig<7>_xo<0>1 ( S_sig<7> )
LUT6:I0->O 1 0.203 0.579 Mmux_Negative1 ( Negative_OBUF )
OBUF:I->O 2.571 Negative_OBUF ( Negative )
--      --      --      --      --      --      --      --      --
--      --      --      --      --      --      --      --      --
Total 11.168ns ( 4.952ns logic, 6.216ns route )
( 44.3% logic, 55.7% route )

=====

Cross Clock Domains Report:
--      --      --      --      --      --      --      --      --
--      --      --      --      --      --      --      --      --
=====

Total REAL time to Xst completion: 10.00 secs
Total CPU time to Xst completion: 9.70 secs

```

-- >

Total memory usage is 4487500 kilobytes

Number of errors : 0 (0 filtered)

Number of warnings : 0 (0 filtered)

Number of infos : 0 (0 filtered)

64210457>fuse -incremental -o alu_cla_tb_isim_beh.exe -prj alu_cla_tb.prj -top alu_cla_tb

Running: \unwrapped\fuse.exe -incremental -o alu_cla_tb_isim_beh.exe -prj alu_cla_tb.prj -top alu_cla_tb

ISim P.20131013 (signature 0x7708f090)

Number of CPUs detected in this system: 8

Turning on mult-threading, number of parallel sub-compilation jobs: 16

Determining compilation order of HDL files

Parsing VHDL file "cla_gp.vhd" into library work

Parsing VHDL file "cla_add_n_bit.vhd" into library work

Parsing VHDL file "alu_cla.vhd" into library work

Parsing VHDL file "alu_cla_tb_IDEAL.vhd" into library work

Starting static elaboration

Completed static elaboration

Compiling package standard

Compiling package std_logic_1164

Compiling package textio

Compiling package std_logic_textio

Compiling package numeric_std

Compiling package attributes

Compiling package std_logic_misc

Compiling architecture ndv of entity cla_add_n_bit [\cla_add_n_bit(8)\]

Compiling architecture ndv of entity alu_cla [\alu_cla(8)\]

Compiling architecture testbench_arch of entity alu_cla_tb

Time Resolution for simulation is 1ps.

Waiting for 1 sub-compilation(s) to finish...

Compiled 12 VHDL Units

Built simulation executable alu_cla_tb_isim_beh.exe

Fuse Memory Usage: 37768 KB

Fuse CPU Usage: 905 ms

64210457>alu_cla_tb_isim_beh.exe -tclbatch isim.tcl -wdb alu_cla_tb_isim_beh.wdb

ISim P.20131013 (signature 0x7708f090)

WARNING: A WEBPACK license was found.

WARNING: Please use Xilinx License Configuration Manager to check out a full ISim license.

WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for more information on the differences between the Lite and the Full version.

This is a Lite version of ISim.

Time resolution is 1 ps

Simulator is doing circuit initialization process.

Finished circuit initialization process.

at 7864320 ns, Instance /alu_cla_tb/ : Warning: NUMERIC_STD.TO_UNSIGNED: vector truncated

at 8847360 ns, Instance /alu_cla_tb/ : Warning: NUMERIC_STD.TO_UNSIGNED: vector truncated

at 9830400 ns, Instance /alu_cla_tb/ : Warning: NUMERIC_STD.TO_UNSIGNED: vector truncated

at 10813440 ns, Instance /alu_cla_tb/ : Warning: NUMERIC_STD.TO_UNSIGNED: vector truncated

at 11796480 ns, Instance /alu_cla_tb/ : Warning: NUMERIC_STD.TO_UNSIGNED: vector truncated
at 12779520 ns, Instance /alu_cla_tb/ : Warning: NUMERIC_STD.TO_UNSIGNED: vector truncated
at 13762560 ns, Instance /alu_cla_tb/ : Warning: NUMERIC_STD.TO_UNSIGNED: vector truncated
at 14745600 ns, Instance /alu_cla_tb/ : Warning: NUMERIC_STD.TO_UNSIGNED: vector truncated

64210457>rem ***** test alu flags

64210457>xst -ifn alu_cla_flags.xst
Release 14.7 - xst P.20131013 (nt64)
Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.
-- > Parameter TMPDIR set to xst/projnav.tmp

Total REAL time to Xst completion: 1.00 secs
Total CPU time to Xst completion: 0.33 secs

-- > Parameter xsthdmdir set to xst

Total REAL time to Xst completion: 1.00 secs
Total CPU time to Xst completion: 0.34 secs

-- >

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=====
* Synthesis Options Summary *

=====

-- -- Source Parameters

Input File Name : "alu_cla_flags_tb.prj"
Ignore Synthesis Constraint File : NO

-- -- Target Parameters

Output File Name : "alu_cla_flags_tb"
Output Format : NGC
Target Device : xc6slx4-3-tqg144

-- -- Source Options

Top Module Name : alu_cla_flags_tb
Automatic FSM Extraction : YES
FSM Encoding Algorithm : Auto
Safe Implementation : No
FSM Style : LUT
RAM Extraction : Yes
RAM Style : Auto
ROM Extraction : Yes
Shift Register Extraction : YES
ROM Style : Auto
Resource Sharing : YES
Asynchronous To Synchronous : NO
Shift Register Minimum Size : 2
Use DSP Block : Auto
Automatic Register Balancing : No

-- -- Target Options

LUT Combining : Auto
Reduce Control Sets : Auto
Add IO Buffers : YES
Global Maximum Fanout : 100000
Add Generic Clock Buffer(BUFG) : 16
Register Duplication : YES
Optimize Instantiated Primitives : NO
Use Clock Enable : Auto
Use Synchronous Set : Auto
Use Synchronous Reset : Auto
Pack IO Registers into IOBs : Auto
Equivalent register Removal : YES

-- -- General Options

Optimization Goal : Speed
Optimization Effort : 1
Power Reduction : NO
Keep Hierarchy : No
Netlist Hierarchy : As_Optimized
RTL Output : Yes
Global Optimization : AllClockNets
Read Cores : YES
Write Timing Constraints : NO
Cross Clock Analysis : NO
Hierarchy Separator : /
Bus Delimiter : <>
Case Specifier : Maintain
Slice Utilization Ratio : 100
BRAM Utilization Ratio : 100
DSP48 Utilization Ratio : 100
Auto BRAM Packing : NO
Slice Utilization Ratio Delta : 5

=====

=====

* HDL Parsing *

=====

Parsing VHDL file "64210457\cla_gp.vhd" into library work
Parsing entity <cla_gp>.
Parsing architecture <ideal> of entity <cla_gp>.
Parsing VHDL file "64210457\cla_add_n_bit.vhd" into library work


```

Parsing entity <cla_add_n_bit>.
Parsing architecture <NDV> of entity <cla_add_n_bit>.
Parsing VHDL file "64210457\alu_cla.vhd" into library work
Parsing entity <alu_cla>.
Parsing architecture <NDV> of entity <alu_cla>.
Parsing VHDL file "64210457\alu_cla_tb_FLAGS_IDEAL.vhd" into library work
Parsing entity <alu_cla_flags_tb>.
Parsing architecture <test_alu_flags> of entity <alu_cla_flags_tb>.

=====
* HDL Elaboration *
=====

Elaborating entity <alu_cla_flags_tb> ( architecture <test_alu_flags> ) with
generics from library <work>.

Elaborating entity <alu_cla> ( architecture <NDV> ) with generics from library
<work>.

Elaborating entity <cla_add_n_bit> ( architecture <NDV> ) with generics from
library <work>.
ERROR:HDLCompiler:890 - "64210457\alu_cla_tb_FLAGS_IDEAL.vhd" Line 144: wait
statement without UNTIL clause not supported for synthesis
Netlist alu_cla_flags_tb( 8 )( test_alu_flags ) remains a blackbox, due to errors
in its contents
-- >

Total memory usage is 4466680 kilobytes

Number of errors : 1 ( 0 filtered )
Number of warnings : 0 ( 0 filtered )
Number of infos : 0 ( 0 filtered )

64210457>fuse -incremental -o alu_cla_flags_tb_isim_beh.exe -prj
alu_cla_flags_tb.prj -top alu_cla_flags_tb
Running: \unwrapped\fuse.exe -incremental -o alu_cla_flags_tb_isim_beh.exe -prj
alu_cla_flags_tb.prj -top alu_cla_flags_tb
ISim P.20131013 ( signature 0x7708f090 )
Number of CPUs detected in this system: 8
Turning on mult-threading, number of parallel sub-compilation jobs: 16
Determining compilation order of HDL files
Parsing VHDL file "cla_gp.vhd" into library work
Parsing VHDL file "cla_add_n_bit.vhd" into library work
Parsing VHDL file "alu_cla.vhd" into library work
Parsing VHDL file "alu_cla_tb_FLAGS_IDEAL.vhd" into library work
Starting static elaboration
Completed static elaboration
Compiling package standard
Compiling package std_logic_1164
Compiling package textio
Compiling package std_logic_textio
Compiling package numeric_std
Compiling package attributes
Compiling package std_logic_misc
Compiling architecture ndv of entity cla_add_n_bit [\cla_add_n_bit( 8 )\]
Compiling architecture ndv of entity alu_cla [\alu_cla( 8 )\]
Compiling architecture test_alu_flags of entity alu_cla_flags_tb
Time Resolution for simulation is 1ps.
Waiting for 1 sub-compilation( s ) to finish...

```

Compiled 12 VHDL Units
Built simulation executable alu_cla_flags_tb_isim_beh.exe
Fuse Memory Usage: 37488 KB
Fuse CPU Usage: 999 ms

```
64210457>alu_cla_flags_tb_isim_beh.exe -tclbatch isim.tcl -wdb
alu_cla_flags_tb_isim_beh.wdb
ISim P.20131013 ( signature 0x7708f090 )
WARNING: A WEBPACK license was found.
WARNING: Please use Xilinx License Configuration Manager to check out a full ISim
license.
WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for
more information on the differences between the Lite and the Full version.
This is a Lite version of ISim.
Time resolution is 1 ps
Simulator is doing circuit initialization process.
Finished circuit initialization process.
```

```
-- *****
-- **** STUDENT: 64240429
-- *****
-- KOMENTARJI K OCENI NALOGE
-- Matej Možek: Ni pripomb
-- *****
```

```
64240429>rem ***** test cla adder
```

```
64240429>if not exist "xst" mkdir xst
```

```
64240429>cd XST
```

```
64240429\xst>if not exist "projnav.tmp" mkdir "projnav.tmp"
```

```
64240429\xst>cd ..
```

```
64240429>rem ***** test cla operations
```

```
64240429>xst -ifn cla_add_n_bit.xst
Release 14.7 - xst P.20131013 ( nt64 )
Copyright ( c ) 1995-2013 Xilinx, Inc. All rights reserved.
-- > Parameter TMPDIR set to xst/projnav.tmp
```

```
Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.24 secs
```

```
-- > Parameter xsthdpdir set to xst
```

```
Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.25 secs
```

```
-- >
```

```
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```
=====
* Synthesis Options Summary *
```

```
-- -- Source Parameters
```

```
Input File Name : "cla_add_n_bit.prj"
```

Ignore Synthesis Constraint File : NO

-- -- Target Parameters

Output File Name : "cla_add_n_bit"

Output Format : NGC

Target Device : xc6slx4-3-tqg144

-- -- Source Options

Top Module Name : cla_add_n_bit

Automatic FSM Extraction : YES

FSM Encoding Algorithm : Auto

Safe Implementation : No

FSM Style : LUT

RAM Extraction : Yes

RAM Style : Auto

ROM Extraction : Yes

Shift Register Extraction : YES

ROM Style : Auto

Resource Sharing : YES

Asynchronous To Synchronous : NO

Shift Register Minimum Size : 2

Use DSP Block : Auto

Automatic Register Balancing : No

-- -- Target Options

LUT Combining : Auto

Reduce Control Sets : Auto

Add IO Buffers : YES

Global Maximum Fanout : 100000

Add Generic Clock Buffer(BUFG) : 16

Register Duplication : YES

Optimize Instantiated Primitives : NO

Use Clock Enable : Auto

Use Synchronous Set : Auto

Use Synchronous Reset : Auto

Pack IO Registers into IOBs : Auto

Equivalent register Removal : YES

-- -- General Options

Optimization Goal : Speed

Optimization Effort : 1

Power Reduction : NO

Keep Hierarchy : No

Netlist Hierarchy : As_Optimized

RTL Output : Yes

Global Optimization : AllClockNets

Read Cores : YES

Write Timing Constraints : NO

Cross Clock Analysis : NO

Hierarchy Separator : /

Bus Delimiter : <>

Case Specifier : Maintain

Slice Utilization Ratio : 100

BRAM Utilization Ratio : 100

DSP48 Utilization Ratio : 100

Auto BRAM Packing : NO

Slice Utilization Ratio Delta : 5

=====

```

=====
* HDL Parsing *
=====
Parsing VHDL file "64240429\cla_gp.vhd" into library work
Parsing entity <cla_gp>.
Parsing architecture <ideal> of entity <cla_gp>.
Parsing VHDL file "64240429\cla_add_n_bit.vhd" into library work
Parsing entity <cla_add_n_bit>.
Parsing architecture <NDV> of entity <cla_add_n_bit>.

=====
* HDL Elaboration *
=====

Elaborating entity <cla_add_n_bit> ( architecture <NDV> ) with generics from
library <work>.

=====
* HDL Synthesis *
=====

Synthesizing Unit <cla_add_n_bit>.
Related source file is "64240429\cla_add_n_bit.vhd".
n = 8
Summary:
Unit <cla_add_n_bit> synthesized.

=====
HDL Synthesis Report

Macro Statistics
# Xors : 16
1-bit xor2 : 16

=====

=====
* Advanced HDL Synthesis *
=====

=====
Advanced HDL Synthesis Report

Macro Statistics
# Xors : 16
1-bit xor2 : 16

=====

=====
* Low Level Synthesis *
=====

Optimizing unit <cla_add_n_bit> ...

Mapping all equations...
Building and optimizing final netlist ...

```

Found area constraint ratio of 100 (+ 5) on block cla_add_n_bit, actual ratio is 1.

Final Macro Processing ...

=====
Final Register Report

Found no macro

=====
* Partition Report *
=====

Partition Implementation Status

-- -- -- -- -- -- -- -- -- -- -- -- -- --
-- -- -

No Partitions were found in this design.

-- -- -- -- -- -- -- -- -- -- -- -- -- --
-- -- -

=====
* Design Summary *
=====

Top Level Output File Name : cla_add_n_bit.ngc

Primitive and Black Box Usage:

-- -- -- -- -- -- -- -- -- -- -- -- -- --
-- --

BELS : 24
LUT2 : 6
LUT3 : 3
LUT5 : 6
LUT6 : 9
IO Buffers : 28
IBUF : 17
OBUF : 11

Device utilization summary:

-- -- -- -- -- -- -- -- -- -- -- -- -- --
-

Selected Device : 6slx4tqg144-3

Slice Logic Utilization:

Number of Slice LUTs: 24 out of 2400 1%
Number used as Logic: 24 out of 2400 1%

Slice Logic Distribution:

Number of LUT Flip Flop pairs used: 24
Number with an unused Flip Flop: 24 out of 24 100%
Number with an unused LUT: 0 out of 24 0%
Number of fully used LUT-FF pairs: 0 out of 24 0%
Number of unique control sets: 0

IO Utilization:

Number of IOs: 28

Number of bonded IOBs: 28 out of 102 27%

Specific Feature Utilization:

```
-- -- -- -- -- -- -- -- -- -- -- -- -- --  
-
```

Partition Resource Summary:

```
-- -- -- -- -- -- -- -- -- -- -- -- -- --  
-
```

No Partitions were found in this design.

```
-- -- -- -- -- -- -- -- -- -- -- -- -- --  
-
```

=====
Timing Report

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.

FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT
GENERATED AFTER PLACE-and-ROUTE.

Clock Information:

```
-- -- -- -- -- -- -- -- -- -- -- -- -- --  
No clock signals found in this design
```

Asynchronous Control Signals Information:

```
-- -- -- -- -- -- -- -- -- -- -- -- -- --  
-- -- -- -- -- -- -- -- -- -- -- -- -- --
```

No asynchronous control signals found in this design

Timing Summary:

```
-- -- -- -- -- -- -- -- -- -- -- -- -- --
```

Speed Grade: -3

Minimum period: No path found

Minimum input arrival time before clock: No path found

Maximum output required time after clock: No path found

Maximum combinational path delay: 9.101ns

Timing Details:

```
-- -- -- -- -- -- -- -- -- -- -- -- -- --
```

All values displayed in nanoseconds (ns)

=====
Timing constraint: Default path analysis

Total number of paths / destination ports: 131 / 11

```
-- -- -- -- -- -- -- -- -- -- -- -- -- --  
-- -- -- -- -- -- -- -- -- -- -- -- -- --  
-- -- -- -- -- -- -- -- -- -- -- -- -- --
```

Delay: 9.101ns (Levels of Logic = 7)

Source: Y<0> (PAD)

Destination: S<7> (PAD)

Data Path: Y<0> to S<7>

Gate Net

Cell:in->out fanout Delay Delay Logical Name (Net Name)

```

--      --      --      --      --      --      --      --      --      --      --
--      --      --      --      --      --      --      --      --      --      --
--      --
IBUF:I->0 6 1.222 0.973 Y_0_IBUF ( Y_0_IBUF )
LUT3:I0->0 2 0.205 0.617 C<3>_SW0 ( N2 )
LUT5:I4->0 3 0.205 0.651 C<3> ( C<3> )
LUT3:I2->0 2 0.205 0.617 C<6>_SW0 ( N4 )
LUT5:I4->0 2 0.205 0.845 C<6> ( C<6> )
LUT5:I2->0 1 0.205 0.579 Mxor_S_sig<7>_xo<0>1 ( S_7_OBUF )
OBUF:I->0 2.571 S_7_OBUF ( S<7> )
--      --      --      --      --      --      --      --      --      --      --
--      --      --      --      --      --      --      --      --      --      --
Total 9.101ns ( 4.818ns logic, 4.283ns route )
( 52.9% logic, 47.1% route )

```

Cross Clock Domains Report:

```

Total REAL time to Xst completion: 9.00 secs
Total CPU time to Xst completion: 9.31 secs

```

```
-- >
```

Total memory usage is 4487500 kilobytes

Number of errors : 0 (0 filtered)

Number of warnings : 0 (0 filtered)

Number of infos : 0 (0 filtered)

```

64240429>fuse -incremental -o cla_add_n_bit_tb_isim_beh.exe -prj
cla_add_n_bit_tb.prj -top cla_add_n_bit_tb
Running: \unwrapped\fuse.exe -incremental -o cla_add_n_bit_tb_isim_beh.exe -prj
cla_add_n_bit_tb.prj -top cla_add_n_bit_tb
ISim P.20131013 ( signature 0x7708f090 )
Number of CPUs detected in this system: 8
Turning on mult-threading, number of parallel sub-compilation jobs: 16
Determining compilation order of HDL files
Parsing VHDL file "cla_gp.vhd" into library work
Parsing VHDL file "cla_add_n_bit.vhd" into library work
Parsing VHDL file "cla_add_n_bit_tb_IDEAL.vhd" into library work
Starting static elaboration
Completed static elaboration
Compiling package standard
Compiling package std_logic_1164
Compiling package textio
Compiling package std_logic_textio
Compiling package numeric_std
Compiling package attributes
Compiling package std_logic_misc
Compiling architecture ndv of entity cla_add_n_bit [\cla_add_n_bit( 8 )\]
Compiling architecture testbench_arch of entity cla_add_n_bit_tb
Time Resolution for simulation is 1ps.
Waiting for 1 sub-compilation( s ) to finish...
Compiled 10 VHDL Units
Built simulation executable cla_add_n_bit_tb_isim_beh.exe

```


Fuse Memory Usage: 37420 KB
Fuse CPU Usage: 921 ms

```
64240429>cla_add_n_bit_tb_isim_beh.exe -tclbatch isim.tcl -wdb
cla_add_n_bit_tb_isim_beh.wdb
ISim P.20131013 ( signature 0x7708f090 )
WARNING: A WEBPACK license was found.
WARNING: Please use Xilinx License Configuration Manager to check out a full ISim
license.
WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for
more information on the differences between the Lite and the Full version.
This is a Lite version of ISim.
Time resolution is 1 ps
Simulator is doing circuit initialization process.
Finished circuit initialization process.
```

```
64240429>rem ***** test cla flags
```

```
64240429>xst -ifn cla_add_n_bit_flags.xst
Release 14.7 - xst P.20131013 ( nt64 )
Copyright ( c ) 1995-2013 Xilinx, Inc. All rights reserved.
-- > Parameter TMPDIR set to xst/projnav.tmp
```

Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.31 secs

```
-- > Parameter xsthdpdir set to xst
```

Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.31 secs

```
-- > ERROR:Xst:438 - Can not open file : cla_add_n_bit_flags.prj
```

Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.35 secs

```
-- >
```

Total memory usage is 4422880 kilobytes

Number of errors : 1 (0 filtered)
Number of warnings : 0 (0 filtered)
Number of infos : 0 (0 filtered)

```
64240429>fuse -incremental -o cla_add_n_bit_tb_flags_isim_beh.exe -prj
cla_add_n_bit_flags_tb.prj -top cla_add_n_bit_flags_tb_IDEAL
Running: \unwrapped\fuse.exe -incremental -o cla_add_n_bit_tb_flags_isim_beh.exe -
prj cla_add_n_bit_flags_tb.prj -top cla_add_n_bit_flags_tb_IDEAL
ISim P.20131013 ( signature 0x7708f090 )
Number of CPUs detected in this system: 8
Turning on mult-threading, number of parallel sub-compilation jobs: 16
Determining compilation order of HDL files
Parsing VHDL file "cla_gp.vhd" into library work
Parsing VHDL file "cla_add_n_bit.vhd" into library work
Parsing VHDL file "cla_add_n_bit_flags_tb_IDEAL.vhd" into library work
Starting static elaboration
Completed static elaboration
Compiling package standard
Compiling package std_logic_1164
```

```

Compiling package textio
Compiling package std_logic_textio
Compiling package numeric_std
Compiling package attributes
Compiling package std_logic_misc
Compiling architecture ndv of entity cla_add_n_bit [\cla_add_n_bit( 8 )\]
Compiling architecture a1 of entity cla_add_n_bit_flags_tb_ideal
Time Resolution for simulation is 1ps.
Waiting for 1 sub-compilation( s ) to finish...
Compiled 10 VHDL Units
Built simulation executable cla_add_n_bit_tb_flags_isim_beh.exe
Fuse Memory Usage: 37464 KB
Fuse CPU Usage: 968 ms

64240429>cla_add_n_bit_tb_flags_isim_beh.exe -tclbatch isim.tcl -wdb
cla_add_n_bit_flags_tb.wdb
ISim P.20131013 ( signature 0x7708f090 )
WARNING: A WEBPACK license was found.
WARNING: Please use Xilinx License Configuration Manager to check out a full ISim
license.
WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for
more information on the differences between the Lite and the Full version.
This is a Lite version of ISim.
Time resolution is 1 ps
Simulator is doing circuit initialization process.
Finished circuit initialization process.

64240429>rem ***** test alu operations

64240429>xst -ifn alu_cla.xst
Release 14.7 - xst P.20131013 ( nt64 )
Copyright ( c ) 1995-2013 Xilinx, Inc. All rights reserved.
-- > Parameter TMPDIR set to xst/projnav.tmp

Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.24 secs

-- > Parameter xsthdmdir set to xst

Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.24 secs

-- >
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```

- 8.4.2) Asynchronous Control Signals Information
- 8.4.3) Timing Summary
- 8.4.4) Timing Details
- 8.4.5) Cross Clock Domains [Report](#)

```

=====
* Synthesis Options Summary *
=====
--      -- Source Parameters
Input File Name : "alu_cla.prj"
Ignore Synthesis Constraint File : NO

--      -- Target Parameters
Output File Name : "alu_cla"
Output Format : NGC
Target Device : xc6slx4-3-tqg144

--      -- Source Options
Top Module Name : alu_cla
Automatic FSM Extraction : YES
FSM Encoding Algorithm : Auto
Safe Implementation : No
FSM Style : LUT
RAM Extraction : Yes
RAM Style : Auto
ROM Extraction : Yes
Shift Register Extraction : YES
ROM Style : Auto
Resource Sharing : YES
Asynchronous To Synchronous : NO
Shift Register Minimum Size : 2
Use DSP Block : Auto
Automatic Register Balancing : No

--      -- Target Options
LUT Combining : Auto
Reduce Control Sets : Auto
Add IO Buffers : YES
Global Maximum Fanout : 100000
Add Generic Clock Buffer( BUFG ) : 16
Register Duplication : YES
Optimize Instantiated Primitives : NO
Use Clock Enable : Auto
Use Synchronous Set : Auto
Use Synchronous Reset : Auto
Pack IO Registers into IOBs : Auto
Equivalent register Removal : YES

--      -- General Options
Optimization Goal : Speed
Optimization Effort : 1
Power Reduction : NO
Keep Hierarchy : No
Netlist Hierarchy : As_Optimized
RTL Output : Yes
Global Optimization : AllClockNets
Read Cores : YES
Write Timing Constraints : NO
Cross Clock Analysis : NO

```

Hierarchy Separator : /
Bus Delimiter : <>
Case Specifier : Maintain
Slice Utilization Ratio : 100
BRAM Utilization Ratio : 100
DSP48 Utilization Ratio : 100
Auto BRAM Packing : NO
Slice Utilization Ratio Delta : 5

=====

=====

* HDL Parsing *

=====

Parsing VHDL file "64240429\cla_gp.vhd" into library work
Parsing entity <cla_gp>.
Parsing architecture <ideal> of entity <cla_gp>.
Parsing VHDL file "64240429\cla_add_n_bit.vhd" into library work
Parsing entity <cla_add_n_bit>.
Parsing architecture <NDV> of entity <cla_add_n_bit>.
Parsing VHDL file "64240429\alu_cla.vhd" into library work
Parsing entity <alu_cla>.
Parsing architecture <NDV> of entity <alu_cla>.

=====

* HDL Elaboration *

=====

Elaborating entity <alu_cla> (architecture <NDV>) with generics from library <work>.

Elaborating entity <cla_add_n_bit> (architecture <NDV>) with generics from library <work>.

=====

* HDL Synthesis *

=====

Synthesizing Unit <alu_cla>.

Related source file is "64240429\alu_cla.vhd".

n = 8

Found 8-bit 12-to-1 multiplexer for signal <S> created at line 64.

Summary:

inferred 7 Multiplexer(s).

Unit <alu_cla> synthesized.

Synthesizing Unit <cla_add_n_bit>.

Related source file is "64240429\cla_add_n_bit.vhd".

n = 8

Summary:

Unit <cla_add_n_bit> synthesized.

=====

HDL Synthesis Report

Macro Statistics

Multiplexers : 7

8-bit 12-to-1 multiplexer : 1

8-bit 2-to-1 multiplexer : 6

```
# Xors : 17
1-bit xor2 : 16
8-bit xor2 : 1
```

=====

=====

```
* Advanced HDL Synthesis *
```

=====

=====

Advanced HDL Synthesis Report

Macro Statistics

```
# Multiplexers : 7
8-bit 12-to-1 multiplexer : 1
8-bit 2-to-1 multiplexer : 6
# Xors : 17
1-bit xor2 : 16
8-bit xor2 : 1
```

=====

=====

```
* Low Level Synthesis *
```

=====

Optimizing unit <alu_cla> ...

Optimizing unit <cla_add_n_bit> ...

Mapping all equations...

Building and optimizing final netlist ...

Found area constraint ratio of 100 (+ 5) on block alu_cla, actual ratio is 3.

Final Macro Processing ...

=====

Final Register Report

Found no macro

=====

=====

```
* Partition Report *
```

=====

Partition Implementation Status

```
--      --      --      --      --      --      --      --      --      --      --      --
--      --      --
```

No Partitions were found in this design.

```
--      --      --      --      --      --      --      --      --      --      --      --
--      --      --
```

=====

```
* Design Summary *
```

=====

Primitive and Black Box Usage:

-- -- -- -- -- -- -- -- -- -- -- -- -- --
 -- -- -- -- -- -- -- -- -- -- -- -- -- --

```
# BELS : 52
# LUT3 : 2
# LUT5 : 7
# LUT6 : 42
# MUXF7 : 1
# IO Buffers : 34
# IBUF : 20
# OBUF : 14
```

Device utilization summary:

1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53 54 55 56 57 58 59 60 61 62 63 64 65 66 67 68 69 70 71 72 73 74 75 76 77 78 79 80 81 82 83 84 85 86 87 88 89 90 91 92 93 94 95 96 97 98 99 100

Selected Device : 6s1x4tqg144-3

Slice Logic Utilization:

Number of Slice LUTs: 51 out of 2400 2%
Number used as Logic: 51 out of 2400 2%

Slice Logic Distribution:

```

Number of LUT Flip Flop pairs used: 51
Number with an unused Flip Flop: 51 out of 51 100%
Number with an unused LUT: 0 out of 51 0%
Number of fully used LUT-FF pairs: 0 out of 51 0%
Number of unique control sets: 0

```

IO Utilization:

Number of IOs: 34
Number of bonded IOBs: 34 out of 102 33%

Specific Feature Utilization:

Partition Resource Summary:

1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53 54 55 56 57 58 59 60 61 62 63 64 65 66 67 68 69 70 71 72 73 74 75 76 77 78 79 80 81 82 83 84 85 86 87 88 89 90 91 92 93 94 95 96 97 98 99 100

No Partitions were found in this design.

.....

.....

Timing Report

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.
FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT
GENERATED AFTER PLACE-and-ROUTE.

Clock Information:

[illegible]

Asynchronous Control Signals Information:

```
-- -- -- -- -- -- -- -- -- -- -- -- -- --
-- -- -- -- -- -- -- -- -- -- -- -- -- --
```

No asynchronous control signals found in this design

Timing Summary:

```
-- -- -- -- -- -- -- -- -- -- -- -- -- --
```

Speed Grade: -3

Minimum period: No path found

Minimum input arrival time before clock: No path found

Maximum output required time after clock: No path found

Maximum combinational path delay: 11.074ns

Timing Details:

```
-- -- -- -- -- -- -- -- -- -- -- -- -- --
```

All values displayed in nanoseconds (ns)

=====
Timing constraint: Default path analysis

Total number of paths / destination ports: 1126 / 14

```
-- -- -- -- -- -- -- -- -- -- -- -- -- --
-- -- -- -- -- -- -- -- -- -- -- -- -- --
-- -- -- -- -- -- -- -- -- -- -- -- -- --
```

Delay: 11.074ns (Levels of Logic = 8)

Source: F<2> (PAD)

Destination: S<7> (PAD)

Data Path: F<2> to S<7>

Gate Net

Cell:in->out fanout Delay Delay Logical Name (Net Name)

```
-- -- -- -- -- -- -- -- -- -- -- -- -- --
-- -- -- -- -- -- -- -- -- -- -- -- -- --
-- -- -- -- -- -- -- -- -- -- -- -- -- --
```

IBUF:I->0 32 1.222 1.636 F_2_IBUF (F_2_IBUF)

LUT6:I1->0 6 0.203 0.973 Mmux_Y_sig31 (Y_sig<1>)

LUT5:I2->0 4 0.205 1.028 U1/C<3>2 (U1/C<3>)

LUT6:I1->0 1 0.203 0.000 U1/C<6>_G (N14)

MUXF7:I1->0 4 0.140 0.912 U1/C<6> (U1/C<6>)

LUT5:I2->0 3 0.205 0.995 U1/Mxor_S_sig<7>_xo<0>1 (Negative_OBUF)

LUT6:I1->0 1 0.203 0.579 Zero (Zero_OBUF)

OBUF:I->0 2.571 Zero_OBUF (Zero)

```
-- -- -- -- -- -- -- -- -- -- -- -- -- --
-- -- -- -- -- -- -- -- -- -- -- -- -- --
```

Total 11.074ns (4.952ns logic, 6.122ns route)

(44.7% logic, 55.3% route)

=====
Cross Clock Domains Report:

```
-- -- -- -- -- -- -- -- -- -- -- -- -- --
```

=====
Total REAL time to Xst completion: 9.00 secs

Total CPU time to Xst completion: 9.65 secs

-- >

Total memory usage is 4487500 kilobytes

Number of errors : 0 (0 filtered)

Number of warnings : 0 (0 filtered)

Number of infos : 0 (0 filtered)

64240429>fuse -incremental -o alu_cla_tb_isim_beh.exe -prj alu_cla_tb.prj -top alu_cla_tb

Running: \unwrapped\fuse.exe -incremental -o alu_cla_tb_isim_beh.exe -prj alu_cla_tb.prj -top alu_cla_tb

ISim P.20131013 (signature 0x7708f090)

Number of CPUs detected in this system: 8

Turning on mult-threading, number of parallel sub-compilation jobs: 16

Determining compilation order of HDL files

Parsing VHDL file "cla_gp.vhd" into library work

Parsing VHDL file "cla_add_n_bit.vhd" into library work

Parsing VHDL file "alu_cla.vhd" into library work

Parsing VHDL file "alu_cla_tb_IDEAL.vhd" into library work

Starting static elaboration

Completed static elaboration

Compiling package standard

Compiling package std_logic_1164

Compiling package textio

Compiling package std_logic_textio

Compiling package numeric_std

Compiling package attributes

Compiling package std_logic_misc

Compiling architecture ndv of entity cla_add_n_bit [\cla_add_n_bit(8)\]

Compiling architecture ndv of entity alu_cla [\alu_cla(8)\]

Compiling architecture testbench_arch of entity alu_cla_tb

Time Resolution for simulation is 1ps.

Waiting for 1 sub-compilation(s) to finish...

Compiled 12 VHDL Units

Built simulation executable alu_cla_tb_isim_beh.exe

Fuse Memory Usage: 37640 KB

Fuse CPU Usage: 968 ms

64240429>alu_cla_tb_isim_beh.exe -tclbatch isim.tcl -wdb alu_cla_tb_isim_beh.wdb

ISim P.20131013 (signature 0x7708f090)

WARNING: A WEBPACK license was found.

WARNING: Please use Xilinx License Configuration Manager to check out a full ISim license.

WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for more information on the differences between the Lite and the Full version.

This is a Lite version of ISim.

Time resolution is 1 ps

Simulator is doing circuit initialization process.

Finished circuit initialization process.

at 7864320 ns, Instance /alu_cla_tb/ : Warning: NUMERIC_STD.TO_UNSIGNED: vector truncated

at 8847360 ns, Instance /alu_cla_tb/ : Warning: NUMERIC_STD.TO_UNSIGNED: vector truncated

at 9830400 ns, Instance /alu_cla_tb/ : Warning: NUMERIC_STD.TO_UNSIGNED: vector truncated

at 10813440 ns, Instance /alu_cla_tb/ : Warning: NUMERIC_STD.TO_UNSIGNED: vector truncated

at 11796480 ns, Instance /alu_cla_tb/ : Warning: NUMERIC_STD.TO_UNSIGNED: vector truncated

at 12779520 ns, Instance /alu_cla_tb/ : Warning: NUMERIC_STD.TO_UNSIGNED: vector truncated
at 13762560 ns, Instance /alu_cla_tb/ : Warning: NUMERIC_STD.TO_UNSIGNED: vector truncated
at 14745600 ns, Instance /alu_cla_tb/ : Warning: NUMERIC_STD.TO_UNSIGNED: vector truncated

64240429>rem ***** test alu flags

64240429>xst -ifn alu_cla_flags.xst
Release 14.7 - xst P.20131013 (nt64)
Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.
-- > Parameter TMPDIR set to xst/projnav.tmp

Total REAL time to Xst completion: 1.00 secs
Total CPU time to Xst completion: 0.23 secs

-- > Parameter xsthdpdir set to xst

Total REAL time to Xst completion: 1.00 secs
Total CPU time to Xst completion: 0.23 secs

-- >

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 - 8.4.5) Cross Clock Domains Report

=====
* Synthesis Options Summary *

-- -- Source Parameters

Input File Name : "alu_cla_flags_tb.prj"
Ignore Synthesis Constraint File : NO

-- -- Target Parameters

Output File Name : "alu_cla_flags_tb"
Output Format : NGC
Target Device : xc6slx4-3-tqg144

-- -- Source Options

Top Module Name : alu_cla_flags_tb
Automatic FSM Extraction : YES

FSM Encoding Algorithm : Auto
Safe Implementation : No
FSM Style : LUT
RAM Extraction : Yes
RAM Style : Auto
ROM Extraction : Yes
Shift Register Extraction : YES
ROM Style : Auto
Resource Sharing : YES
Asynchronous To Synchronous : NO
Shift Register Minimum Size : 2
Use DSP Block : Auto
Automatic Register Balancing : No

-- -- Target Options

LUT Combining : Auto
Reduce Control Sets : Auto
Add IO Buffers : YES
Global Maximum Fanout : 100000
Add Generic Clock Buffer(BUFG) : 16
Register Duplication : YES
Optimize Instantiated Primitives : NO
Use Clock Enable : Auto
Use Synchronous Set : Auto
Use Synchronous Reset : Auto
Pack IO Registers into IOBs : Auto
Equivalent register Removal : YES

-- -- General Options

Optimization Goal : Speed
Optimization Effort : 1
Power Reduction : NO
Keep Hierarchy : No
Netlist Hierarchy : As_Optimized
RTL Output : Yes
Global Optimization : AllClockNets
Read Cores : YES
Write Timing Constraints : NO
Cross Clock Analysis : NO
Hierarchy Separator : /
Bus Delimiter : <>
Case Specifier : Maintain
Slice Utilization Ratio : 100
BRAM Utilization Ratio : 100
DSP48 Utilization Ratio : 100
Auto BRAM Packing : NO
Slice Utilization Ratio Delta : 5

=====

=====

* HDL Parsing *

=====

Parsing VHDL file "64240429\cla_gp.vhd" into library work
Parsing entity <cla_gp>.
Parsing architecture <ideal> of entity <cla_gp>.
Parsing VHDL file "64240429\cla_add_n_bit.vhd" into library work
Parsing entity <cla_add_n_bit>.
Parsing architecture <NDV> of entity <cla_add_n_bit>.

```

Parsing VHDL file "64240429\alu_cla.vhd" into library work
Parsing entity <alu_cla>.
Parsing architecture <NDV> of entity <alu_cla>.
Parsing VHDL file "64240429\alu_cla_tb_FLAGS_IDEAL.vhd" into library work
Parsing entity <alu_cla_flags_tb>.
Parsing architecture <test_alu_flags> of entity <alu_cla_flags_tb>.

=====
* HDL Elaboration *
=====

Elaborating entity <alu_cla_flags_tb> ( architecture <test_alu_flags> ) with
generics from library <work>.

Elaborating entity <alu_cla> ( architecture <NDV> ) with generics from library
<work>.

Elaborating entity <cla_add_n_bit> ( architecture <NDV> ) with generics from
library <work>.
ERROR:HDLCompiler:890 - "64240429\alu_cla_tb_FLAGS_IDEAL.vhd" Line 144: wait
statement without UNTIL clause not supported for synthesis
Netlist alu_cla_flags_tb( 8 )( test_alu_flags ) remains a blackbox, due to errors
in its contents
-- >

Total memory usage is 4466680 kilobytes

Number of errors : 1 ( 0 filtered )
Number of warnings : 0 ( 0 filtered )
Number of infos : 0 ( 0 filtered )

64240429>fuse -incremental -o alu_cla_flags_tb_isim_beh.exe -prj
alu_cla_flags_tb.prj -top alu_cla_flags_tb
Running: \unwrapped\fuse.exe -incremental -o alu_cla_flags_tb_isim_beh.exe -prj
alu_cla_flags_tb.prj -top alu_cla_flags_tb
ISim P.20131013 ( signature 0x7708f090 )
Number of CPUs detected in this system: 8
Turning on mult-threading, number of parallel sub-compilation jobs: 16
Determining compilation order of HDL files
Parsing VHDL file "cla_gp.vhd" into library work
Parsing VHDL file "cla_add_n_bit.vhd" into library work
Parsing VHDL file "alu_cla.vhd" into library work
Parsing VHDL file "alu_cla_tb_FLAGS_IDEAL.vhd" into library work
Starting static elaboration
Completed static elaboration
Compiling package standard
Compiling package std_logic_1164
Compiling package textio
Compiling package std_logic_textio
Compiling package numeric_std
Compiling package attributes
Compiling package std_logic_misc
Compiling architecture ndv of entity cla_add_n_bit [\cla_add_n_bit( 8 )\]
Compiling architecture ndv of entity alu_cla [\alu_cla( 8 )\]
Compiling architecture test_alu_flags of entity alu_cla_flags_tb
Time Resolution for simulation is 1ps.
Compiled 12 VHDL Units
Built simulation executable alu_cla_flags_tb_isim_beh.exe
Fuse Memory Usage: 37464 KB

```

Fuse CPU Usage: 967 ms

```
64240429>alu_cla_flags_tb_isim_beh.exe -tclbatch isim.tcl -wdb
```

```
alu_cla_flags_tb_isim_beh.wdb
```

```
ISim P.20131013 ( signature 0x7708f090 )
```

```
WARNING: A WEBPACK license was found.
```

```
WARNING: Please use Xilinx License Configuration Manager to check out a full ISim license.
```

```
WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for more information on the differences between the Lite and the Full version.
```

```
This is a Lite version of ISim.
```

```
Time resolution is 1 ps
```

```
Simulator is doing circuit initialization process.
```

```
Finished circuit initialization process.
```

```
-- *****
-- **** STUDENT: 64240430
-- *****
-- KOMENTARJI K OCENI NALOGE
-- Matej Možek: Ni pripomb
-- *****
```

```
64240430>rem ***** test cla adder
```

```
64240430>if not exist "xst" mkdir xst
```

```
64240430>cd XST
```

```
64240430\xst>if not exist "projnav.tmp" mkdir "projnav.tmp"
```

```
64240430\xst>cd ..
```

```
64240430>rem ***** test cla operations
```

```
64240430>xst -ifn cla_add_n_bit.xst
Release 14.7 - xst P.20131013 ( nt64 )
Copyright ( c ) 1995-2013 Xilinx, Inc. All rights reserved.
-- > Parameter TMPDIR set to xst/projnav.tmp
```

```
Total REAL time to Xst completion: 1.00 secs
Total CPU time to Xst completion: 0.30 secs
```

```
-- > Parameter xsthdpdir set to xst
```

```
Total REAL time to Xst completion: 1.00 secs
Total CPU time to Xst completion: 0.30 secs
```

```
-- >
```

```
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 - 8.4.3) Timing Summary
 - 8.4.4) Timing Details
 - 8.4.5) Cross Clock Domains Report

```
=====
* Synthesis Options Summary *
```

```
-- -- Source Parameters
```

```
Input File Name : "cla_add_n_bit.prj"
```

Ignore Synthesis Constraint File : NO

-- -- Target Parameters

Output File Name : "cla_add_n_bit"

Output Format : NGC

Target Device : xc6slx4-3-tqg144

-- -- Source Options

Top Module Name : cla_add_n_bit

Automatic FSM Extraction : YES

FSM Encoding Algorithm : Auto

Safe Implementation : No

FSM Style : LUT

RAM Extraction : Yes

RAM Style : Auto

ROM Extraction : Yes

Shift Register Extraction : YES

ROM Style : Auto

Resource Sharing : YES

Asynchronous To Synchronous : NO

Shift Register Minimum Size : 2

Use DSP Block : Auto

Automatic Register Balancing : No

-- -- Target Options

LUT Combining : Auto

Reduce Control Sets : Auto

Add IO Buffers : YES

Global Maximum Fanout : 100000

Add Generic Clock Buffer(BUFG) : 16

Register Duplication : YES

Optimize Instantiated Primitives : NO

Use Clock Enable : Auto

Use Synchronous Set : Auto

Use Synchronous Reset : Auto

Pack IO Registers into IOBs : Auto

Equivalent register Removal : YES

-- -- General Options

Optimization Goal : Speed

Optimization Effort : 1

Power Reduction : NO

Keep Hierarchy : No

Netlist Hierarchy : As_Optimized

RTL Output : Yes

Global Optimization : AllClockNets

Read Cores : YES

Write Timing Constraints : NO

Cross Clock Analysis : NO

Hierarchy Separator : /

Bus Delimiter : <>

Case Specifier : Maintain

Slice Utilization Ratio : 100

BRAM Utilization Ratio : 100

DSP48 Utilization Ratio : 100

Auto BRAM Packing : NO

Slice Utilization Ratio Delta : 5

=====

```

=====
* HDL Parsing *
=====
Parsing VHDL file "64240430\cla_gp.vhd" into library work
Parsing entity <cla_gp>.
Parsing architecture <ideal> of entity <cla_gp>.
Parsing VHDL file "64240430\cla_add_n_bit.vhd" into library work
Parsing entity <cla_add_n_bit>.
Parsing architecture <NDV> of entity <cla_add_n_bit>.

=====
* HDL Elaboration *
=====

Elaborating entity <cla_add_n_bit> ( architecture <NDV> ) with generics from
library <work>.

=====
* HDL Synthesis *
=====

Synthesizing Unit <cla_add_n_bit>.
Related source file is "64240430\cla_add_n_bit.vhd".
  n = 8
  Summary:
Unit <cla_add_n_bit> synthesized.

=====
HDL Synthesis Report

Macro Statistics
# Xors : 16
  1-bit xor2 : 16

=====

=====
* Advanced HDL Synthesis *
=====

=====
Advanced HDL Synthesis Report

Macro Statistics
# Xors : 16
  1-bit xor2 : 16

=====

=====
* Low Level Synthesis *
=====

Optimizing unit <cla_add_n_bit> ...

Mapping all equations...
Building and optimizing final netlist ...

```

Found area constraint ratio of 100 (+ 5) on block cla_add_n_bit, actual ratio is 1.

Final Macro Processing ...

=====
Final Register Report

Found no macro

=====
* Partition Report *
=====

Partition Implementation Status

-- -- -- -- -- -- -- -- -- -- -- -- -- --
-- -- -

No Partitions were found in this design.

-- -- -- -- -- -- -- -- -- -- -- -- -- --
-- -- -

=====
* Design Summary *
=====

Top Level Output File Name : cla_add_n_bit.ngc

Primitive and Black Box Usage:

-- -- -- -- -- -- -- -- -- -- -- -- -- --
-- -- -

BELS : 24
LUT2 : 6
LUT3 : 3
LUT5 : 6
LUT6 : 9
IO Buffers : 28
IBUF : 17
OBUF : 11

Device utilization summary:

-- -- -- -- -- -- -- -- -- -- -- -- -- --
-

Selected Device : 6slx4tqg144-3

Slice Logic Utilization:

Number of Slice LUTs: 24 out of 2400 1%
Number used as Logic: 24 out of 2400 1%

Slice Logic Distribution:

Number of LUT Flip Flop pairs used: 24
Number with an unused Flip Flop: 24 out of 24 100%
Number with an unused LUT: 0 out of 24 0%
Number of fully used LUT-FF pairs: 0 out of 24 0%
Number of unique control sets: 0

IO Utilization:

Number of IOs: 28

Number of bonded IOBs: 28 out of 102 27%

Specific Feature Utilization:

```
-- -- -- -- -- -- -- -- -- -- -- -- -- --
-
```

Partition Resource Summary:

```
-- -- -- -- -- -- -- -- -- -- -- -- -- --
-
```

No Partitions were found in this design.

```
-- -- -- -- -- -- -- -- -- -- -- -- -- --
-
```

=====
Timing Report

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.

FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT
GENERATED AFTER PLACE-and-ROUTE.

Clock Information:

```
-- -- -- -- -- -- -- -- -- -- -- -- -- --
```

No clock signals found in this design

Asynchronous Control Signals Information:

```
-- -- -- -- -- -- -- -- -- -- -- -- -- --
-- -- -- -- -- -- -- -- -- -- -- -- -- --
```

No asynchronous control signals found in this design

Timing Summary:

```
-- -- -- -- -- -- -- -- -- -- -- -- -- --
```

Speed Grade: -3

Minimum period: No path found

Minimum input arrival time before clock: No path found

Maximum output required time after clock: No path found

Maximum combinational path delay: 9.101ns

Timing Details:

```
-- -- -- -- -- -- -- -- -- -- -- -- -- --
```

All values displayed in nanoseconds (ns)

=====
Timing constraint: Default path analysis

Total number of paths / destination ports: 131 / 11

```
-- -- -- -- -- -- -- -- -- -- -- -- -- --
-- -- -- -- -- -- -- -- -- -- -- -- -- --
-- -- -- -- -- -- -- -- -- -- -- -- -- --
```

Delay: 9.101ns (Levels of Logic = 7)

Source: Y<0> (PAD)

Destination: S<7> (PAD)

Data Path: Y<0> to S<7>

Gate Net

Cell:in->out fanout Delay Delay Logical Name (Net Name)

```

--      --      --      --      --      --      --      --      --      --      --
--      --      --      --      --      --      --      --      --      --      --
--      --
IBUF:I->0 6 1.222 0.973 Y_0_IBUF ( Y_0_IBUF )
LUT3:I0->0 2 0.205 0.617 Carry<3>_SW0 ( N2 )
LUT5:I4->0 3 0.205 0.651 Carry<3> ( Carry<3> )
LUT3:I2->0 2 0.205 0.617 Carry<6>_SW0 ( N4 )
LUT5:I4->0 2 0.205 0.845 Carry<6> ( Carry<6> )
LUT5:I2->0 1 0.205 0.579 Mxor_vsota<7>_xo<0>1 ( S_7_OBUF )
OBUF:I->0 2.571 S_7_OBUF ( S<7> )
--      --      --      --      --      --      --      --      --      --      --
--      --      --      --      --      --      --      --      --      --      --
Total 9.101ns ( 4.818ns logic, 4.283ns route )
( 52.9% logic, 47.1% route )

```

===== Cross Clock Domains Report:

```

--      --      --      --      --      --      --      --      --      --      --
--      --      --      --      --      --      --      --      --      --      --
=====
Total REAL time to Xst completion: 10.00 secs
Total CPU time to Xst completion: 9.68 secs

```

-- >

Total memory usage is 4487500 kilobytes

Number of errors : 0 (0 filtered)

Number of warnings : 0 (0 filtered)

Number of infos : 0 (0 filtered)

```

64240430>fuse -incremental -o cla_add_n_bit_tb_isim_beh.exe -prj
cla_add_n_bit_tb.prj -top cla_add_n_bit_tb
Running: \unwrapped\fuse.exe -incremental -o cla_add_n_bit_tb_isim_beh.exe -prj
cla_add_n_bit_tb.prj -top cla_add_n_bit_tb
ISim P.20131013 ( signature 0x7708f090 )
Number of CPUs detected in this system: 8
Turning on mult-threading, number of parallel sub-compilation jobs: 16
Determining compilation order of HDL files
Parsing VHDL file "cla_gp.vhd" into library work
Parsing VHDL file "cla_add_n_bit.vhd" into library work
Parsing VHDL file "cla_add_n_bit_tb_IDEAL.vhd" into library work
Starting static elaboration
Completed static elaboration
Compiling package standard
Compiling package std_logic_1164
Compiling package textio
Compiling package std_logic_textio
Compiling package numeric_std
Compiling package attributes
Compiling package std_logic_misc
Compiling architecture ndv of entity cla_add_n_bit [\cla_add_n_bit( 8 )\]
Compiling architecture testbench_arch of entity cla_add_n_bit_tb
Time Resolution for simulation is 1ps.
Waiting for 1 sub-compilation( s ) to finish...
Compiled 10 VHDL Units
Built simulation executable cla_add_n_bit_tb_isim_beh.exe

```

Fuse Memory Usage: 37460 KB
Fuse CPU Usage: 968 ms

```
64240430>cla_add_n_bit_tb_isim_beh.exe -tclbatch isim.tcl -wdb
cla_add_n_bit_tb_isim_beh.wdb
ISim P.20131013 ( signature 0x7708f090 )
WARNING: A WEBPACK license was found.
WARNING: Please use Xilinx License Configuration Manager to check out a full ISim
license.
WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for
more information on the differences between the Lite and the Full version.
This is a Lite version of ISim.
Time resolution is 1 ps
Simulator is doing circuit initialization process.
Finished circuit initialization process.
```

```
64240430>rem ***** test cla flags
```

```
64240430>xst -ifn cla_add_n_bit_flags.xst
Release 14.7 - xst P.20131013 ( nt64 )
Copyright ( c ) 1995-2013 Xilinx, Inc. All rights reserved.
-- > Parameter TMPDIR set to xst/projnav.tmp
```

Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.24 secs

```
-- > Parameter xsthdpdir set to xst
```

Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.25 secs

```
-- > ERROR:Xst:438 - Can not open file : cla_add_n_bit_flags.prj
```

Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.27 secs

```
-- >
```

Total memory usage is 4422880 kilobytes

Number of errors : 1 (0 filtered)
Number of warnings : 0 (0 filtered)
Number of infos : 0 (0 filtered)

```
64240430>fuse -incremental -o cla_add_n_bit_tb_flags_isim_beh.exe -prj
cla_add_n_bit_flags_tb.prj -top cla_add_n_bit_flags_tb_IDEAL
Running: \unwrapped\fuse.exe -incremental -o cla_add_n_bit_tb_flags_isim_beh.exe -
prj cla_add_n_bit_flags_tb.prj -top cla_add_n_bit_flags_tb_IDEAL
ISim P.20131013 ( signature 0x7708f090 )
Number of CPUs detected in this system: 8
Turning on mult-threading, number of parallel sub-compilation jobs: 16
Determining compilation order of HDL files
Parsing VHDL file "cla_gp.vhd" into library work
Parsing VHDL file "cla_add_n_bit.vhd" into library work
Parsing VHDL file "cla_add_n_bit_flags_tb_IDEAL.vhd" into library work
Starting static elaboration
Completed static elaboration
Compiling package standard
Compiling package std_logic_1164
```

```

Compiling package textio
Compiling package std_logic_textio
Compiling package numeric_std
Compiling package attributes
Compiling package std_logic_misc
Compiling architecture ndv of entity cla_add_n_bit [\cla_add_n_bit( 8 )\]
Compiling architecture a1 of entity cla_add_n_bit_flags_tb_ideal
Time Resolution for simulation is 1ps.
Waiting for 1 sub-compilation( s ) to finish...
Compiled 10 VHDL Units
Built simulation executable cla_add_n_bit_tb_flags_isim_beh.exe
Fuse Memory Usage: 37508 KB
Fuse CPU Usage: 983 ms

64240430>cla_add_n_bit_tb_flags_isim_beh.exe -tclbatch isim.tcl -wdb
cla_add_n_bit_flags_tb.wdb
ISim P.20131013 ( signature 0x7708f090 )
WARNING: A WEBPACK license was found.
WARNING: Please use Xilinx License Configuration Manager to check out a full ISim
license.
WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for
more information on the differences between the Lite and the Full version.
This is a Lite version of ISim.
Time resolution is 1 ps
Simulator is doing circuit initialization process.
Finished circuit initialization process.

64240430>rem ***** test alu operations

64240430>xst -ifn alu_cla.xst
Release 14.7 - xst P.20131013 ( nt64 )
Copyright ( c ) 1995-2013 Xilinx, Inc. All rights reserved.
-- > Parameter TMPDIR set to xst/projnav.tmp

Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.25 secs

-- > Parameter xsthdmdir set to xst

Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.25 secs

-- >
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8.4.1 ) Clock Information

```

- 8.4.2) Asynchronous Control Signals Information
- 8.4.3) Timing Summary
- 8.4.4) Timing Details
- 8.4.5) Cross Clock Domains [Report](#)

```

=====
* Synthesis Options Summary *
=====
--      -- Source Parameters
Input File Name : "alu_cla.prj"
Ignore Synthesis Constraint File : NO

--      -- Target Parameters
Output File Name : "alu_cla"
Output Format : NGC
Target Device : xc6slx4-3-tqg144

--      -- Source Options
Top Module Name : alu_cla
Automatic FSM Extraction : YES
FSM Encoding Algorithm : Auto
Safe Implementation : No
FSM Style : LUT
RAM Extraction : Yes
RAM Style : Auto
ROM Extraction : Yes
Shift Register Extraction : YES
ROM Style : Auto
Resource Sharing : YES
Asynchronous To Synchronous : NO
Shift Register Minimum Size : 2
Use DSP Block : Auto
Automatic Register Balancing : No

--      -- Target Options
LUT Combining : Auto
Reduce Control Sets : Auto
Add IO Buffers : YES
Global Maximum Fanout : 100000
Add Generic Clock Buffer( BUFG ) : 16
Register Duplication : YES
Optimize Instantiated Primitives : NO
Use Clock Enable : Auto
Use Synchronous Set : Auto
Use Synchronous Reset : Auto
Pack IO Registers into IOBs : Auto
Equivalent register Removal : YES

--      -- General Options
Optimization Goal : Speed
Optimization Effort : 1
Power Reduction : NO
Keep Hierarchy : No
Netlist Hierarchy : As_Optimized
RTL Output : Yes
Global Optimization : AllClockNets
Read Cores : YES
Write Timing Constraints : NO
Cross Clock Analysis : NO

```

Hierarchy Separator : /
Bus Delimiter : <>
Case Specifier : Maintain
Slice Utilization Ratio : 100
BRAM Utilization Ratio : 100
DSP48 Utilization Ratio : 100
Auto BRAM Packing : NO
Slice Utilization Ratio Delta : 5

=====

=====

* HDL Parsing *

=====

Parsing VHDL file "64240430\cla_gp.vhd" into library work
Parsing entity <cla_gp>.
Parsing architecture <ideal> of entity <cla_gp>.
Parsing VHDL file "64240430\cla_add_n_bit.vhd" into library work
Parsing entity <cla_add_n_bit>.
Parsing architecture <NDV> of entity <cla_add_n_bit>.
Parsing VHDL file "64240430\alu_cla.vhd" into library work
Parsing entity <alu_cla>.
Parsing architecture <NDV> of entity <alu_cla>.

=====

* HDL Elaboration *

=====

Elaborating entity <alu_cla> (architecture <NDV>) with generics from library <work>.

Elaborating entity <cla_add_n_bit> (architecture <NDV>) with generics from library <work>.

=====

* HDL Synthesis *

=====

Synthesizing Unit <alu_cla>.

Related source file is "64240430\alu_cla.vhd".

n = 8

Found 8-bit 12-to-1 multiplexer for signal <S> created at line 65.

Summary:

inferred 8 Multiplexer(s).

Unit <alu_cla> synthesized.

Synthesizing Unit <cla_add_n_bit>.

Related source file is "64240430\cla_add_n_bit.vhd".

n = 8

Summary:

Unit <cla_add_n_bit> synthesized.

=====

HDL Synthesis Report

Macro Statistics

Multiplexers : 8

1-bit 2-to-1 multiplexer : 1

8-bit 12-to-1 multiplexer : 1

```
8-bit 2-to-1 multiplexer : 6
# Xors : 17
1-bit xor2 : 16
8-bit xor2 : 1
```

=====

=====

* Advanced HDL Synthesis *

=====

=====

Advanced HDL Synthesis Report

Macro Statistics

```
# Multiplexers : 8
1-bit 2-to-1 multiplexer : 1
8-bit 12-to-1 multiplexer : 1
8-bit 2-to-1 multiplexer : 6
# Xors : 17
1-bit xor2 : 16
8-bit xor2 : 1
```

=====

=====

* Low Level Synthesis *

=====

Optimizing unit <alu_cla> ...

Optimizing unit <cla_add_n_bit> ...

Mapping all equations...

Building and optimizing final netlist ...

Found area constraint ratio of 100 (+ 5) on block alu_cla, actual ratio is 3.

Final Macro Processing ...

=====

Final Register Report

Found no macro

=====

=====

* Partition Report *

=====

Partition Implementation Status

```
--      --      --      --      --      --      --      --      --      --      --      --
--      --      --      --      --      --      --      --      --      --      --      --
```

No Partitions were found in this design.

```
--      --      --      --      --      --      --      --      --      --      --      --
--      --      --      --      --      --      --      --      --      --      --      --
```

=====

* Design Summary *

=====

Top Level Output File Name : alu_cla.ngc

Primitive and Black Box Usage:

```
--      --      --      --      --      --      --      --      --      --      --      --
--      --      --
# BELS : 52
# LUT3 : 1
# LUT5 : 13
# LUT6 : 34
# MUXF7 : 4
# IO Buffers : 34
# IBUF : 20
# OBUF : 14
```

Device utilization summary:

```
--      --      --      --      --      --      --      --      --      --      --      --
-
```

Selected Device : 6slx4tqg144-3

Slice Logic Utilization:

Number of Slice LUTs: 48 out of 2400 2%
Number used as Logic: 48 out of 2400 2%

Slice Logic Distribution:

Number of LUT Flip Flop pairs used: 48
Number with an unused Flip Flop: 48 out of 48 100%
Number with an unused LUT: 0 out of 48 0%
Number of fully used LUT-FF pairs: 0 out of 48 0%
Number of unique control sets: 0

IO Utilization:

Number of IOs: 34
Number of bonded IOBs: 34 out of 102 33%

Specific Feature Utilization:

```
--      --      --      --      --      --      --      --      --      --      --      --
-
```

Partition Resource Summary:

```
--      --      --      --      --      --      --      --      --      --      --      --
-
```

No Partitions were found in this design.

```
--      --      --      --      --      --      --      --      --      --      --      --
-
```

=====

Timing Report

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.
FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT
GENERATED AFTER PLACE-and-ROUTE.

Clock Information:


```

--      --      --      --      --      --      --      --      --
No clock signals found in this design

Asynchronous Control Signals Information:
--      --      --      --      --      --      --      --      --
--      --      --      --      --      --      --      --      --
No asynchronous control signals found in this design

Timing Summary:
--      --      --      --      --      --      --      --
Speed Grade: -3

Minimum period: No path found
Minimum input arrival time before clock: No path found
Maximum output required time after clock: No path found
Maximum combinational path delay: 12.374ns

Timing Details:
--      --      --      --      --      --      --      --
All values displayed in nanoseconds ( ns )

=====
Timing constraint: Default path analysis
Total number of paths / destination ports: 1306 / 14
--      --      --      --      --      --      --      --      --
--      --      --      --      --      --      --      --      --
--      --      --      --      --      --      --      --      --
Delay: 12.374ns ( Levels of Logic = 10 )
Source: F<2> ( PAD )
Destination: Overflow ( PAD )

Data Path: F<2> to Overflow
Gate Net
Cell:in->out fanout Delay Delay Logical Name ( Net Name )
--      --      --      --      --      --      --      --      --
--      --      --      --      --      --      --      --      --
--      --      --      --      --      --      --      --      --
IBUF:I->0 32 1.222 1.636 F_2_IBUF ( F_2_IBUF )
LUT6:I1->0 5 0.203 0.943 Mmux_y_temp31 ( y_temp<1> )
LUT5:I2->0 5 0.205 1.059 U1/Carry<3>2 ( U1/Carry<3> )
LUT6:I1->0 1 0.203 0.000 U1/Carry<6>_G ( N21 )
MUXF7:I1->0 3 0.140 0.879 U1/Carry<6> ( U1/Carry<6> )
LUT5:I2->0 1 0.205 0.924 U1/Mxor_vsota<7>_xo<0>1 ( s_temp<7> )
LUT6:I1->0 5 0.203 1.059 Mmux_S22 ( Negative_OBUF )
LUT6:I1->0 1 0.203 0.000 Mmux_Overflow1_G ( N17 )
MUXF7:I1->0 1 0.140 0.579 Mmux_Overflow1 ( Overflow_OBUF )
OBUF:I->0 2.571 Overflow_OBUF ( Overflow )
--      --      --      --      --      --      --      --      --
--      --      --      --      --      --      --      --      --
Total 12.374ns ( 5.295ns logic, 7.079ns route )
( 42.8% logic, 57.2% route )

=====

Cross Clock Domains Report:
--      --      --      --      --      --      --      --      --
--      --      --      --      --      --      --      --      --
=====

```

Total REAL time to Xst completion: 9.00 secs
Total CPU time to Xst completion: 9.25 secs

-- >

Total memory usage is 4487500 kilobytes

Number of errors : 0 (0 filtered)

Number of warnings : 0 (0 filtered)

Number of infos : 0 (0 filtered)

64240430>fuse -incremental -o alu_cla_tb_isim_beh.exe -prj alu_cla_tb.prj -top alu_cla_tb

Running: \unwrapped\fuse.exe -incremental -o alu_cla_tb_isim_beh.exe -prj alu_cla_tb.prj -top alu_cla_tb

ISim P.20131013 (signature 0x7708f090)

Number of CPUs detected in this system: 8

Turning on mult-threading, number of parallel sub-compilation jobs: 16

Determining compilation order of HDL files

Parsing VHDL file "cla_gp.vhd" into library work

Parsing VHDL file "cla_add_n_bit.vhd" into library work

Parsing VHDL file "alu_cla.vhd" into library work

Parsing VHDL file "alu_cla_tb_IDEAL.vhd" into library work

Starting static elaboration

Completed static elaboration

Compiling package standard

Compiling package std_logic_1164

Compiling package textio

Compiling package std_logic_textio

Compiling package numeric_std

Compiling package attributes

Compiling package std_logic_misc

Compiling architecture ndv of entity cla_add_n_bit [\cla_add_n_bit(8)\]

Compiling architecture ndv of entity alu_cla [\alu_cla(8)\]

Compiling architecture testbench_arch of entity alu_cla_tb

Time Resolution for simulation is 1ps.

Waiting for 1 sub-compilation(s) to finish...

Compiled 12 VHDL Units

Built simulation executable alu_cla_tb_isim_beh.exe

Fuse Memory Usage: 37516 KB

Fuse CPU Usage: 999 ms

64240430>alu_cla_tb_isim_beh.exe -tclbatch isim.tcl -wdb alu_cla_tb_isim_beh.wdb

ISim P.20131013 (signature 0x7708f090)

WARNING: A WEBPACK license was found.

WARNING: Please use Xilinx License Configuration Manager to check out a full ISim license.

WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for more information on the differences between the Lite and the Full version.

This is a Lite version of ISim.

Time resolution is 1 ps

Simulator is doing circuit initialization process.

Finished circuit initialization process.

at 7864320 ns, Instance /alu_cla_tb/ : Warning: NUMERIC_STD.TO_UNSIGNED: vector truncated

at 8847360 ns, Instance /alu_cla_tb/ : Warning: NUMERIC_STD.TO_UNSIGNED: vector truncated

at 9830400 ns, Instance /alu_cla_tb/ : Warning: NUMERIC_STD.TO_UNSIGNED: vector truncated

at 10813440 ns, Instance /alu_cla_tb/ : Warning: NUMERIC_STD.TO_UNSIGNED: vector truncated
at 11796480 ns, Instance /alu_cla_tb/ : Warning: NUMERIC_STD.TO_UNSIGNED: vector truncated
at 12779520 ns, Instance /alu_cla_tb/ : Warning: NUMERIC_STD.TO_UNSIGNED: vector truncated
at 13762560 ns, Instance /alu_cla_tb/ : Warning: NUMERIC_STD.TO_UNSIGNED: vector truncated
at 14745600 ns, Instance /alu_cla_tb/ : Warning: NUMERIC_STD.TO_UNSIGNED: vector truncated

64240430>rem ***** test alu flags

64240430>xst -ifn alu_cla_flags.xst
Release 14.7 - xst P.20131013 (nt64)
Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.
-- > Parameter TMPDIR set to xst/projnav.tmp

Total REAL time to Xst completion: 1.00 secs
Total CPU time to Xst completion: 0.23 secs

-- > Parameter xsthdpdir set to xst

Total REAL time to Xst completion: 1.00 secs
Total CPU time to Xst completion: 0.23 secs

-- >

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 - 8.4.5) Cross Clock Domains Report

=====
* Synthesis Options Summary *

-- -- Source Parameters

Input File Name : "alu_cla_flags_tb.prj"
Ignore Synthesis Constraint File : NO

-- -- Target Parameters

Output File Name : "alu_cla_flags_tb"
Output Format : NGC
Target Device : xc6slx4-3-tqg144

-- -- Source Options

Top Module Name : alu_cla_flags_tb
Automatic FSM Extraction : YES
FSM Encoding Algorithm : Auto
Safe Implementation : No
FSM Style : LUT
RAM Extraction : Yes
RAM Style : Auto
ROM Extraction : Yes
Shift Register Extraction : YES
ROM Style : Auto
Resource Sharing : YES
Asynchronous To Synchronous : NO
Shift Register Minimum Size : 2
Use DSP Block : Auto
Automatic Register Balancing : No

-- -- Target Options

LUT Combining : Auto
Reduce Control Sets : Auto
Add IO Buffers : YES
Global Maximum Fanout : 100000
Add Generic Clock Buffer(BUFG) : 16
Register Duplication : YES
Optimize Instantiated Primitives : NO
Use Clock Enable : Auto
Use Synchronous Set : Auto
Use Synchronous Reset : Auto
Pack IO Registers into IOBs : Auto
Equivalent register Removal : YES

-- -- General Options

Optimization Goal : Speed
Optimization Effort : 1
Power Reduction : NO
Keep Hierarchy : No
Netlist Hierarchy : As_Optimized
RTL Output : Yes
Global Optimization : AllClockNets
Read Cores : YES
Write Timing Constraints : NO
Cross Clock Analysis : NO
Hierarchy Separator : /
Bus Delimiter : <>
Case Specifier : Maintain
Slice Utilization Ratio : 100
BRAM Utilization Ratio : 100
DSP48 Utilization Ratio : 100
Auto BRAM Packing : NO
Slice Utilization Ratio Delta : 5

=====

=====

* HDL Parsing *

=====

Parsing VHDL file "64240430\cla_gp.vhd" into library work
Parsing entity <cla_gp>.

```

Parsing architecture <ideal> of entity <cla_gp>.
Parsing VHDL file "64240430\cla_add_n_bit.vhd" into library work
Parsing entity <cla_add_n_bit>.
Parsing architecture <NDV> of entity <cla_add_n_bit>.
Parsing VHDL file "64240430\alu_cla.vhd" into library work
Parsing entity <alu_cla>.
Parsing architecture <NDV> of entity <alu_cla>.
Parsing VHDL file "64240430\alu_cla_tb_FLAGS_IDEAL.vhd" into library work
Parsing entity <alu_cla_flags_tb>.
Parsing architecture <test_alu_flags> of entity <alu_cla_flags_tb>.

=====
* HDL Elaboration *
=====

Elaborating entity <alu_cla_flags_tb> ( architecture <test_alu_flags> ) with
generics from library <work>.

Elaborating entity <alu_cla> ( architecture <NDV> ) with generics from library
<work>.

Elaborating entity <cla_add_n_bit> ( architecture <NDV> ) with generics from
library <work>.
ERROR:HDLCompiler:890 - "64240430\alu_cla_tb_FLAGS_IDEAL.vhd" Line 144: wait
statement without UNTIL clause not supported for synthesis
Netlist alu_cla_flags_tb( 8 )( test_alu_flags ) remains a blackbox, due to errors
in its contents
-- >

Total memory usage is 4466680 kilobytes

Number of errors : 1 ( 0 filtered )
Number of warnings : 0 ( 0 filtered )
Number of infos : 0 ( 0 filtered )

64240430>fuse -incremental -o alu_cla_flags_tb_isim_beh.exe -prj
alu_cla_flags_tb.prj -top alu_cla_flags_tb
Running: \unwrapped\fuse.exe -incremental -o alu_cla_flags_tb_isim_beh.exe -prj
alu_cla_flags_tb.prj -top alu_cla_flags_tb
ISim P.20131013 ( signature 0x7708f090 )
Number of CPUs detected in this system: 8
Turning on mult-threading, number of parallel sub-compilation jobs: 16
Determining compilation order of HDL files
Parsing VHDL file "cla_gp.vhd" into library work
Parsing VHDL file "cla_add_n_bit.vhd" into library work
Parsing VHDL file "alu_cla.vhd" into library work
Parsing VHDL file "alu_cla_tb_FLAGS_IDEAL.vhd" into library work
Starting static elaboration
Completed static elaboration
Compiling package standard
Compiling package std_logic_1164
Compiling package textio
Compiling package std_logic_textio
Compiling package numeric_std
Compiling package attributes
Compiling package std_logic_misc
Compiling architecture ndv of entity cla_add_n_bit [\cla_add_n_bit( 8 )\]
Compiling architecture ndv of entity alu_cla [\alu_cla( 8 )\]
Compiling architecture test_alu_flags of entity alu_cla_flags_tb

```

Time Resolution for simulation is 1ps.
Waiting for 1 sub-compilation(s) to finish...
Compiled 12 VHDL Units
Built simulation executable alu_cla_flags_tb_isim_beh.exe
Fuse Memory Usage: 37468 KB
Fuse CPU Usage: 936 ms

64240430>alu_cla_flags_tb_isim_beh.exe -tclbatch isim.tcl -wdb
alu_cla_flags_tb_isim_beh.wdb
ISim P.20131013 (signature 0x7708f090)
WARNING: A WEBPACK license was found.
WARNING: Please use Xilinx License Configuration Manager to check out a full ISim license.
WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for more information on the differences between the Lite and the Full version.
This is a Lite version of ISim.
Time resolution is 1 ps
Simulator is doing circuit initialization process.
Finished circuit initialization process.

```
-- *****
-- **** STUDENT: IDEAL
-- *****
-- KOMENTARJI K OCENI NALOGE
-- Matej Možek: Ni pripomb
-- *****
```

```
IDEAL>rem ***** test cla adder
```

```
IDEAL>if not exist "xst" mkdir xst
```

```
IDEAL>cd XST
```

```
IDEAL\xst>if not exist "projnav.tmp" mkdir "projnav.tmp"
```

```
IDEAL\xst>cd ..
```

```
IDEAL>rem ***** test cla operations
```

```
IDEAL>xst -ifn cla_add_n_bit.xst
Release 14.7 - xst P.20131013 ( nt64 )
Copyright ( c ) 1995-2013 Xilinx, Inc. All rights reserved.
-- > Parameter TMPDIR set to xst/projnav.tmp
```

```
Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.37 secs
```

```
-- > Parameter xsthdpdir set to xst
```

```
Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.37 secs
```

```
-- >
```

```
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 - 8.4.5) Cross Clock Domains Report

```
=====
* Synthesis Options Summary *
```

```
=====
-- -- Source Parameters
```

```
Input File Name : "cla_add_n_bit.prj"
```

Ignore Synthesis Constraint File : NO

-- -- Target Parameters

Output File Name : "cla_add_n_bit"

Output Format : NGC

Target Device : xc6slx4-3-tqg144

-- -- Source Options

Top Module Name : cla_add_n_bit

Automatic FSM Extraction : YES

FSM Encoding Algorithm : Auto

Safe Implementation : No

FSM Style : LUT

RAM Extraction : Yes

RAM Style : Auto

ROM Extraction : Yes

Shift Register Extraction : YES

ROM Style : Auto

Resource Sharing : YES

Asynchronous To Synchronous : NO

Shift Register Minimum Size : 2

Use DSP Block : Auto

Automatic Register Balancing : No

-- -- Target Options

LUT Combining : Auto

Reduce Control Sets : Auto

Add IO Buffers : YES

Global Maximum Fanout : 100000

Add Generic Clock Buffer(BUFG) : 16

Register Duplication : YES

Optimize Instantiated Primitives : NO

Use Clock Enable : Auto

Use Synchronous Set : Auto

Use Synchronous Reset : Auto

Pack IO Registers into IOBs : Auto

Equivalent register Removal : YES

-- -- General Options

Optimization Goal : Speed

Optimization Effort : 1

Power Reduction : NO

Keep Hierarchy : No

Netlist Hierarchy : As_Optimized

RTL Output : Yes

Global Optimization : AllClockNets

Read Cores : YES

Write Timing Constraints : NO

Cross Clock Analysis : NO

Hierarchy Separator : /

Bus Delimiter : <>

Case Specifier : Maintain

Slice Utilization Ratio : 100

BRAM Utilization Ratio : 100

DSP48 Utilization Ratio : 100

Auto BRAM Packing : NO

Slice Utilization Ratio Delta : 5

=====


```

=====
* HDL Parsing *
=====
Parsing VHDL file "IDEAL\cla_gp.vhd" into library work
Parsing entity <cla_gp>.
Parsing architecture <ideal> of entity <cla_gp>.
Parsing VHDL file "IDEAL\cla_add_n_bit.vhd" into library work
Parsing entity <cla_add_n_bit>.
Parsing architecture <ideal> of entity <cla_add_n_bit>.

=====
* HDL Elaboration *
=====

Elaborating entity <cla_add_n_bit> ( architecture <ideal> ) with generics from
library <work>.

=====
* HDL Synthesis *
=====

Synthesizing Unit <cla_add_n_bit>.
Related source file is "IDEAL\cla_add_n_bit.vhd".
  n = 8
  Summary:
Unit <cla_add_n_bit> synthesized.

=====
HDL Synthesis Report

Macro Statistics
# Xors : 16
  1-bit xor2 : 16

=====

=====
* Advanced HDL Synthesis *
=====

=====
Advanced HDL Synthesis Report

Macro Statistics
# Xors : 16
  1-bit xor2 : 16

=====

=====
* Low Level Synthesis *
=====

Optimizing unit <cla_add_n_bit> ...

Mapping all equations...
Building and optimizing final netlist ...

```

Found area constraint ratio of 100 (+ 5) on block cla_add_n_bit, actual ratio is 1.

Final Macro Processing ...

=====
Final Register Report

Found no macro

=====
* Partition Report *
=====

Partition Implementation Status

-- -- -- -- -- -- -- -- -- -- -- -- -- --
-- -- -

No Partitions were found in this design.

-- -- -- -- -- -- -- -- -- -- -- -- -- --
-- -- -

=====
* Design Summary *
=====

Top Level Output File Name : cla_add_n_bit.ngc

Primitive and Black Box Usage:

-- -- -- -- -- -- -- -- -- -- -- -- -- --
-- -- -

BELS : 24
LUT2 : 6
LUT3 : 3
LUT5 : 6
LUT6 : 9
IO Buffers : 28
IBUF : 17
OBUF : 11

Device utilization summary:

-- -- -- -- -- -- -- -- -- -- -- -- -- --
-

Selected Device : 6slx4tqg144-3

Slice Logic Utilization:

Number of Slice LUTs: 24 out of 2400 1%
Number used as Logic: 24 out of 2400 1%

Slice Logic Distribution:

Number of LUT Flip Flop pairs used: 24
Number with an unused Flip Flop: 24 out of 24 100%
Number with an unused LUT: 0 out of 24 0%
Number of fully used LUT-FF pairs: 0 out of 24 0%
Number of unique control sets: 0

IO Utilization:

Number of IOs: 28

Number of bonded IOBs: 28 out of 102 27%

Specific Feature Utilization:

```
-- -- -- -- -- -- -- -- -- -- -- -- -- --
-
```

Partition Resource Summary:

```
-- -- -- -- -- -- -- -- -- -- -- -- -- --
-
```

No Partitions were found in this design.

```
-- -- -- -- -- -- -- -- -- -- -- -- -- --
-
```

=====
Timing Report

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.

FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT
GENERATED AFTER PLACE-and-ROUTE.

Clock Information:

```
-- -- -- -- -- -- -- -- -- -- -- -- -- --
```

No clock signals found in this design

Asynchronous Control Signals Information:

```
-- -- -- -- -- -- -- -- -- -- -- -- -- --
-- -- -- -- -- -- -- -- -- -- -- -- -- --
```

No asynchronous control signals found in this design

Timing Summary:

```
-- -- -- -- -- -- -- -- -- -- -- -- -- --
```

Speed Grade: -3

Minimum period: No path found

Minimum input arrival time before clock: No path found

Maximum output required time after clock: No path found

Maximum combinational path delay: 9.101ns

Timing Details:

```
-- -- -- -- -- -- -- -- -- -- -- -- -- --
```

All values displayed in nanoseconds (ns)

=====
Timing constraint: Default path analysis

Total number of paths / destination ports: 131 / 11

```
-- -- -- -- -- -- -- -- -- -- -- -- -- --
-- -- -- -- -- -- -- -- -- -- -- -- -- --
-- -- -- -- -- -- -- -- -- -- -- -- -- --
```

Delay: 9.101ns (Levels of Logic = 7)

Source: Y<0> (PAD)

Destination: S<7> (PAD)

Data Path: Y<0> to S<7>

Gate Net

Cell:in->out fanout Delay Delay Logical Name (Net Name)

```

--      --      --      --      --      --      --      --      --      --      --
--      --      --      --      --      --      --      --      --      --      --
--      --
IBUF:I->0 6 1.222 0.973 Y_0_IBUF ( Y_0_IBUF )
LUT3:I0->0 2 0.205 0.617 Cint_xtd<3>_SW0 ( N2 )
LUT5:I4->0 3 0.205 0.651 Cint_xtd<3> ( Cint_xtd<3> )
LUT3:I2->0 2 0.205 0.617 Cint_xtd<6>_SW0 ( N4 )
LUT5:I4->0 2 0.205 0.845 Cint_xtd<6> ( Cint_xtd<6> )
LUT5:I2->0 1 0.205 0.579 Mxor_S<7>_xo<0>1 ( S_7_OBUF )
OBUF:I->0 2.571 S_7_OBUF ( S<7> )
--      --      --      --      --      --      --      --      --      --      --
--      --
Total 9.101ns ( 4.818ns logic, 4.283ns route )
( 52.9% logic, 47.1% route )

```

Cross Clock Domains Report:

```

Total REAL time to Xst completion: 9.00 secs
Total CPU time to Xst completion: 9.37 secs

```

```
-- >
```

Total memory usage is 4487500 kilobytes

Number of errors : 0 (0 filtered)

Number of warnings : 0 (0 filtered)

Number of infos : 0 (0 filtered)

```

IDEAL>fuse -incremental -o cla_add_n_bit_tb_isim_beh.exe -prj cla_add_n_bit_tb.prj
-top cla_add_n_bit_tb
Running: \unwrapped\fuse.exe -incremental -o cla_add_n_bit_tb_isim_beh.exe -prj
cla_add_n_bit_tb.prj -top cla_add_n_bit_tb
ISim P.20131013 ( signature 0x7708f090 )
Number of CPUs detected in this system: 8
Turning on mult-threading, number of parallel sub-compilation jobs: 16
Determining compilation order of HDL files
Parsing VHDL file "cla_gp.vhd" into library work
Parsing VHDL file "cla_add_n_bit.vhd" into library work
Parsing VHDL file "cla_add_n_bit_tb_IDEAL.vhd" into library work
Starting static elaboration
Completed static elaboration
Compiling package standard
Compiling package std_logic_1164
Compiling package textio
Compiling package std_logic_textio
Compiling package numeric_std
Compiling package attributes
Compiling package std_logic_misc
Compiling architecture ideal of entity cla_add_n_bit [\cla_add_n_bit( 8 )\]
Compiling architecture testbench_arch of entity cla_add_n_bit_tb
Time Resolution for simulation is 1ps.
Compiled 10 VHDL Units
Built simulation executable cla_add_n_bit_tb_isim_beh.exe
Fuse Memory Usage: 37436 KB

```

Fuse CPU Usage: 906 ms

```
IDEAL>cla_add_n_bit_tb_isim_beh.exe -tclbatch isim.tcl -wdb
cla_add_n_bit_tb_isim_beh.wdb
ISim P.20131013 ( signature 0x7708f090 )
WARNING: A WEBPACK license was found.
WARNING: Please use Xilinx License Configuration Manager to check out a full ISim
license.
WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for
more information on the differences between the Lite and the Full version.
This is a Lite version of ISim.
Time resolution is 1 ps
Simulator is doing circuit initialization process.
Finished circuit initialization process.
```

```
IDEAL>rem ***** test cla flags
```

```
IDEAL>xst -ifn cla_add_n_bit_flags.xst
Release 14.7 - xst P.20131013 ( nt64 )
Copyright ( c ) 1995-2013 Xilinx, Inc. All rights reserved.
-- > Parameter TMPDIR set to xst/projnav.tmp
```

```
Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.24 secs
```

```
-- > Parameter xsthdpdir set to xst
```

```
Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.25 secs
```

```
-- > ERROR:Xst:438 - Can not open file : cla_add_n_bit_flags.prj
```

```
Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.27 secs
```

```
-- >
```

Total memory usage is 4422880 kilobytes

Number of errors : 1 (0 filtered)

Number of warnings : 0 (0 filtered)

Number of infos : 0 (0 filtered)

```
IDEAL>fuse -incremental -o cla_add_n_bit_tb_flags_isim_beh.exe -prj
cla_add_n_bit_flags_tb.prj -top cla_add_n_bit_flags_tb_IDEAL
Running: \unwrapped\fuse.exe -incremental -o cla_add_n_bit_tb_flags_isim_beh.exe -
prj cla_add_n_bit_flags_tb.prj -top cla_add_n_bit_flags_tb_IDEAL
ISim P.20131013 ( signature 0x7708f090 )
Number of CPUs detected in this system: 8
Turning on mult-threading, number of parallel sub-compilation jobs: 16
Determining compilation order of HDL files
Parsing VHDL file "cla_gp.vhd" into library work
Parsing VHDL file "cla_add_n_bit.vhd" into library work
Parsing VHDL file "cla_add_n_bit_flags_tb_IDEAL.vhd" into library work
Starting static elaboration
Completed static elaboration
Compiling package standard
Compiling package std_logic_1164
Compiling package textio
```

```

Compiling package std_logic_textio
Compiling package numeric_std
Compiling package attributes
Compiling package std_logic_misc
Compiling architecture ideal of entity cla_add_n_bit [\cla_add_n_bit( 8 )\]
Compiling architecture a1 of entity cla_add_n_bit_flags_tb_ideal
Time Resolution for simulation is 1ps.
Waiting for 1 sub-compilation( s ) to finish...
Compiled 10 VHDL Units
Built simulation executable cla_add_n_bit_tb_flags_isim_beh.exe
Fuse Memory Usage: 37528 KB
Fuse CPU Usage: 937 ms

IDEAL>cla_add_n_bit_tb_flags_isim_beh.exe -tclbatch isim.tcl -wdb
cla_add_n_bit_flags_tb.wdb
ISim P.20131013 ( signature 0x7708f090 )
WARNING: A WEBPACK license was found.
WARNING: Please use Xilinx License Configuration Manager to check out a full ISim
license.
WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for
more information on the differences between the Lite and the Full version.
This is a Lite version of ISim.
Time resolution is 1 ps
Simulator is doing circuit initialization process.
Finished circuit initialization process.

IDEAL>rem ***** test alu operations

IDEAL>xst -ifn alu_cla.xst
Release 14.7 - xst P.20131013 ( nt64 )
Copyright ( c ) 1995-2013 Xilinx, Inc. All rights reserved.
-- > Parameter TMPDIR set to xst/projnav.tmp

Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.24 secs

-- > Parameter xsthdpdir set to xst

Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.25 secs

-- >
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```

- 8.4.3) Timing Summary
- 8.4.4) Timing Details
- 8.4.5) Cross Clock Domains [Report](#)

```
=====
* Synthesis Options Summary *
=====
```

```
--      -- Source Parameters
```

```
Input File Name : "alu_cla.prj"
```

```
Ignore Synthesis Constraint File : NO
```

```
--      -- Target Parameters
```

```
Output File Name : "alu_cla"
```

```
Output Format : NGC
```

```
Target Device : xc6slx4-3-tqg144
```

```
--      -- Source Options
```

```
Top Module Name : alu_cla
```

```
Automatic FSM Extraction : YES
```

```
FSM Encoding Algorithm : Auto
```

```
Safe Implementation : No
```

```
FSM Style : LUT
```

```
RAM Extraction : Yes
```

```
RAM Style : Auto
```

```
ROM Extraction : Yes
```

```
Shift Register Extraction : YES
```

```
ROM Style : Auto
```

```
Resource Sharing : YES
```

```
Asynchronous To Synchronous : NO
```

```
Shift Register Minimum Size : 2
```

```
Use DSP Block : Auto
```

```
Automatic Register Balancing : No
```

```
--      -- Target Options
```

```
LUT Combining : Auto
```

```
Reduce Control Sets : Auto
```

```
Add IO Buffers : YES
```

```
Global Maximum Fanout : 100000
```

```
Add Generic Clock Buffer( BUFG ) : 16
```

```
Register Duplication : YES
```

```
Optimize Instantiated Primitives : NO
```

```
Use Clock Enable : Auto
```

```
Use Synchronous Set : Auto
```

```
Use Synchronous Reset : Auto
```

```
Pack IO Registers into IOBs : Auto
```

```
Equivalent register Removal : YES
```

```
--      -- General Options
```

```
Optimization Goal : Speed
```

```
Optimization Effort : 1
```

```
Power Reduction : NO
```

```
Keep Hierarchy : No
```

```
Netlist Hierarchy : As_Optimized
```

```
RTL Output : Yes
```

```
Global Optimization : AllClockNets
```

```
Read Cores : YES
```

```
Write Timing Constraints : NO
```

```
Cross Clock Analysis : NO
```

```
Hierarchy Separator : /
```

Bus Delimiter : <>
Case Specifier : Maintain
Slice Utilization Ratio : 100
BRAM Utilization Ratio : 100
DSP48 Utilization Ratio : 100
Auto BRAM Packing : NO
Slice Utilization Ratio Delta : 5

=====

* HDL Parsing *

=====

Parsing VHDL file "IDEAL\cla_gp.vhd" into library work
Parsing entity <cla_gp>.
Parsing architecture <ideal> of entity <cla_gp>.
Parsing VHDL file "IDEAL\cla_add_n_bit.vhd" into library work
Parsing entity <cla_add_n_bit>.
Parsing architecture <ideal> of entity <cla_add_n_bit>.
Parsing VHDL file "IDEAL\alu_cla.vhd" into library work
Parsing entity <alu_cla>.
Parsing architecture <ideal> of entity <alu_cla>.

=====

* HDL Elaboration *

=====

Elaborating entity <alu_cla> (architecture <ideal>) with generics from library <work>.

Elaborating entity <cla_add_n_bit> (architecture <ideal>) with generics from library <work>.

=====

* HDL Synthesis *

=====

Synthesizing Unit <alu_cla>.
Related source file is "IDEAL\alu_cla.vhd".
n = 8
Found 8-bit 12-to-1 multiplexer for signal <S> created at line 103.
Summary:
inferred 28 Multiplexer(s).
Unit <alu_cla> synthesized.

Synthesizing Unit <cla_add_n_bit>.
Related source file is "IDEAL\cla_add_n_bit.vhd".
n = 8
Summary:
Unit <cla_add_n_bit> synthesized.

=====

HDL Synthesis Report

Macro Statistics

Multiplexers : 28
1-bit 2-to-1 multiplexer : 21
8-bit 12-to-1 multiplexer : 1
8-bit 2-to-1 multiplexer : 6


```
# Xors : 17
1-bit xor2 : 16
8-bit xor2 : 1
```

=====

=====

```
* Advanced HDL Synthesis *
```

=====

=====

Advanced HDL Synthesis Report

Macro Statistics

```
# Multiplexers : 28
1-bit 2-to-1 multiplexer : 21
8-bit 12-to-1 multiplexer : 1
8-bit 2-to-1 multiplexer : 6
# Xors : 17
1-bit xor2 : 16
8-bit xor2 : 1
```

=====

=====

```
* Low Level Synthesis *
```

=====

Optimizing unit <alu_cla> ...

Optimizing unit <cla_add_n_bit> ...

Mapping all equations...

Building and optimizing final netlist ...

Found area constraint ratio of 100 (+ 5) on block alu_cla, actual ratio is 4.

Final Macro Processing ...

=====

Final Register Report

Found no macro

=====

=====

```
* Partition Report *
```

=====

Partition Implementation Status

```
--      --      --      --      --      --      --      --      --      --      --      --
--      --      --      --      --      --      --      --      --      --      --      --
```

No Partitions were found in this design.

```
--      --      --      --      --      --      --      --      --      --      --      --
--      --      --      --      --      --      --      --      --      --      --      --
```

=====

```
* Design Summary *
```

=====

Top Level Output File Name : alu_cla.ngc

Primitive and Black Box Usage:

```
--      --      --      --      --      --      --      --      --      --      --      --
--      --      --
# BELS : 62
# LUT3 : 4
# LUT5 : 13
# LUT6 : 43
# MUXF7 : 2
# IO Buffers : 34
# IBUF : 20
# OBUF : 14
```

Device utilization summary:

```
--      --      --      --      --      --      --      --      --      --      --      --
-
```

Selected Device : 6slx4tqg144-3

Slice Logic Utilization:

Number of Slice LUTs: 60 out of 2400 2%
Number used as Logic: 60 out of 2400 2%

Slice Logic Distribution:

Number of LUT Flip Flop pairs used: 60
Number with an unused Flip Flop: 60 out of 60 100%
Number with an unused LUT: 0 out of 60 0%
Number of fully used LUT-FF pairs: 0 out of 60 0%
Number of unique control sets: 0

IO Utilization:

Number of IOs: 34
Number of bonded IOBs: 34 out of 102 33%

Specific Feature Utilization:

```
--      --      --      --      --      --      --      --      --      --      --      --
-
```

Partition Resource Summary:

```
--      --      --      --      --      --      --      --      --      --      --      --
-
```

No Partitions were found in this design.

```
--      --      --      --      --      --      --      --      --      --      --      --
-
```

=====

Timing Report

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.

FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT
GENERATED AFTER PLACE-and-ROUTE.

Clock Information:

```
--      --      --      --      --      --      --      --
```

No clock signals found in this design

Asynchronous Control Signals Information:

```
-- -- -- -- -- -- -- -- -- -- -- -- -- -- -- --
-- -- -- -- -- -- -- -- -- -- -- -- -- -- -- --
```

No asynchronous control signals found in this design

Timing Summary:

```
-- -- -- -- -- -- -- -- -- -- -- -- -- -- -- --
Speed Grade: -3
```

Minimum period: No path found

Minimum input arrival time before clock: No path found

Maximum output required time after clock: No path found

Maximum combinational path delay: 11.243ns

Timing Details:

```
-- -- -- -- -- -- -- -- -- -- -- -- -- -- -- --
All values displayed in nanoseconds ( ns )
```

=====
Timing constraint: Default path analysis

Total number of paths / destination ports: 1252 / 14

```
-- -- -- -- -- -- -- -- -- -- -- -- -- -- -- --
-- -- -- -- -- -- -- -- -- -- -- -- -- -- -- --
-- -- -- -- -- -- -- -- -- -- -- -- -- -- -- --
```

Delay: 11.243ns (Levels of Logic = 9)

Source: F<2> (PAD)

Destination: Overflow (PAD)

Data Path: F<2> to Overflow

Gate Net

Cell:in->out fanout Delay Delay Logical Name (Net Name)

```
-- -- -- -- -- -- -- -- -- -- -- -- -- -- -- --
-- -- -- -- -- -- -- -- -- -- -- -- -- -- -- --
-- -- -- -- -- -- -- -- -- -- -- -- -- -- -- --
```

IBUF:I->0 37 1.222 1.707 F_2_IBUF (F_2_IBUF)

LUT6:I1->0 6 0.203 0.973 Mmux_Y_sig31 (Y_sig<1>)

LUT5:I2->0 4 0.205 1.028 U1/Cint_xtd<3>2 (U1/Cint_xtd<3>)

LUT6:I1->0 1 0.203 0.000 U1/Cint_xtd<6>_G (N23)

MUXF7:I1->0 4 0.140 0.912 U1/Cint_xtd<6> (U1/Cint_xtd<6>)

LUT5:I2->0 5 0.205 0.962 U1/Mxor_S<7>_xo<0>1 (Sum_sig<7>)

LUT6:I2->0 1 0.203 0.000 Mmux_Overflow2_F (N24)

MUXF7:I0->0 1 0.131 0.579 Mmux_Overflow2 (Overflow_OBUF)

OBUF:I->0 2.571 Overflow_OBUF (Overflow)

```
-- -- -- -- -- -- -- -- -- -- -- -- -- -- -- --
-- -- -- -- -- -- -- -- -- -- -- -- -- -- -- --
```

Total 11.243ns (5.083ns logic, 6.160ns route)

(45.2% logic, 54.8% route)

=====
Cross Clock Domains Report:

```
-- -- -- -- -- -- -- -- -- -- -- -- -- -- -- --
```

=====
Total REAL time to Xst completion: 9.00 secs

Total CPU time to Xst completion: 8.99 secs

-- >

Total memory usage is 4487500 kilobytes

Number of errors : 0 (0 filtered)

Number of warnings : 0 (0 filtered)

Number of infos : 0 (0 filtered)

IDEAL>fuse -incremental -o alu_cla_tb_isim_beh.exe -prj alu_cla_tb.prj -top alu_cla_tb

Running: \unwrapped\fuse.exe -incremental -o alu_cla_tb_isim_beh.exe -prj alu_cla_tb.prj -top alu_cla_tb

ISim P.20131013 (signature 0x7708f090)

Number of CPUs detected in this system: 8

Turning on mult-threading, number of parallel sub-compilation jobs: 16

Determining compilation order of HDL files

Parsing VHDL file "cla_gp.vhd" into library work

Parsing VHDL file "cla_add_n_bit.vhd" into library work

Parsing VHDL file "alu_cla.vhd" into library work

Parsing VHDL file "alu_cla_tb_IDEAL.vhd" into library work

Starting static elaboration

Completed static elaboration

Compiling package standard

Compiling package std_logic_1164

Compiling package textio

Compiling package std_logic_textio

Compiling package numeric_std

Compiling package attributes

Compiling package std_logic_misc

Compiling architecture ideal of entity cla_add_n_bit [\cla_add_n_bit(8)\]

Compiling architecture ideal of entity alu_cla [\alu_cla(8)\]

Compiling architecture testbench_arch of entity alu_cla_tb

Time Resolution for simulation is 1ps.

Waiting for 1 sub-compilation(s) to finish...

Compiled 12 VHDL Units

Built simulation executable alu_cla_tb_isim_beh.exe

Fuse Memory Usage: 37672 KB

Fuse CPU Usage: 968 ms

IDEAL>alu_cla_tb_isim_beh.exe -tclbatch isim.tcl -wdb alu_cla_tb_isim_beh.wdb

ISim P.20131013 (signature 0x7708f090)

WARNING: A WEBPACK license was found.

WARNING: Please use Xilinx License Configuration Manager to check out a full ISim license.

WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for more information on the differences between the Lite and the Full version.

This is a Lite version of ISim.

Time resolution is 1 ps

Simulator is doing circuit initialization process.

Finished circuit initialization process.

at 7864320 ns, Instance /alu_cla_tb/ : Warning: NUMERIC_STD.TO_UNSIGNED: vector truncated

at 8847360 ns, Instance /alu_cla_tb/ : Warning: NUMERIC_STD.TO_UNSIGNED: vector truncated

at 9830400 ns, Instance /alu_cla_tb/ : Warning: NUMERIC_STD.TO_UNSIGNED: vector truncated

at 10813440 ns, Instance /alu_cla_tb/ : Warning: NUMERIC_STD.TO_UNSIGNED: vector truncated

at 11796480 ns, Instance /alu_cla_tb/ : Warning: NUMERIC_STD.TO_UNSIGNED: vector truncated
at 12779520 ns, Instance /alu_cla_tb/ : Warning: NUMERIC_STD.TO_UNSIGNED: vector truncated
at 13762560 ns, Instance /alu_cla_tb/ : Warning: NUMERIC_STD.TO_UNSIGNED: vector truncated
at 14745600 ns, Instance /alu_cla_tb/ : Warning: NUMERIC_STD.TO_UNSIGNED: vector truncated

IDEAL>rem ***** test alu flags

IDEAL>xst -ifn alu_cla_flags.xst
Release 14.7 - xst P.20131013 (nt64)
Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.
-- > Parameter TMPDIR set to xst/projnav.tmp

Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.23 secs

-- > Parameter xsthdpdir set to xst

Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.23 secs

-- >

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 - 8.4.5) Cross Clock Domains Report

=====
* Synthesis Options Summary *

=====

-- -- Source Parameters

Input File Name : "alu_cla_flags_tb.prj"
Ignore Synthesis Constraint File : NO

-- -- Target Parameters

Output File Name : "alu_cla_flags_tb"
Output Format : NGC
Target Device : xc6slx4-3-tqg144

-- -- Source Options

Top Module Name : alu_cla_flags_tb
Automatic FSM Extraction : YES
FSM Encoding Algorithm : Auto
Safe Implementation : No
FSM Style : LUT
RAM Extraction : Yes
RAM Style : Auto
ROM Extraction : Yes
Shift Register Extraction : YES
ROM Style : Auto
Resource Sharing : YES
Asynchronous To Synchronous : NO
Shift Register Minimum Size : 2
Use DSP Block : Auto
Automatic Register Balancing : No

-- -- Target Options

LUT Combining : Auto
Reduce Control Sets : Auto
Add IO Buffers : YES
Global Maximum Fanout : 100000
Add Generic Clock Buffer(BUFG) : 16
Register Duplication : YES
Optimize Instantiated Primitives : NO
Use Clock Enable : Auto
Use Synchronous Set : Auto
Use Synchronous Reset : Auto
Pack IO Registers into IOBs : Auto
Equivalent register Removal : YES

-- -- General Options

Optimization Goal : Speed
Optimization Effort : 1
Power Reduction : NO
Keep Hierarchy : No
Netlist Hierarchy : As_Optimized
RTL Output : Yes
Global Optimization : AllClockNets
Read Cores : YES
Write Timing Constraints : NO
Cross Clock Analysis : NO
Hierarchy Separator : /
Bus Delimiter : <>
Case Specifier : Maintain
Slice Utilization Ratio : 100
BRAM Utilization Ratio : 100
DSP48 Utilization Ratio : 100
Auto BRAM Packing : NO
Slice Utilization Ratio Delta : 5

=====

=====

* HDL Parsing *

=====

Parsing VHDL file "IDEAL\cla_gp.vhd" into library work
Parsing entity <cla_gp>.
Parsing architecture <ideal> of entity <cla_gp>.
Parsing VHDL file "IDEAL\cla_add_n_bit.vhd" into library work

```

Parsing entity <cla_add_n_bit>.
Parsing architecture <ideal> of entity <cla_add_n_bit>.
Parsing VHDL file "IDEAL\alu_cla.vhd" into library work
Parsing entity <alu_cla>.
Parsing architecture <ideal> of entity <alu_cla>.
Parsing VHDL file "IDEAL\alu_cla_tb_FLAGS_IDEAL.vhd" into library work
Parsing entity <alu_cla_flags_tb>.
Parsing architecture <test_alu_flags> of entity <alu_cla_flags_tb>.

=====
* HDL Elaboration *
=====

Elaborating entity <alu_cla_flags_tb> ( architecture <test_alu_flags> ) with
generics from library <work>.

Elaborating entity <alu_cla> ( architecture <ideal> ) with generics from library
<work>.

Elaborating entity <cla_add_n_bit> ( architecture <ideal> ) with generics from
library <work>.
ERROR:HDLCompiler:890 - "IDEAL\alu_cla_tb_FLAGS_IDEAL.vhd" Line 144: wait
statement without UNTIL clause not supported for synthesis
Netlist alu_cla_flags_tb( 8 )( test_alu_flags ) remains a blackbox, due to errors
in its contents
-- >

Total memory usage is 4466680 kilobytes

Number of errors : 1 ( 0 filtered )
Number of warnings : 0 ( 0 filtered )
Number of infos : 0 ( 0 filtered )

IDEAL>fuse -incremental -o alu_cla_flags_tb_isim_beh.exe -prj alu_cla_flags_tb.prj
-top alu_cla_flags_tb
Running: \unwrapped\fuse.exe -incremental -o alu_cla_flags_tb_isim_beh.exe -prj
alu_cla_flags_tb.prj -top alu_cla_flags_tb
ISim P.20131013 ( signature 0x7708f090 )
Number of CPUs detected in this system: 8
Turning on mult-threading, number of parallel sub-compilation jobs: 16
Determining compilation order of HDL files
Parsing VHDL file "cla_gp.vhd" into library work
Parsing VHDL file "cla_add_n_bit.vhd" into library work
Parsing VHDL file "alu_cla.vhd" into library work
Parsing VHDL file "alu_cla_tb_FLAGS_IDEAL.vhd" into library work
Starting static elaboration
Completed static elaboration
Compiling package standard
Compiling package std_logic_1164
Compiling package textio
Compiling package std_logic_textio
Compiling package numeric_std
Compiling package attributes
Compiling package std_logic_misc
Compiling architecture ideal of entity cla_add_n_bit [\cla_add_n_bit( 8 )\]
Compiling architecture ideal of entity alu_cla [\alu_cla( 8 )\]
Compiling architecture test_alu_flags of entity alu_cla_flags_tb
Time Resolution for simulation is 1ps.
Waiting for 1 sub-compilation( s ) to finish...

```

Compiled 12 VHDL Units
Built simulation executable alu_cla_flags_tb_isim_beh.exe
Fuse Memory Usage: 37632 KB
Fuse CPU Usage: 906 ms

```
IDEAL>alu_cla_flags_tb_isim_beh.exe -tclbatch isim.tcl -wdb
alu_cla_flags_tb_isim_beh.wdb
ISim P.20131013 ( signature 0x7708f090 )
WARNING: A WEBPACK license was found.
WARNING: Please use Xilinx License Configuration Manager to check out a full ISim
license.
WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for
more information on the differences between the Lite and the Full version.
This is a Lite version of ISim.
Time resolution is 1 ps
Simulator is doing circuit initialization process.
Finished circuit initialization process.
```


