

ERROR:HDLCompiler:890 - "64000225\alu_cla_tb_FLAGS_IDEAL.vhd" Line 144: wait statement witho
ERROR:HDLCompiler:890 - "64190088\alu_cla_tb_FLAGS_IDEAL.vhd" Line 144: wait statement witho
WARNING:HDLCompiler:634 - "64200100\cla_add_n_bit.vhd" Line 23: Net <Gint[0]> does not have a c
WARNING:HDLCompiler:634 - "64200100\cla_add_n_bit.vhd" Line 23: Net <Gint[0]> does not have a c
WARNING:HDLCompiler:634 - "64200100\cla_add_n_bit.vhd" Line 23: Net <Gint[0]> does not have a c
ERROR:HDLCompiler:890 - "64200100\alu_cla_tb_FLAGS_IDEAL.vhd" Line 144: wait statement witho
ERROR:HDLCompiler:890 - "64200112\alu_cla_tb_FLAGS_IDEAL.vhd" Line 144: wait statement witho
ERROR:HDLCompiler:890 - "64200163\alu_cla_tb_FLAGS_IDEAL.vhd" Line 144: wait statement witho
ERROR:HDLCompiler:890 - "64200238\alu_cla_tb_FLAGS_IDEAL.vhd" Line 144: wait statement witho
ERROR:HDLCompiler:890 - "64200288\alu_cla_tb_FLAGS_IDEAL.vhd" Line 144: wait statement witho
ERROR:HDLCompiler:890 - "64200296\alu_cla_tb_FLAGS_IDEAL.vhd" Line 144: wait statement witho
ERROR:HDLCompiler:890 - "64200385\alu_cla_tb_FLAGS_IDEAL.vhd" Line 144: wait statement witho
ERROR:HDLCompiler:890 - "64210113\alu_cla_tb_FLAGS_IDEAL.vhd" Line 144: wait statement witho
ERROR:HDLCompiler:890 - "64210290\alu_cla_tb_FLAGS_IDEAL.vhd" Line 144: wait statement witho
ERROR:HDLCompiler:890 - "64210382\alu_cla_tb_FLAGS_IDEAL.vhd" Line 144: wait statement witho
ERROR:HDLCompiler:890 - "64210384\alu_cla_tb_FLAGS_IDEAL.vhd" Line 144: wait statement witho
WARNING:HDLCompiler:634 - "64210386\cla_add_n_bit.vhd" Line 14: Net <g_ind[0]> does not have a
WARNING:HDLCompiler:634 - "64210386\cla_add_n_bit.vhd" Line 14: Net <g_ind[0]> does not have a
WARNING:HDLCompiler:634 - "64210386\cla_add_n_bit.vhd" Line 14: Net <g_ind[0]> does not have a
ERROR:HDLCompiler:890 - "64210386\alu_cla_tb_FLAGS_IDEAL.vhd" Line 144: wait statement witho
WARNING:HDLCompiler:634 - "64210445\cla_add_n_bit.vhd" Line 14: Net <g_i[0]> does not have a dr
WARNING:HDLCompiler:634 - "64210445\cla_add_n_bit.vhd" Line 14: Net <g_i[0]> does not have a dr
WARNING:HDLCompiler:634 - "64210445\cla_add_n_bit.vhd" Line 14: Net <g_i[0]> does not have a dr
ERROR:HDLCompiler:890 - "64210445\alu_cla_tb_FLAGS_IDEAL.vhd" Line 144: wait statement witho
ERROR:HDLCompiler:806 - "64210455\cla_add_n_bit.vhd" Line 59: Syntax error near ".".
ERROR:HDLCompiler:854 - "64210455\cla_add_n_bit.vhd" Line 18: Unit <arch> ignored due to previou
ERROR:HDLCompiler:806 - "64210455\cla_add_n_bit.vhd" Line 59: Syntax error near ".".
ERROR:HDLCompiler:854 - "64210455\cla_add_n_bit.vhd" Line 18: Unit <arch> ignored due to previou
ERROR:HDLCompiler:806 - "64210455\cla_add_n_bit.vhd" Line 59: Syntax error near ".".
ERROR:HDLCompiler:854 - "64210455\cla_add_n_bit.vhd" Line 18: Unit <arch> ignored due to previou
ERROR:HDLCompiler:890 - "64210457\alu_cla_tb_FLAGS_IDEAL.vhd" Line 144: wait statement witho
ERROR:HDLCompiler:890 - "64240429\alu_cla_tb_FLAGS_IDEAL.vhd" Line 144: wait statement witho
ERROR:HDLCompiler:890 - "64240430\alu_cla_tb_FLAGS_IDEAL.vhd" Line 144: wait statement witho
ERROR:HDLCompiler:890 - "IDEAL\alu_cla_tb_FLAGS_IDEAL.vhd" Line 144: wait statement without L

ut UNTIL clause not supported for synthesis
ut UNTIL clause not supported for synthesis
driver.
driver.
driver.
ut UNTIL clause not supported for synthesis
ut UNTIL clause not supported for synthesis
ut UNTIL clause not supported for synthesis
ut UNTIL clause not supported for synthesis
ut UNTIL clause not supported for synthesis
ut UNTIL clause not supported for synthesis
ut UNTIL clause not supported for synthesis
ut UNTIL clause not supported for synthesis
ut UNTIL clause not supported for synthesis
ut UNTIL clause not supported for synthesis
driver.
driver.
driver.
ut UNTIL clause not supported for synthesis
iver.
iver.
iver.
ut UNTIL clause not supported for synthesis

is errors.

is errors.

is errors.

ut UNTIL clause not supported for synthesis
ut UNTIL clause not supported for synthesis
ut UNTIL clause not supported for synthesis
JNTIL clause not supported for synthesis

<pre> >rem ***** test cla adder @if not exist "%*" mkdir %* >cd XST %cd%>if not exist "%projnav.tmp%" mkdir "%projnav.tmp%" %cd%> >rem ***** test cla operations >set -fh cla_add n_bit xst Release 14.7 - xst P 20131013 (n664) Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved. --> Parameter TMPDIR set to xst\projnav.tmp Total REAL time to Xst completion: 0.00 secs Total CPU time to Xst completion: 0.23 secs --> Parameter xst\hdcidr set to xst Total REAL time to Xst completion: 0.00 secs Total CPU time to Xst completion: 0.23 secs --> TABLE OF CONTENTS 1) Synthesis Options Summary 2) HDL Parasit 3) HDL Elaboration 4) HDL Synthesis 4.1) HDL Synthesis Report 5) Advanced HDL Synthesis 5.1) Advanced HDL Synthesis Report 6) Low Level Synthesis 7) Partition Report 8) Design Summary 8.1) Primitive and Black Box Usage 8.2) Device utilization summary 8.3) Partition Resource Summary 8.4) Timing Report 8.4.1) Clock Information 8.4.2) Asynchronous Control Signals Information 8.4.3) Timing Summary 8.4.4) Timing Details 8.4.5) Cross Clock Domains Report Synthesis Options Summary --- Source Parameters Input File Name : "cla_add n_bit.prj" Ignore Synthesis Constraint File : NO --- Target Parameters Output File Name : "cla_add n_bit" Output Format : NDC Target Device : xc6slx4-3-tqg144 --- Source Options Top Module Name : cla_add n_bit Automatic FSM Extraction : YES FSM Encoding Algorithm : Auto Sata Implementation : No FSM Style : LUT RAM Extraction : Yes ROM Extraction : Yes Shift Register Extraction : YES RCM Style : Auto Resource Sharing : YES Asynchronous To Synchronous : NO Shift Register Minimum Size : 2 Use DSP Block : Auto Automatic Register Balancing : No --- Target Options LUT Combining : Auto Reduce Control Sels : Auto Add IO Buffers : YES </pre>		<pre> >rem ***** test cla adder @if not exist "%*" mkdir %* >cd XST %cd%>if not exist "%projnav.tmp%" mkdir "%projnav.tmp%" %cd%> >rem ***** test cla operations >set -fh cla_add n_bit xst Release 14.7 - xst P 20131013 (n664) Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved. --> Parameter TMPDIR set to xst\projnav.tmp Total REAL time to Xst completion: 0.00 secs Total CPU time to Xst completion: 0.37 secs --> Parameter xst\hdcidr set to xst Total REAL time to Xst completion: 0.00 secs Total CPU time to Xst completion: 0.37 secs --> TABLE OF CONTENTS 1) Synthesis Options Summary 2) HDL Parasit 3) HDL Elaboration 4) HDL Synthesis 4.1) HDL Synthesis Report 5) Advanced HDL Synthesis 5.1) Advanced HDL Synthesis Report 6) Low Level Synthesis 7) Partition Report 8) Design Summary 8.1) Primitive and Black Box Usage 8.2) Device utilization summary 8.3) Partition Resource Summary 8.4) Timing Report 8.4.1) Clock Information 8.4.2) Asynchronous Control Signals Information 8.4.3) Timing Summary 8.4.4) Timing Details 8.4.5) Cross Clock Domains Report Synthesis Options Summary --- Source Parameters Input File Name : "cla_add n_bit.prj" Ignore Synthesis Constraint File : NO --- Target Parameters Output File Name : "cla_add n_bit" Output Format : NDC Target Device : xc6slx4-3-tqg144 --- Source Options Top Module Name : cla_add n_bit Automatic FSM Extraction : YES FSM Encoding Algorithm : Auto Sata Implementation : No FSM Style : LUT RAM Extraction : Yes ROM Extraction : Yes Shift Register Extraction : YES RCM Style : Auto Resource Sharing : YES Asynchronous To Synchronous : NO Shift Register Minimum Size : 2 Use DSP Block : Auto Automatic Register Balancing : No --- Target Options LUT Combining : Auto Reduce Control Sels : Auto Add IO Buffers : YES </pre>	
--	--	--	--

<pre> >rem ***** test cla adder @if not exist "%x%" mkdir %x% >cd XST >cd-if not exist "%projnav.tmp%" mkdir "%projnav.tmp%" >cd %x% >rem ***** test cla operations >set -lh cla_add n_bit xst Release 14.7 - xst P 20131013 (n664) Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved. --> Parameter TMPDIR set to xst\projnav.tmp Total REAL time to Xst completion: 0.00 secs Total CPU time to Xst completion: 0.24 secs --> Parameter xsthdiclr set to xst Total REAL time to Xst completion: 0.00 secs Total CPU time to Xst completion: 0.24 secs --> TABLE OF CONTENTS 1) Synthesis Options Summary 2) HDL Parasit 3) HDL Elaboration 4) HDL Synthesis 4.1) HDL Synthesis Report 5) Advanced HDL Synthesis 5.1) Advanced HDL Synthesis Report 6) Low Level Synthesis 7) Partition Report 8) Design Summary 8.1) Primitive and Black Box Usage 8.2) Device utilization summary 8.3) Partition Resource Summary 8.4) Timing Report 8.4.1) Clock Information 8.4.2) Asynchronous Control Signals Information 8.4.3) Timing Summary 8.4.4) Timing Details 8.4.5) Cross Clock Domains Report Synthesis Options Summary --- Source Parameters Input File Name : "cla_add n_bit.prj" Ignore Synthesis Constraint File : NO --- Target Parameters Output File Name : "cla_add n_bit" Output Format : NDC Target Device : xc6slx4-3-tqg144 --- Source Options Top Module Name : cla_add n_bit Automatic FSM Extraction : YES FSM Encoding Algorithm : Auto Sata Implementation : No FSM Style : LUT RAM Extraction : Yes ROM Style : Auto ROM Extraction : Yes Shift Register Extraction : YES RCM Style : Auto Resource Sharing : YES Asynchronous To Synchronous : NO Shift Register Minimum Size : 2 Use DSP Block : Auto Automatic Register Balancing : No --- Target Options LUT Combining : Auto Reduce Control Sels : Auto Add IO Buffers : YES </pre>		<pre> >rem ***** test cla adder @if not exist "%x%" mkdir %x% >cd XST >cd-if not exist "%projnav.tmp%" mkdir "%projnav.tmp%" >cd %x% >rem ***** test cla operations >set -lh cla_add n_bit xst Release 14.7 - xst P 20131013 (n664) Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved. --> Parameter TMPDIR set to xst\projnav.tmp Total REAL time to Xst completion: 0.00 secs Total CPU time to Xst completion: 0.37 secs --> Parameter xsthdiclr set to xst Total REAL time to Xst completion: 0.00 secs Total CPU time to Xst completion: 0.37 secs --> TABLE OF CONTENTS 1) Synthesis Options Summary 2) HDL Parasit 3) HDL Elaboration 4) HDL Synthesis 4.1) HDL Synthesis Report 5) Advanced HDL Synthesis 5.1) Advanced HDL Synthesis Report 6) Low Level Synthesis 7) Partition Report 8) Design Summary 8.1) Primitive and Black Box Usage 8.2) Device utilization summary 8.3) Partition Resource Summary 8.4) Timing Report 8.4.1) Clock Information 8.4.2) Asynchronous Control Signals Information 8.4.3) Timing Summary 8.4.4) Timing Details 8.4.5) Cross Clock Domains Report Synthesis Options Summary --- Source Parameters Input File Name : "cla_add n_bit.prj" Ignore Synthesis Constraint File : NO --- Target Parameters Output File Name : "cla_add n_bit" Output Format : NDC Target Device : xc6slx4-3-tqg144 --- Source Options Top Module Name : cla_add n_bit Automatic FSM Extraction : YES FSM Encoding Algorithm : Auto Sata Implementation : No FSM Style : LUT RAM Extraction : Yes ROM Style : Auto ROM Extraction : Yes Shift Register Extraction : YES RCM Style : Auto Resource Sharing : YES Asynchronous To Synchronous : NO Shift Register Minimum Size : 2 Use DSP Block : Auto Automatic Register Balancing : No --- Target Options LUT Combining : Auto Reduce Control Sels : Auto Add IO Buffers : YES </pre>	
---	--	---	--

<pre> >rem ***** test cla adder @if not exist "%x%" mkdir %x% >cd %XST% >cd %if not exist "%projnav.tmp%" mkdir "%projnav.tmp%" >cd %x% >rem ***** test cla operations >set -fh cla_add n_bit xst Release 14.7 - xst P 20131013 (n664) Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved. --> Parameter TMPDIR set to xst\projnav.tmp Total REAL time to Xst completion: 0.00 secs Total CPU time to Xst completion: 0.24 secs --> Parameter xst\hdcidr set to xst Total REAL time to Xst completion: 0.00 secs Total CPU time to Xst completion: 0.24 secs --> TABLE OF CONTENTS 1) Synthesis Options Summary 2) HDL Parasit 3) HDL Elaboration 4) HDL Synthesis 4.1) HDL Synthesis Report 5) Advanced HDL Synthesis 5.1) Advanced HDL Synthesis Report 6) Low Level Synthesis 7) Partition Report 8) Design Summary 8.1) Primitive and Black Box Usage 8.2) Device utilization summary 8.3) Partition Resource Summary 8.4) Timing Report 8.4.1) Clock Information 8.4.2) Asynchronous Control Signals Information 8.4.3) Timing Summary 8.4.4) Timing Details 8.4.5) Cross Clock Domains Report Synthesis Options Summary --- Source Parameters Input File Name : "cla_add n_bit.prj" Ignore Synthesis Constraint File : NO --- Target Parameters Output File Name : "cla_add n_bit" Output Format : NGC Target Device : xc6slx14-3-tqg144 --- Source Options Top Module Name : cla_add n_bit Automatic FSM Extraction : YES FSM Encoding Algorithm : Auto Sata Implementation : No FSM Style : LUT RAM Extraction : Yes ROM Style : Auto ROM Extraction : Yes Shift Register Extraction : YES RCM Style : Auto Resource Sharing : YES Asynchronous To Synchronous : NO Shift Register Minimum Size : 2 Use DSP Block : Auto Automatic Register Balancing : No --- Target Options LUT Combining : Auto Reduce Control Sels : Auto Add IO Buffers : YES </pre>		<pre> >rem ***** test cla adder @if not exist "%x%" mkdir %x% >cd %XST% >cd %if not exist "%projnav.tmp%" mkdir "%projnav.tmp%" >cd %x% >rem ***** test cla operations >set -fh cla_add n_bit xst Release 14.7 - xst P 20131013 (n664) Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved. --> Parameter TMPDIR set to xst\projnav.tmp Total REAL time to Xst completion: 0.00 secs Total CPU time to Xst completion: 0.37 secs --> Parameter xst\hdcidr set to xst Total REAL time to Xst completion: 0.00 secs Total CPU time to Xst completion: 0.37 secs --> TABLE OF CONTENTS 1) Synthesis Options Summary 2) HDL Parasit 3) HDL Elaboration 4) HDL Synthesis 4.1) HDL Synthesis Report 5) Advanced HDL Synthesis 5.1) Advanced HDL Synthesis Report 6) Low Level Synthesis 7) Partition Report 8) Design Summary 8.1) Primitive and Black Box Usage 8.2) Device utilization summary 8.3) Partition Resource Summary 8.4) Timing Report 8.4.1) Clock Information 8.4.2) Asynchronous Control Signals Information 8.4.3) Timing Summary 8.4.4) Timing Details 8.4.5) Cross Clock Domains Report Synthesis Options Summary --- Source Parameters Input File Name : "cla_add n_bit.prj" Ignore Synthesis Constraint File : NO --- Target Parameters Output File Name : "cla_add n_bit" Output Format : NGC Target Device : xc6slx14-3-tqg144 --- Source Options Top Module Name : cla_add n_bit Automatic FSM Extraction : YES FSM Encoding Algorithm : Auto Sata Implementation : No FSM Style : LUT RAM Extraction : Yes ROM Style : Auto ROM Extraction : Yes Shift Register Extraction : YES RCM Style : Auto Resource Sharing : YES Asynchronous To Synchronous : NO Shift Register Minimum Size : 2 Use DSP Block : Auto Automatic Register Balancing : No --- Target Options LUT Combining : Auto Reduce Control Sels : Auto Add IO Buffers : YES </pre>	
--	--	--	--

<pre> >run ***** test cla adder if not exist "%*" mkdir %* >cd XST >cd-if not exist "%projnav.tmp%" mkdir "%projnav.tmp%" >cd %* >run ***** test cla operations >set -lh cla_add n_bit xst Release 14.7 - xst P 20131013 (n664) Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved. --> Parameter TMPDIR set to xst\projnav.tmp Total REAL time to Xst completion: 0.00 secs Total CPU time to Xst completion: 0.23 secs --> Parameter xst\hdcidr set to xst Total REAL time to Xst completion: 0.00 secs Total CPU time to Xst completion: 0.23 secs --> TABLE OF CONTENTS 1) Synthesis Options Summary 2) HDL Parasit 3) HDL Elaboration 4) HDL Synthesis 4.1) HDL Synthesis Report 5) Advanced HDL Synthesis 5.1) Advanced HDL Synthesis Report 6) Low Level Synthesis 7) Partition Report 8) Design Summary 8.1) Primitive and Black Box Usage 8.2) Device utilization summary 8.3) Partition Resource Summary 8.4) Timing Report 8.4.1) Clock Information 8.4.2) Asynchronous Control Signals Information 8.4.3) Timing Summary 8.4.4) Timing Details 8.4.5) Cross Clock Domains Report Synthesis Options Summary --- Source Parameters Input File Name : "cla_add n_bit.prj" Ignore Synthesis Constraint File : NO --- Target Parameters Output File Name : "cla_add n_bit" Output Format : NGC Target Device : xc6slx4-3-tqg144 --- Source Options Top Module Name : cla_add n_bit Automatic FSM Extraction : YES FSM Encoding Algorithm : Auto Sata Implementation : No FSM Style : LUT RAM Extraction : Yes ROM Style : Auto ROM Extraction : Yes Shift Register Extraction : YES RCM Style : Auto Resource Sharing : YES Asynchronous To Synchronous : NO Shift Register Minimum Size : 2 Use DSP Block : Auto Automatic Register Balancing : No --- Target Options LUT Combining : Auto Reduce Control Sels : Auto Add IO Buffers : YES </pre>		<pre> >run ***** test cla adder if not exist "%*" mkdir %* >cd XST >cd-if not exist "%projnav.tmp%" mkdir "%projnav.tmp%" >cd %* >run ***** test cla operations >set -lh cla_add n_bit xst Release 14.7 - xst P 20131013 (n664) Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved. --> Parameter TMPDIR set to xst\projnav.tmp Total REAL time to Xst completion: 0.00 secs Total CPU time to Xst completion: 0.37 secs --> Parameter xst\hdcidr set to xst Total REAL time to Xst completion: 0.00 secs Total CPU time to Xst completion: 0.37 secs --> TABLE OF CONTENTS 1) Synthesis Options Summary 2) HDL Parasit 3) HDL Elaboration 4) HDL Synthesis 4.1) HDL Synthesis Report 5) Advanced HDL Synthesis 5.1) Advanced HDL Synthesis Report 6) Low Level Synthesis 7) Partition Report 8) Design Summary 8.1) Primitive and Black Box Usage 8.2) Device utilization summary 8.3) Partition Resource Summary 8.4) Timing Report 8.4.1) Clock Information 8.4.2) Asynchronous Control Signals Information 8.4.3) Timing Summary 8.4.4) Timing Details 8.4.5) Cross Clock Domains Report Synthesis Options Summary --- Source Parameters Input File Name : "cla_add n_bit.prj" Ignore Synthesis Constraint File : NO --- Target Parameters Output File Name : "cla_add n_bit" Output Format : NGC Target Device : xc6slx4-3-tqg144 --- Source Options Top Module Name : cla_add n_bit Automatic FSM Extraction : YES FSM Encoding Algorithm : Auto Sata Implementation : No FSM Style : LUT RAM Extraction : Yes ROM Style : Auto ROM Extraction : Yes Shift Register Extraction : YES RCM Style : Auto Resource Sharing : YES Asynchronous To Synchronous : NO Shift Register Minimum Size : 2 Use DSP Block : Auto Automatic Register Balancing : No --- Target Options LUT Combining : Auto Reduce Control Sels : Auto Add IO Buffers : YES </pre>	
--	--	--	--

<pre> >rem ***** test cla adder @if not exist "%*" mkdir %* >cd XST >cd-if not exist "%projnav.tmp%" mkdir "%projnav.tmp%" >cd %* >rem ***** test cla operations >set -lh cla_add n_bit xst Release 14.7 - xst P 20131013 (n664) Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved. --> Parameter TMPDIR set to xst\projnav.tmp Total REAL time to Xst completion: 0.00 secs Total CPU time to Xst completion: 0.25 secs --> Parameter xst\hdcidr set to xst Total REAL time to Xst completion: 0.00 secs Total CPU time to Xst completion: 0.25 secs --> TABLE OF CONTENTS 1) Synthesis Options Summary 2) HDL Parasit 3) HDL Elaboration 4) HDL Synthesis 4.1) HDL Synthesis Report 5) Advanced HDL Synthesis 5.1) Advanced HDL Synthesis Report 6) Low Level Synthesis 7) Partition Report 8) Design Summary 8.1) Primitive and Black Box Usage 8.2) Device utilization summary 8.3) Partition Resource Summary 8.4) Timing Report 8.4.1) Clock Information 8.4.2) Asynchronous Control Signals Information 8.4.3) Timing Summary 8.4.4) Timing Details 8.4.5) Cross Clock Domains Report Synthesis Options Summary --- Source Parameters Input File Name : "cla_add n_bit.prj" Ignore Synthesis Constraint File : NO --- Target Parameters Output File Name : "cla_add n_bit" Output Format : NDC Target Device : xc6slx4-3-tqg144 --- Source Options Top Module Name : cla_add n_bit Automatic FSM Extraction : YES FSM Encoding Algorithm : Auto Sata Implementation : No FSM Style : LUT RAM Extraction : Yes ROM Style : Auto ROM Extraction : Yes Shift Register Extraction : YES RCM Style : Auto Resource Sharing : YES Asynchronous To Synchronous : NO Shift Register Minimum Size : 2 Use DSP Block : Auto Automatic Register Balancing : No --- Target Options LUT Combining : Auto Reduce Control Sels : Auto Add IO Buffers : YES </pre>		<pre> >rem ***** test cla adder @if not exist "%*" mkdir %* >cd XST >cd-if not exist "%projnav.tmp%" mkdir "%projnav.tmp%" >cd %* >rem ***** test cla operations >set -lh cla_add n_bit xst Release 14.7 - xst P 20131013 (n664) Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved. --> Parameter TMPDIR set to xst\projnav.tmp Total REAL time to Xst completion: 0.00 secs Total CPU time to Xst completion: 0.37 secs --> Parameter xst\hdcidr set to xst Total REAL time to Xst completion: 0.00 secs Total CPU time to Xst completion: 0.37 secs --> TABLE OF CONTENTS 1) Synthesis Options Summary 2) HDL Parasit 3) HDL Elaboration 4) HDL Synthesis 4.1) HDL Synthesis Report 5) Advanced HDL Synthesis 5.1) Advanced HDL Synthesis Report 6) Low Level Synthesis 7) Partition Report 8) Design Summary 8.1) Primitive and Black Box Usage 8.2) Device utilization summary 8.3) Partition Resource Summary 8.4) Timing Report 8.4.1) Clock Information 8.4.2) Asynchronous Control Signals Information 8.4.3) Timing Summary 8.4.4) Timing Details 8.4.5) Cross Clock Domains Report Synthesis Options Summary --- Source Parameters Input File Name : "cla_add n_bit.prj" Ignore Synthesis Constraint File : NO --- Target Parameters Output File Name : "cla_add n_bit" Output Format : NDC Target Device : xc6slx4-3-tqg144 --- Source Options Top Module Name : cla_add n_bit Automatic FSM Extraction : YES FSM Encoding Algorithm : Auto Sata Implementation : No FSM Style : LUT RAM Extraction : Yes ROM Style : Auto ROM Extraction : Yes Shift Register Extraction : YES RCM Style : Auto Resource Sharing : YES Asynchronous To Synchronous : NO Shift Register Minimum Size : 2 Use DSP Block : Auto Automatic Register Balancing : No --- Target Options LUT Combining : Auto Reduce Control Sels : Auto Add IO Buffers : YES </pre>	
---	--	---	--

<pre> >rem ***** test cla adder @if not exist "%*" mkdir %* >cd XST >cd-if not exist "%projnav.tmp%" mkdir "%projnav.tmp%" >cd %* >rem ***** test cla operations >set -lh cla_add n_bit xst Release 14.7 - xst P 20131013 (n664) Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved. --> Parameter TMPDIR set to xst\projnav.tmp Total REAL time to Xst completion: 0.00 secs Total CPU time to Xst completion: 0.23 secs --> Parameter xst\hdcidr set to xst Total REAL time to Xst completion: 0.00 secs Total CPU time to Xst completion: 0.24 secs --> TABLE OF CONTENTS 1) Synthesis Options Summary 2) HDL Parasit 3) HDL Elaboration 4) HDL Synthesis 4.1) HDL Synthesis Report 5) Advanced HDL Synthesis 5.1) Advanced HDL Synthesis Report 6) Low Level Synthesis 7) Partition Report 8) Design Summary 8.1) Primitive and Black Box Usage 8.2) Device utilization summary 8.3) Partition Resource Summary 8.4) Timing Report 8.4.1) Clock Information 8.4.2) Asynchronous Control Signals Information 8.4.3) Timing Summary 8.4.4) Timing Details 8.4.5) Cross Clock Domains Report Synthesis Options Summary --- Source Parameters Input File Name : "cla_add n_bit.prj" Ignore Synthesis Constraint File : NO --- Target Parameters Output File Name : "cla_add n_bit" Output Format : NDC Target Device : xc6slx1-3-tqg144 --- Source Options Top Module Name : cla_add n_bit Automatic FSM Extraction : YES FSM Encoding Algorithm : Auto Sata Implementation : No FSM Style : LUT RAM Extraction : Yes ROM Style : Auto ROM Extraction : Yes Shift Register Extraction : YES RCM Style : Auto Resource Sharing : YES Asynchronous To Synchronous : NO Shift Register Minimum Size : 2 Use DSP Block : Auto Automatic Register Balancing : No --- Target Options LUT Combining : Auto Reduce Control Sels : Auto Add IO Buffers : YES </pre>		<pre> >rem ***** test cla adder @if not exist "%*" mkdir %* >cd XST >cd-if not exist "%projnav.tmp%" mkdir "%projnav.tmp%" >cd %* >rem ***** test cla operations >set -lh cla_add n_bit xst Release 14.7 - xst P 20131013 (n664) Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved. --> Parameter TMPDIR set to xst\projnav.tmp Total REAL time to Xst completion: 0.00 secs Total CPU time to Xst completion: 0.37 secs --> Parameter xst\hdcidr set to xst Total REAL time to Xst completion: 0.00 secs Total CPU time to Xst completion: 0.37 secs --> TABLE OF CONTENTS 1) Synthesis Options Summary 2) HDL Parasit 3) HDL Elaboration 4) HDL Synthesis 4.1) HDL Synthesis Report 5) Advanced HDL Synthesis 5.1) Advanced HDL Synthesis Report 6) Low Level Synthesis 7) Partition Report 8) Design Summary 8.1) Primitive and Black Box Usage 8.2) Device utilization summary 8.3) Partition Resource Summary 8.4) Timing Report 8.4.1) Clock Information 8.4.2) Asynchronous Control Signals Information 8.4.3) Timing Summary 8.4.4) Timing Details 8.4.5) Cross Clock Domains Report Synthesis Options Summary --- Source Parameters Input File Name : "cla_add n_bit.prj" Ignore Synthesis Constraint File : NO --- Target Parameters Output File Name : "cla_add n_bit" Output Format : NDC Target Device : xc6slx1-3-tqg144 --- Source Options Top Module Name : cla_add n_bit Automatic FSM Extraction : YES FSM Encoding Algorithm : Auto Sata Implementation : No FSM Style : LUT RAM Extraction : Yes ROM Style : Auto ROM Extraction : Yes Shift Register Extraction : YES RCM Style : Auto Resource Sharing : YES Asynchronous To Synchronous : NO Shift Register Minimum Size : 2 Use DSP Block : Auto Automatic Register Balancing : No --- Target Options LUT Combining : Auto Reduce Control Sels : Auto Add IO Buffers : YES </pre>	
---	--	---	--

->rm ***** test cla adder		->rm ***** test cla adder	
if not exist %~1 mkdir %~1		if not exist %~1 mkdir %~1	
>cd XST		>cd XST	
set-if not exist "projnav.tmp" mkdir "projnav.tmp"		set-if not exist "projnav.tmp" mkdir "projnav.tmp"	
set /p		set /p	
:rem ***** test cla operations		:rem ***** test cla operations	
>set -h %~1 add n bit xst		>set -h %~1 add n bit xst	
Release 14.7 - sat P 20131013 (n664)		Release 14.7 - sat P 20131013 (n664)	
Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.		Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.	
-> Parameter TMPDIR set to xst\projnav.tmp		-> Parameter TMPDIR set to xst\projnav.tmp	
Total REAL time to Xst completion: 0.00 secs		Total REAL time to Xst completion: 0.00 secs	
Total CPU time to Xst completion: 0.24 secs		Total CPU time to Xst completion: 0.37 secs	
-> Parameter xsthdiclr set to xst		-> Parameter xsthdiclr set to xst	
Total REAL time to Xst completion: 0.00 secs		Total REAL time to Xst completion: 0.00 secs	
Total CPU time to Xst completion: 0.24 secs		Total CPU time to Xst completion: 0.37 secs	
->		->	
TABLE OF CONTENTS		TABLE OF CONTENTS	
1) Synthesis Options Summary		1) Synthesis Options Summary	
2) HDL Parasite		2) HDL Parasite	
3) HDL Elaboration		3) HDL Elaboration	
4) HDL Synthesis		4) HDL Synthesis	
4.1) HDL Synthesis Report		4.1) HDL Synthesis Report	
5) Advanced HDL Synthesis		5) Advanced HDL Synthesis	
5.1) Advanced HDL Synthesis Report		5.1) Advanced HDL Synthesis Report	
6) Low Level Synthesis		6) Low Level Synthesis	
7) Partition Report		7) Partition Report	
8) Design Summary		8) Design Summary	
8.1) Primitive and Black Box Usage		8.1) Primitive and Black Box Usage	
8.2) Device utilization summary		8.2) Device utilization summary	
8.3) Partition Resource Summary		8.3) Partition Resource Summary	
8.4) Timing Report		8.4) Timing Report	
8.4.1) Clock Information		8.4.1) Clock Information	
8.4.2) Asynchronous Control Signals Information		8.4.2) Asynchronous Control Signals Information	
8.4.3) Timing Summary		8.4.3) Timing Summary	
8.4.4) Timing Details		8.4.4) Timing Details	
8.4.5) Cross Clock Domains Report		8.4.5) Cross Clock Domains Report	
Synthesis Options Summary		Synthesis Options Summary	
--- Source Parameters		--- Source Parameters	
Input File Name : "cla_add_n_bit.prj"		Input File Name : "cla_add_n_bit.prj"	
Ignore Synthesis Constraint File : NO		Ignore Synthesis Constraint File : NO	
--- Target Parameters		--- Target Parameters	
Output File Name : "cla_add_n_bit"		Output File Name : "cla_add_n_bit"	
Output Format : NDC		Output Format : NDC	
Target Device : xc6slx4-3-tqg144		Target Device : xc6slx4-3-tqg144	
--- Source Options		--- Source Options	
Top Module Name : cla_add_n_bit		Top Module Name : cla_add_n_bit	
Automatic FSM Extraction : YES		Automatic FSM Extraction : YES	
FSM Encoding Algorithm : Auto		FSM Encoding Algorithm : Auto	
Sata Implementation : No		Sata Implementation : No	
FSM Style : LUT		FSM Style : LUT	
RAM Extraction : Yes		RAM Extraction : Yes	
ROM Style : Auto		ROM Style : Auto	
ROM Extraction : Yes		ROM Extraction : Yes	
Shift Register Extraction : YES		Shift Register Extraction : YES	
ROM Style : Auto		ROM Style : Auto	
Resource Sharing : YES		Resource Sharing : YES	
Asynchronous To Synchronous : NO		Asynchronous To Synchronous : NO	
Shift Register Minimum Size : 2		Shift Register Minimum Size : 2	
Use DSP Block : Auto		Use DSP Block : Auto	
Automatic Register Balancing : No		Automatic Register Balancing : No	
--- Target Options		--- Target Options	
LUT Combining : Auto		LUT Combining : Auto	
Reduce Control Sels : Auto		Reduce Control Sels : Auto	
Add IO Buffers : YES		Add IO Buffers : YES	

<pre> >rem ***** test cla adder @if not exist "%*" mkdir %* >cd XST >cd %if not exist "%projnav.tmp%" mkdir "%projnav.tmp%" >cd %* >rem ***** test cla operations >set -fh cla_add n_bit xst Release 14.7 - xst P 20131013 (n664) Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved. --> Parameter TMPDIR set to xstprojnav.tmp Total REAL time to Xst completion: 1.00 secs Total CPU time to Xst completion: 0.24 secs --> Parameter xsthdicdir set to xst Total REAL time to Xst completion: 1.00 secs Total CPU time to Xst completion: 0.24 secs --> TABLE OF CONTENTS 1) Synthesis Options Summary 2) HDL Parasit 3) HDL Elaboration 4) HDL Synthesis 4.1) HDL Synthesis Report 5) Advanced HDL Synthesis 5.1) Advanced HDL Synthesis Report 6) Low Level Synthesis 7) Partition Report 8) Design Summary 8.1) Primitive and Black Box Usage 8.2) Device utilization summary 8.3) Partition Resource Summary 8.4) Timing Report 8.4.1) Clock Information 8.4.2) Asynchronous Control Signals Information 8.4.3) Timing Summary 8.4.4) Timing Details 8.4.5) Cross Clock Domains Report Synthesis Options Summary --- Source Parameters Input File Name : "cla_add n_bit.prj" Ignore Synthesis Constraint File : NO --- Target Parameters Output File Name : "cla_add n_bit" Output Format : NCG Target Device : xc6slx4-3-tqg144 --- Source Options Top Module Name : cla_add n_bit Automatic FSM Extraction : YES FSM Encoding Algorithm : Auto Sata Implementation : No FSM Style : LUT RAM Extraction : Yes ROM Extraction : Yes Shift Register Extraction : YES RCM Style : Auto Resource Sharing : YES Asynchronous To Synchronous : NO Shift Register Minimum Size : 2 Use DSP Block : Auto Automatic Register Balancing : No --- Target Options LUT Combining : Auto Reduce Control Sels : Auto Add IO Buffers : YES </pre>	<pre> >rem ***** test cla adder @if not exist "%*" mkdir %* >cd XST >cd %if not exist "%projnav.tmp%" mkdir "%projnav.tmp%" >cd %* >rem ***** test cla operations >set -fh cla_add n_bit xst Release 14.7 - xst P 20131013 (n664) Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved. --> Parameter TMPDIR set to xstprojnav.tmp Total REAL time to Xst completion: 0.00 secs Total CPU time to Xst completion: 0.37 secs --> Parameter xsthdicdir set to xst Total REAL time to Xst completion: 0.00 secs Total CPU time to Xst completion: 0.37 secs --> TABLE OF CONTENTS 1) Synthesis Options Summary 2) HDL Parasit 3) HDL Elaboration 4) HDL Synthesis 4.1) HDL Synthesis Report 5) Advanced HDL Synthesis 5.1) Advanced HDL Synthesis Report 6) Low Level Synthesis 7) Partition Report 8) Design Summary 8.1) Primitive and Black Box Usage 8.2) Device utilization summary 8.3) Partition Resource Summary 8.4) Timing Report 8.4.1) Clock Information 8.4.2) Asynchronous Control Signals Information 8.4.3) Timing Summary 8.4.4) Timing Details 8.4.5) Cross Clock Domains Report Synthesis Options Summary --- Source Parameters Input File Name : "cla_add n_bit.prj" Ignore Synthesis Constraint File : NO --- Target Parameters Output File Name : "cla_add n_bit" Output Format : NCG Target Device : xc6slx4-3-tqg144 --- Source Options Top Module Name : cla_add n_bit Automatic FSM Extraction : YES FSM Encoding Algorithm : Auto Sata Implementation : No FSM Style : LUT RAM Extraction : Yes ROM Extraction : Yes Shift Register Extraction : YES RCM Style : Auto Resource Sharing : YES Asynchronous To Synchronous : NO Shift Register Minimum Size : 2 Use DSP Block : Auto Automatic Register Balancing : No --- Target Options LUT Combining : Auto Reduce Control Sels : Auto Add IO Buffers : YES </pre>
--	--

<pre> >rem ***** test cla adder %if not exist "%*" mkdir %* >cd XST %cd-if not exist "%projnav.tmp" mkdir "%projnav.tmp" %cd %* >rem ***** test cla operations >set -lh cla_add n_bit xst Release 14.7 - sat P 20131013 (n664) Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved. --> Parameter TMPDIR set to xst\projnav.tmp Total REAL time to Xst completion: 0.00 secs Total CPU time to Xst completion: 0.28 secs --> Parameter xst\hdcidr set to xst Total REAL time to Xst completion: 0.00 secs Total CPU time to Xst completion: 0.29 secs --> TABLE OF CONTENTS 1) Synthesis Options Summary 2) HDL Parasitc 3) HDL Elaboration 4) HDL Synthesis 4.1) HDL Synthesis Report 5) Advanced HDL Synthesis 5.1) Advanced HDL Synthesis Report 6) Low Level Synthesis 7) Partition Report 8) Design Summary 8.1) Primitive and Black Box Usage 8.2) Device utilization summary 8.3) Partition Resource Summary 8.4) Timing Report 8.4.1) Clock Information 8.4.2) Asynchronous Control Signals Information 8.4.3) Timing Summary 8.4.4) Timing Details 8.4.5) Cross Clock Domains Report Synthesis Options Summary --- Source Parameters Input File Name : "cla_add n_bit.prj" Ignore Synthesis Constraint File : NO --- Target Parameters Output File Name : "cla_add n_bit" Output Format : NGC Target Device : xc6slx4-3-tqg144 --- Source Options Top Module Name : cla_add n_bit Automatic FSM Extraction : YES FSM Encoding Algorithm : Auto Sata Implementation : No FSM Style : LUT RAM Extraction : Yes ROM Style : Auto ROM Extraction : Yes Shift Register Extraction : YES RCM Style : Auto Resource Sharing : YES Asynchronous To Synchronous : NO Shift Register Minimum Size : 2 Use DSP Block : Auto Automatic Register Balancing : No --- Target Options LUT Combining : Auto Reduce Control Sels : Auto Add IO Buffers : YES </pre>	<pre> >rem ***** test cla adder %if not exist "%*" mkdir %* >cd XST %cd-if not exist "%projnav.tmp" mkdir "%projnav.tmp" %cd %* >rem ***** test cla operations >set -lh cla_add n_bit xst Release 14.7 - sat P 20131013 (n664) Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved. --> Parameter TMPDIR set to xst\projnav.tmp Total REAL time to Xst completion: 0.00 secs Total CPU time to Xst completion: 0.37 secs --> Parameter xst\hdcidr set to xst Total REAL time to Xst completion: 0.00 secs Total CPU time to Xst completion: 0.37 secs --> TABLE OF CONTENTS 1) Synthesis Options Summary 2) HDL Parasitc 3) HDL Elaboration 4) HDL Synthesis 4.1) HDL Synthesis Report 5) Advanced HDL Synthesis 5.1) Advanced HDL Synthesis Report 6) Low Level Synthesis 7) Partition Report 8) Design Summary 8.1) Primitive and Black Box Usage 8.2) Device utilization summary 8.3) Partition Resource Summary 8.4) Timing Report 8.4.1) Clock Information 8.4.2) Asynchronous Control Signals Information 8.4.3) Timing Summary 8.4.4) Timing Details 8.4.5) Cross Clock Domains Report Synthesis Options Summary --- Source Parameters Input File Name : "cla_add n_bit.prj" Ignore Synthesis Constraint File : NO --- Target Parameters Output File Name : "cla_add n_bit" Output Format : NGC Target Device : xc6slx4-3-tqg144 --- Source Options Top Module Name : cla_add n_bit Automatic FSM Extraction : YES FSM Encoding Algorithm : Auto Sata Implementation : No FSM Style : LUT RAM Extraction : Yes ROM Style : Auto ROM Extraction : Yes Shift Register Extraction : YES RCM Style : Auto Resource Sharing : YES Asynchronous To Synchronous : NO Shift Register Minimum Size : 2 Use DSP Block : Auto Automatic Register Balancing : No --- Target Options LUT Combining : Auto Reduce Control Sels : Auto Add IO Buffers : YES </pre>
--	--

<pre> >rem ***** test cla adder @if not exist "%x%" mkdir %x% >cd XST >cd-if not exist "%projnav.tmp%" mkdir "%projnav.tmp%" >cd %x% >rem ***** test cla operations >set -f %x% cla_add n bit xst Release 14.7 - sat P 20131013 (n664) Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved. --> Parameter TMPDIR set to xst\projnav.tmp Total REAL time to Xst completion: 0.00 secs Total CPU time to Xst completion: 0.25 secs --> Parameter xst\hdcidr set to xst Total REAL time to Xst completion: 0.00 secs Total CPU time to Xst completion: 0.25 secs --> TABLE OF CONTENTS 1) Synthesis Options Summary 2) HDL Parasit 3) HDL Elaboration 4) HDL Synthesis 4.1) HDL Synthesis Report 5) Advanced HDL Synthesis 5.1) Advanced HDL Synthesis Report 6) Low Level Synthesis 7) Partition Report 8) Design Summary 8.1) Primitive and Black Box Usage 8.2) Device utilization summary 8.3) Partition Resource Summary 8.4) Timing Report 8.4.1) Clock Information 8.4.2) Asynchronous Control Signals Information 8.4.3) Timing Summary 8.4.4) Timing Details 8.4.5) Cross Clock Domains Report Synthesis Options Summary --- Source Parameters Input File Name : "cla_add n bit.prj" Ignore Synthesis Constraint File : NO --- Target Parameters Output File Name : "cla_add n bit" Output Format : NGC Target Device : xc6slx14-3-tqg144 --- Source Options Top Module Name : cla_add n bit Automatic FSM Extraction : YES FSM Encoding Algorithm : Auto Sata Implementation : No FSM Style : LUT RAM Extraction : Yes ROM Style : Auto ROM Extraction : Yes Shift Register Extraction : YES RCM Style : Auto Resource Sharing : YES Asynchronous To Synchronous : NO Shift Register Minimum Size : 2 Use DSP Block : Auto Automatic Register Balancing : No --- Target Options LUT Combining : Auto Reduce Control Sats : Auto Add IO Buffers : YES </pre>	<pre> >rem ***** test cla adder @if not exist "%x%" mkdir %x% >cd XST >cd-if not exist "%projnav.tmp%" mkdir "%projnav.tmp%" >cd %x% >rem ***** test cla operations >set -f %x% cla_add n bit xst Release 14.7 - sat P 20131013 (n664) Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved. --> Parameter TMPDIR set to xst\projnav.tmp Total REAL time to Xst completion: 0.00 secs Total CPU time to Xst completion: 0.37 secs --> Parameter xst\hdcidr set to xst Total REAL time to Xst completion: 0.00 secs Total CPU time to Xst completion: 0.37 secs --> TABLE OF CONTENTS 1) Synthesis Options Summary 2) HDL Parasit 3) HDL Elaboration 4) HDL Synthesis 4.1) HDL Synthesis Report 5) Advanced HDL Synthesis 5.1) Advanced HDL Synthesis Report 6) Low Level Synthesis 7) Partition Report 8) Design Summary 8.1) Primitive and Black Box Usage 8.2) Device utilization summary 8.3) Partition Resource Summary 8.4) Timing Report 8.4.1) Clock Information 8.4.2) Asynchronous Control Signals Information 8.4.3) Timing Summary 8.4.4) Timing Details 8.4.5) Cross Clock Domains Report Synthesis Options Summary --- Source Parameters Input File Name : "cla_add n bit.prj" Ignore Synthesis Constraint File : NO --- Target Parameters Output File Name : "cla_add n bit" Output Format : NGC Target Device : xc6slx14-3-tqg144 --- Source Options Top Module Name : cla_add n bit Automatic FSM Extraction : YES FSM Encoding Algorithm : Auto Sata Implementation : No FSM Style : LUT RAM Extraction : Yes ROM Style : Auto ROM Extraction : Yes Shift Register Extraction : YES RCM Style : Auto Resource Sharing : YES Asynchronous To Synchronous : NO Shift Register Minimum Size : 2 Use DSP Block : Auto Automatic Register Balancing : No --- Target Options LUT Combining : Auto Reduce Control Sats : Auto Add IO Buffers : YES </pre>
--	--

<pre> >rem ***** test cla adder @if not exist "%*" mkdir %* >cd XST >cd-if not exist "%projnav.tmp%" mkdir "%projnav.tmp%" >cd %* >rem ***** test cla operations >set -lh cla_add n_bit xst Release 14.7 - xst P 20131013 (n664) Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved. --> Parameter TMPDIR set to xst\projnav.tmp Total REAL time to Xst completion: 0.00 secs Total CPU time to Xst completion: 0.28 secs --> Parameter xsthdicdir set to xst Total REAL time to Xst completion: 0.00 secs Total CPU time to Xst completion: 0.28 secs --> TABLE OF CONTENTS 1) Synthesis Options Summary 2) HDL Parasit 3) HDL Elaboration 4) HDL Synthesis 4.1) HDL Synthesis Report 5) Advanced HDL Synthesis 5.1) Advanced HDL Synthesis Report 6) Low Level Synthesis 7) Partition Report 8) Design Summary 8.1) Primitive and Black Box Usage 8.2) Device utilization summary 8.3) Partition Resource Summary 8.4) Timing Report 8.4.1) Clock Information 8.4.2) Asynchronous Control Signals Information 8.4.3) Timing Summary 8.4.4) Timing Details 8.4.5) Cross Clock Domains Report Synthesis Options Summary --- Source Parameters Input File Name : "cla_add n_bit.prj" Ignore Synthesis Constraint File : NO --- Target Parameters Output File Name : "cla_add n_bit" Output Format : NCG Target Device : xc6slx4-3-tqg144 --- Source Options Top Module Name : cla_add n_bit Automatic FSM Extraction : YES FSM Encoding Algorithm : Auto Sata Implementation : No FSM Style : LUT RAM Extraction : Yes ROM Style : Auto ROM Extraction : Yes Shift Register Extraction : YES RCM Style : Auto Resource Sharing : YES Asynchronous To Synchronous : NO Shift Register Minimum Size : 2 Use DSP Block : Auto Automatic Register Balancing : No --- Target Options LUT Combining : Auto Reduce Control Sats : Auto Add IO Buffers : YES </pre>		<pre> >rem ***** test cla adder @if not exist "%*" mkdir %* >cd XST >cd-if not exist "%projnav.tmp%" mkdir "%projnav.tmp%" >cd %* >rem ***** test cla operations >set -lh cla_add n_bit xst Release 14.7 - xst P 20131013 (n664) Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved. --> Parameter TMPDIR set to xst\projnav.tmp Total REAL time to Xst completion: 0.00 secs Total CPU time to Xst completion: 0.37 secs --> Parameter xsthdicdir set to xst Total REAL time to Xst completion: 0.00 secs Total CPU time to Xst completion: 0.37 secs --> TABLE OF CONTENTS 1) Synthesis Options Summary 2) HDL Parasit 3) HDL Elaboration 4) HDL Synthesis 4.1) HDL Synthesis Report 5) Advanced HDL Synthesis 5.1) Advanced HDL Synthesis Report 6) Low Level Synthesis 7) Partition Report 8) Design Summary 8.1) Primitive and Black Box Usage 8.2) Device utilization summary 8.3) Partition Resource Summary 8.4) Timing Report 8.4.1) Clock Information 8.4.2) Asynchronous Control Signals Information 8.4.3) Timing Summary 8.4.4) Timing Details 8.4.5) Cross Clock Domains Report Synthesis Options Summary --- Source Parameters Input File Name : "cla_add n_bit.prj" Ignore Synthesis Constraint File : NO --- Target Parameters Output File Name : "cla_add n_bit" Output Format : NCG Target Device : xc6slx4-3-tqg144 --- Source Options Top Module Name : cla_add n_bit Automatic FSM Extraction : YES FSM Encoding Algorithm : Auto Sata Implementation : No FSM Style : LUT RAM Extraction : Yes ROM Style : Auto ROM Extraction : Yes Shift Register Extraction : YES RCM Style : Auto Resource Sharing : YES Asynchronous To Synchronous : NO Shift Register Minimum Size : 2 Use DSP Block : Auto Automatic Register Balancing : No --- Target Options LUT Combining : Auto Reduce Control Sats : Auto Add IO Buffers : YES </pre>	
---	--	---	--

>rem ***** test cla adder	>rem ***** test cla adder
>if not exist "xst" mkdir xst	>if not exist "xst" mkdir xst
>cd XST	>cd XST
set-if not exist "projnav.tmp" mkdir "projnav.tmp"	set-if not exist "projnav.tmp" mkdir "projnav.tmp"
set-cd	set-cd
>rem ***** test cla operations	>rem ***** test cla operations
>xst -fn cla add n bit xst	>xst -fn cla add n bit xst
Release 14.7 - xst P.20131013 (n64)	Release 14.7 - xst P.20131013 (n64)
Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.	Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.
--> Parameter TMPDIR set to xst/projnav.tmp	--> Parameter TMPDIR set to xst/projnav.tmp
Total REAL time to Xst completion: 1.00 secs	Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.29 secs	Total CPU time to Xst completion: 0.37 secs
--> Parameter xsthdpr set to xst	--> Parameter xsthdpr set to xst
Total REAL time to Xst completion: 1.00 secs	Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.30 secs	Total CPU time to Xst completion: 0.37 secs
-->	-->
TABLE OF CONTENTS	TABLE OF CONTENTS
1) Synthesis Options Summary	1) Synthesis Options Summary
2) HDL Parsing	2) HDL Parsing
3) HDL Elaboration	3) HDL Elaboration
4) HDL Synthesis	4) HDL Synthesis
4.1) HDL Synthesis Report	4.1) HDL Synthesis Report
5) Advanced HDL Synthesis	5) Advanced HDL Synthesis
5.1) Advanced HDL Synthesis Report	5.1) Advanced HDL Synthesis Report
6) Low Level Synthesis	6) Low Level Synthesis
7) Partition Report	7) Partition Report
8) Design Summary	8) Design Summary
8.1) Primitive and Black Box Usage	8.1) Primitive and Black Box Usage
8.2) Device utilization summary	8.2) Device utilization summary
8.3) Partition Resource Summary	8.3) Partition Resource Summary
8.4) Timing Report	8.4) Timing Report
8.4.1) Clock Information	8.4.1) Clock Information
8.4.2) Asynchronous Control Signals Information	8.4.2) Asynchronous Control Signals Information
8.4.3) Timing Summary	8.4.3) Timing Summary
8.4.4) Timing Details	8.4.4) Timing Details
8.4.5) Cross Clock Domains Report	8.4.5) Cross Clock Domains Report
Synthesis Options Summary	Synthesis Options Summary
----	----
Source Parameters	Source Parameters
Input File Name : "cla_add_n_bit.prj"	Input File Name : "cla_add_n_bit.prj"
Ignore Synthesis Constraint File : NO	Ignore Synthesis Constraint File : NO
-----	-----
Target Parameters	Target Parameters
Output File Name : "cla_add_n_bit"	Output File Name : "cla_add_n_bit"
Output Format : NGC	Output Format : NGC
Target Device : xc6slx4-3-tqp144	Target Device : xc6slx4-3-tqp144
-----	-----
Source Options	Source Options
Top Module Name : cla_add_n_bit	Top Module Name : cla_add_n_bit
Automatic FSM Extraction : YES	Automatic FSM Extraction : YES
FSM Encoding Algorithm : Auto	FSM Encoding Algorithm : Auto
Safe Implementation : No	Safe Implementation : No
FSM Style : LUT	FSM Style : LUT
RAM Extraction : Yes	RAM Extraction : Yes
RAM Style : Auto	RAM Style : Auto
ROM Extraction : Yes	ROM Extraction : Yes
Shift Register Extraction : YES	Shift Register Extraction : YES
ROM Style : Auto	ROM Style : Auto
Resource Sharing : YES	Resource Sharing : YES
Asynchronous To Synchronous : NO	Asynchronous To Synchronous : NO
Shift Register Minimum Size : 2	Shift Register Minimum Size : 2
Use DSP Block : Auto	Use DSP Block : Auto
Automatic Register Balancing : No	Automatic Register Balancing : No
-----	-----
Target Options	Target Options
LUT Combining : Auto	LUT Combining : Auto
Reduce Control Sets : Auto	Reduce Control Sets : Auto
Add IO Buffers : YES	Add IO Buffers : YES

<pre> >run ***** test cla adder if not exist "%x%" mkdir %x% >cd XST >cd-if not exist "%projnav.tmp%" mkdir "%projnav.tmp%" >cd %x% >run ***** test cla operations >set -lh cla_add n_bit xst Release 14.7 - xst P 20131013 (n664) Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved. --> Parameter TMPDIR set to xst\projnav.tmp Total REAL time to Xst completion: 0.00 secs Total CPU time to Xst completion: 0.24 secs --> Parameter xst\hdcidr set to xst Total REAL time to Xst completion: 0.00 secs Total CPU time to Xst completion: 0.25 secs --> TABLE OF CONTENTS 1) Synthesis Options Summary 2) HDL Parasit 3) HDL Elaboration 4) HDL Synthesis 4.1) HDL Synthesis Report 5) Advanced HDL Synthesis 5.1) Advanced HDL Synthesis Report 6) Low Level Synthesis 7) Partition Report 8) Design Summary 8.1) Primitive and Black Box Usage 8.2) Device utilization summary 8.3) Partition Resource Summary 8.4) Timing Report 8.4.1) Clock Information 8.4.2) Asynchronous Control Signals Information 8.4.3) Timing Summary 8.4.4) Timing Details 8.4.5) Cross Clock Domains Report Synthesis Options Summary --- Source Parameters Input File Name : "cla_add n_bit.prj" Ignore Synthesis Constraint File : NO --- Target Parameters Output File Name : "cla_add n_bit" Output Format : NGC Target Device : xc6slx14-3-tqg144 --- Source Options Top Module Name : cla_add n_bit Automatic FSM Extraction : YES FSM Encoding Algorithm : Auto Sata Implementation : No FSM Style : LUT RAM Extraction : Yes ROM Style : Auto ROM Extraction : Yes Shift Register Extraction : YES RCM Style : Auto Resource Sharing : YES Asynchronous To Synchronous : NO Shift Register Minimum Size : 2 Use DSP Block : Auto Automatic Register Balancing : No --- Target Options LUT Combining : Auto Reduce Control Sels : Auto Add IO Buffers : YES </pre>		<pre> >run ***** test cla adder if not exist "%x%" mkdir %x% >cd XST >cd-if not exist "%projnav.tmp%" mkdir "%projnav.tmp%" >cd %x% >run ***** test cla operations >set -lh cla_add n_bit xst Release 14.7 - xst P 20131013 (n664) Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved. --> Parameter TMPDIR set to xst\projnav.tmp Total REAL time to Xst completion: 0.00 secs Total CPU time to Xst completion: 0.37 secs --> Parameter xst\hdcidr set to xst Total REAL time to Xst completion: 0.00 secs Total CPU time to Xst completion: 0.37 secs --> TABLE OF CONTENTS 1) Synthesis Options Summary 2) HDL Parasit 3) HDL Elaboration 4) HDL Synthesis 4.1) HDL Synthesis Report 5) Advanced HDL Synthesis 5.1) Advanced HDL Synthesis Report 6) Low Level Synthesis 7) Partition Report 8) Design Summary 8.1) Primitive and Black Box Usage 8.2) Device utilization summary 8.3) Partition Resource Summary 8.4) Timing Report 8.4.1) Clock Information 8.4.2) Asynchronous Control Signals Information 8.4.3) Timing Summary 8.4.4) Timing Details 8.4.5) Cross Clock Domains Report Synthesis Options Summary --- Source Parameters Input File Name : "cla_add n_bit.prj" Ignore Synthesis Constraint File : NO --- Target Parameters Output File Name : "cla_add n_bit" Output Format : NGC Target Device : xc6slx14-3-tqg144 --- Source Options Top Module Name : cla_add n_bit Automatic FSM Extraction : YES FSM Encoding Algorithm : Auto Sata Implementation : No FSM Style : LUT RAM Extraction : Yes ROM Style : Auto ROM Extraction : Yes Shift Register Extraction : YES RCM Style : Auto Resource Sharing : YES Asynchronous To Synchronous : NO Shift Register Minimum Size : 2 Use DSP Block : Auto Automatic Register Balancing : No --- Target Options LUT Combining : Auto Reduce Control Sels : Auto Add IO Buffers : YES </pre>	
--	--	--	--

<pre> >rem ***** test cla adder @if not exist "%x%" mkdir %x% >cd %XST% >cd %if not exist "prognav.tmp" mkdir "prognav.tmp" >cd %x% >rem ***** test cla operations >set -fh cla_add n_bit xst Release 14.7 - xst P 20131013 (n664) Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved. --> Parameter TMPDIR set to xst/prognav.tmp Total REAL time to Xst completion: 1.00 secs Total CPU time to Xst completion: 0.39 secs --> Parameter xsthdicdir set to xst Total REAL time to Xst completion: 1.00 secs Total CPU time to Xst completion: 0.39 secs --> TABLE OF CONTENTS 1) Synthesis Options Summary 2) HDL Parasit 3) HDL Elaboration 4) HDL Synthesis 4.1) HDL Synthesis Report 5) Advanced HDL Synthesis 5.1) Advanced HDL Synthesis Report 6) Low Level Synthesis 7) Partition Report 8) Design Summary 8.1) Primitive and Black Box Usage 8.2) Device utilization summary 8.3) Partition Resource Summary 8.4) Timing Report 8.4.1) Clock Information 8.4.2) Asynchronous Control Signals Information 8.4.3) Timing Summary 8.4.4) Timing Details 8.4.5) Cross Clock Domains Report Synthesis Options Summary --- Source Parameters Input File Name : "cla_add n_bit.prj" Ignore Synthesis Constraint File : NO --- Target Parameters Output File Name : "cla_add n_bit" Output Format : NGC Target Device : xc6slx4-3-tqg144 --- Source Options Top Module Name : cla_add n_bit Automatic FSM Extraction : YES FSM Encoding Algorithm : Auto Sata Implementation : No FSM Style : LUT RAM Extraction : Yes ROM Extraction : Yes Shift Register Extraction : YES RCM Style : Auto Resource Sharing : YES Asynchronous To Synchronous : NO Shift Register Minimum Size : 2 Use DSP Block : Auto Automatic Register Balancing : No --- Target Options LUT Combining : Auto Reduce Control Sats : Auto Add IO Buffers : YES </pre>		<pre> >rem ***** test cla adder @if not exist "%x%" mkdir %x% >cd %XST% >cd %if not exist "prognav.tmp" mkdir "prognav.tmp" >cd %x% >rem ***** test cla operations >set -fh cla_add n_bit xst Release 14.7 - xst P 20131013 (n664) Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved. --> Parameter TMPDIR set to xst/prognav.tmp Total REAL time to Xst completion: 0.00 secs Total CPU time to Xst completion: 0.37 secs --> Parameter xsthdicdir set to xst Total REAL time to Xst completion: 0.00 secs Total CPU time to Xst completion: 0.37 secs --> TABLE OF CONTENTS 1) Synthesis Options Summary 2) HDL Parasit 3) HDL Elaboration 4) HDL Synthesis 4.1) HDL Synthesis Report 5) Advanced HDL Synthesis 5.1) Advanced HDL Synthesis Report 6) Low Level Synthesis 7) Partition Report 8) Design Summary 8.1) Primitive and Black Box Usage 8.2) Device utilization summary 8.3) Partition Resource Summary 8.4) Timing Report 8.4.1) Clock Information 8.4.2) Asynchronous Control Signals Information 8.4.3) Timing Summary 8.4.4) Timing Details 8.4.5) Cross Clock Domains Report Synthesis Options Summary --- Source Parameters Input File Name : "cla_add n_bit.prj" Ignore Synthesis Constraint File : NO --- Target Parameters Output File Name : "cla_add n_bit" Output Format : NGC Target Device : xc6slx4-3-tqg144 --- Source Options Top Module Name : cla_add n_bit Automatic FSM Extraction : YES FSM Encoding Algorithm : Auto Sata Implementation : No FSM Style : LUT RAM Extraction : Yes ROM Extraction : Yes Shift Register Extraction : YES RCM Style : Auto Resource Sharing : YES Asynchronous To Synchronous : NO Shift Register Minimum Size : 2 Use DSP Block : Auto Automatic Register Balancing : No --- Target Options LUT Combining : Auto Reduce Control Sats : Auto Add IO Buffers : YES </pre>	
--	--	--	--

```

>rem ***** test cla adder
>if not exist "xst" mkdir xst
>cd XST
\xst>if not exist "projnav.tmp" mkdir "projnav.tmp"
\xst>cd ..
>rem ***** test cla operations
>xst -ifn cla_add_n_bit.xst
Release 14.7 - xst P.20131013 (nt64)
Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.
--> Parameter TMPDIR set to xst/projnav.tmp
Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.37 secs

```

```

--> Parameter xsthdpdir set to xst
Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.37 secs

```

-->

TABLE OF CONTENTS

- 1) Synthesis Options Summary
- 2) HDL Parsing
- 3) HDL Elaboration
- 4) HDL Synthesis
 - 4.1) HDL Synthesis Report
- 5) Advanced HDL Synthesis
 - 5.1) Advanced HDL Synthesis Report
- 6) Low Level Synthesis
- 7) Partition Report
- 8) Design Summary
 - 8.1) Primitive and Black Box Usage
 - 8.2) Device utilization summary
 - 8.3) Partition Resource Summary
 - 8.4) Timing Report
 - 8.4.1) Clock Information
 - 8.4.2) Asynchronous Control Signals Information
 - 8.4.3) Timing Summary
 - 8.4.4) Timing Details
 - 8.4.5) Cross Clock Domains Report

* Synthesis Options Summary *

---- Source Parameters

```

Input File Name           : "cla_add_n_bit.prj"
Ignore Synthesis Constraint File : NO

```

---- Target Parameters

```

Output File Name          : "cla_add_n_bit"
Output Format              : NGC
Target Device              : xc6slx4-3-tqg144

```

---- Source Options

```

Top Module Name           : cla_add_n_bit
Automatic FSM Extraction   : YES
FSM Encoding Algorithm     : Auto
Safe Implementation       : No
FSM Style                 : LUT
RAM Extraction             : Yes
RAM Style                 : Auto
ROM Extraction            : Yes
Shift Register Extraction  : YES
ROM Style                 : Auto
Resource Sharing          : YES

```

```

Asynchronous To Synchronous      : NO
Shift Register Minimum Size      : 2
Use DSP Block                     : Auto
Automatic Register Balancing     : No
---- Target Options
LUT Combining                     : Auto
Reduce Control Sets              : Auto
Add IO Buffers                   : YES
Global Maximum Fanout            : 100000
Add Generic Clock Buffer(BUFG)   : 16
Register Duplication             : YES
Optimize Instantiated Primitives : NO
Use Clock Enable                 : Auto
Use Synchronous Set              : Auto
Use Synchronous Reset            : Auto
Pack IO Registers into IOBs      : Auto
Equivalent register Removal      : YES
---- General Options
Optimization Goal                 : Speed
Optimization Effort               : 1
Power Reduction                  : NO
Keep Hierarchy                   : No
Netlist Hierarchy                : As_Optimized
RTL Output                       : Yes
Global Optimization              : AllClockNets
Read Cores                       : YES
Write Timing Constraints          : NO
Cross Clock Analysis             : NO
Hierarchy Separator              : /
Bus Delimiter                    : <>
Case Specifier                   : Maintain
Slice Utilization Ratio          : 100
BRAM Utilization Ratio           : 100
DSP48 Utilization Ratio          : 100
Auto BRAM Packing                : NO
Slice Utilization Ratio Delta    : 5
*                               *
*                               *
HDL Parsing
Parsing VHDL file "\cla_gp.vhd" into library work
Parsing entity <cla_gp>.
Parsing architecture <> of entity <cla_gp>.
Parsing VHDL file "\cla_add_n_bit.vhd" into library work
Parsing entity <cla_add_n_bit>.
Parsing architecture <> of entity <cla_add_n_bit>.
*                               *
*                               *
HDL Elaboration
Elaborating entity <cla_add_n_bit> (architecture <>) with generics from library <work>.
*                               *
*                               *
HDL Synthesis
Synthesizing Unit <cla_add_n_bit>.
  Related source file is "\cla_add_n_bit.vhd".
    n = 8
  Summary:
Unit <cla_add_n_bit> synthesized.
HDL Synthesis Report
Macro Statistics
# Xors                          : 16
  1-bit xor2                    : 16
*                               *
*                               *
Advanced HDL Synthesis
Advanced HDL Synthesis Report
Macro Statistics
# Xors                          : 16

```

1-bit xor2 : 16
* Low Level Synthesis *
Optimizing unit <cla_add_n_bit> ...
Mapping all equations...
Building and optimizing final netlist ...
Found area constraint ratio of 100 (+ 5) on block cla_add_n_bit, actual ratio is 1.
Final Macro Processing ...
Final Register Report
Found no macro

* Partition Report *
Partition Implementation Status

No Partitions were found in this design.

* Design Summary *
Top Level Output File Name : cla_add_n_bit.ngc
Primitive and Black Box Usage:

BELS : 24
LUT2 : 6
LUT3 : 3
LUT5 : 6
LUT6 : 9
IO Buffers : 28
IBUF : 17
OBUF : 11

Device utilization summary:

Selected Device : 6slx4tqg144-3

Slice Logic Utilization:

Number of Slice LUTs: 24 out of 2400 1%
Number used as Logic: 24 out of 2400 1%

Slice Logic Distribution:

Number of LUT Flip Flop pairs used: 24
Number with an unused Flip Flop: 24 out of 24 100%
Number with an unused LUT: 0 out of 24 0%
Number of fully used LUT-FF pairs: 0 out of 24 0%
Number of unique control sets: 0

IO Utilization:

Number of IOs: 28
Number of bonded IOBs: 28 out of 102 27%

Specific Feature Utilization:

Partition Resource Summary:

No Partitions were found in this design.

Timing Report

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.

FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT
GENERATED AFTER PLACE-and-ROUTE.

Clock Information:

No clock signals found in this design

Asynchronous Control Signals Information:

No asynchronous control signals found in this design

Timing Summary:

Speed Grade: -3

Minimum period: No path found

Minimum input arrival time before clock: No path found

Maximum output required time after clock: No path found

Maximum combinational path delay: 9.101ns

Timing Details:

All values displayed in nanoseconds (ns)

Timing constraint: Default path analysis

Total number of paths / destination ports: 131 / 11

Delay: 9.101ns (Levels of Logic = 7)

Source: Y<0> (PAD)

Destination: S<7> (PAD)

Data Path: Y<0> to S<7>

	Gate	Net			
Cell:in->out	fanout	Delay	Delay	Logical Name (Net Name)	

IBUF:I->O	6	1.222	0.973	Y_0_IBUF (Y_0_IBUF)	
LUT3:I0->O	2	0.205	0.617	Cint_xtd<3>_SW0 (N2)	
LUT5:I4->O	3	0.205	0.651	Cint_xtd<3> (Cint_xtd<3>)	
LUT3:I2->O	2	0.205	0.617	Cint_xtd<6>_SW0 (N4)	
LUT5:I4->O	2	0.205	0.845	Cint_xtd<6> (Cint_xtd<6>)	
LUT5:I2->O	1	0.205	0.579	Mxor_S<7>_xo<0>1 (S_7_OBUF)	
OBUF:I->O		2.571		S_7_OBUF (S<7>)	

Total 9.101ns (4.818ns logic, 4.283ns route)
(52.9% logic, 47.1% route)

Cross Clock Domains Report:

Total REAL time to Xst completion: 9.00 secs

Total CPU time to Xst completion: 9.37 secs

-->

Total memory usage is 4487500 kilobytes

Number of errors : 0 (0 filtered)

Number of warnings : 0 (0 filtered)

Number of infos : 0 (0 filtered)

>fuse -incremental -o cla_add_n_bit_tb_isim_beh.exe -prj cla_add_n_bit_tb.prj -top cla_add_n_bit_tb

ISim P.20131013 (signature 0x7708f090)

Number of CPUs detected in this system: 8

Turning on mult-threading, number of parallel sub-compilation jobs: 16

Determining compilation order of HDL files

Parsing VHDL file "cla_gp.vhd" into library work

Parsing VHDL file "cla_add_n_bit.vhd" into library work

Parsing VHDL file "cla_add_n_bit_tb.vhd" into library work

Starting static elaboration

Completed static elaboration

Compiling package standard

Compiling package std_logic_1164

Compiling package textio

Compiling package std_logic_textio

Compiling package numeric_std

Compiling package attributes

Compiling package std_logic_misc

Compiling architecture of entity cla_add_n_bit [\\cla_add_n_bit(8)]

Compiling architecture testbench_arch of entity cla_add_n_bit_tb

Time Resolution for simulation is 1ps.

Compiled 10 VHDL Units

```

Built simulation executable cla_add_n_bit_tb_isim_beh.exe
Fuse Memory Usage: 37436 KB
Fuse CPU Usage: 906 ms
>cla_add_n_bit_tb_isim_beh.exe -tclbatch isim.tcl -wdb cla_add_n_bit_tb_isim_beh.wdb
ISim P.20131013 (signature 0x7708f090)
WARNING: A WEBPACK license was found.
WARNING: Please use Xilinx License Configuration Manager to check out a full ISim license.
WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for more information on t
This is a Lite version of ISim.
Time resolution is 1 ps
Simulator is doing circuit initialization process.
Finished circuit initialization process.
>rem ***** test cla flags
>xst -ifn cla_add_n_bit_flags.xst
Release 14.7 - xst P.20131013 (nt64)
Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.
--> Parameter TMPDIR set to xst/projnav.tmp
Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.24 secs

--> Parameter xsthdpdir set to xst
Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.25 secs

--> ERROR:Xst:438 - Can not open file : cla_add_n_bit_flags.prj
Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.27 secs

-->
Total memory usage is 4422880 kilobytes
Number of errors : 1 ( 0 filtered)
Number of warnings : 0 ( 0 filtered)
Number of infos : 0 ( 0 filtered)
>fuse -incremental -o cla_add_n_bit_tb_flags_isim_beh.exe -prj cla_add_n_bit_flags_tb.prj -top cla_ad
ISim P.20131013 (signature 0x7708f090)
Number of CPUs detected in this system: 8
Turning on mult-threading, number of parallel sub-compilation jobs: 16
Determining compilation order of HDL files
Parsing VHDL file "cla_gp.vhd" into library work
Parsing VHDL file "cla_add_n_bit.vhd" into library work
Parsing VHDL file "cla_add_n_bit_flags_tb.vhd" into library work
Starting static elaboration
Completed static elaboration
Compiling package standard
Compiling package std_logic_1164
Compiling package textio
Compiling package std_logic_textio
Compiling package numeric_std
Compiling package attributes
Compiling package std_logic_misc
Compiling architecture of entity cla_add_n_bit [\cla_add_n_bit(8)]
Compiling architecture a1 of entity cla_add_n_bit_flags_tb_
Time Resolution for simulation is 1ps.
Waiting for 1 sub-compilation(s) to finish...
Compiled 10 VHDL Units
Built simulation executable cla_add_n_bit_tb_flags_isim_beh.exe
Fuse Memory Usage: 37528 KB
Fuse CPU Usage: 937 ms
>cla_add_n_bit_tb_flags_isim_beh.exe -tclbatch isim.tcl -wdb cla_add_n_bit_flags_tb.wdb

```

ISim P.20131013 (signature 0x7708f090)
WARNING: A WEBPACK license was found.
WARNING: Please use Xilinx License Configuration Manager to check out a full ISim license.
WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for more information on t
This is a Lite version of ISim.

Time resolution is 1 ps

Simulator is doing circuit initialization process.

Finished circuit initialization process.

>rem ***** test alu operations

>xst -ifn alu_cla.xst

Release 14.7 - xst P.20131013 (nt64)

Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.

--> Parameter TMPDIR set to xst/projnav.tmp

Total REAL time to Xst completion: 0.00 secs

Total CPU time to Xst completion: 0.24 secs

--> Parameter xsthdpdir set to xst

Total REAL time to Xst completion: 0.00 secs

Total CPU time to Xst completion: 0.25 secs

-->

TABLE OF CONTENTS

- 1) Synthesis Options Summary
- 2) HDL Parsing
- 3) HDL Elaboration
- 4) HDL Synthesis
 - 4.1) HDL Synthesis Report
- 5) Advanced HDL Synthesis
 - 5.1) Advanced HDL Synthesis Report
- 6) Low Level Synthesis
- 7) Partition Report
- 8) Design Summary
 - 8.1) Primitive and Black Box Usage
 - 8.2) Device utilization summary
 - 8.3) Partition Resource Summary
 - 8.4) Timing Report
 - 8.4.1) Clock Information
 - 8.4.2) Asynchronous Control Signals Information
 - 8.4.3) Timing Summary
 - 8.4.4) Timing Details
 - 8.4.5) Cross Clock Domains Report

* Synthesis Options Summary *

---- Source Parameters

Input File Name : "alu_cla.prj"

Ignore Synthesis Constraint File : NO

---- Target Parameters

Output File Name : "alu_cla"

Output Format : NGC

Target Device : xc6slx4-3-tqg144

---- Source Options

Top Module Name : alu_cla

Automatic FSM Extraction : YES

FSM Encoding Algorithm : Auto

Safe Implementation : No

FSM Style : LUT

RAM Extraction : Yes

RAM Style : Auto

ROM Extraction : Yes

Shift Register Extraction : YES

ROM Style : Auto
Resource Sharing : YES
Asynchronous To Synchronous : NO
Shift Register Minimum Size : 2
Use DSP Block : Auto
Automatic Register Balancing : No

---- Target Options

LUT Combining : Auto
Reduce Control Sets : Auto
Add IO Buffers : YES
Global Maximum Fanout : 100000
Add Generic Clock Buffer(BUFG) : 16
Register Duplication : YES
Optimize Instantiated Primitives : NO
Use Clock Enable : Auto
Use Synchronous Set : Auto
Use Synchronous Reset : Auto
Pack IO Registers into IOBs : Auto
Equivalent register Removal : YES

---- General Options

Optimization Goal : Speed
Optimization Effort : 1
Power Reduction : NO
Keep Hierarchy : No
Netlist Hierarchy : As_Optimized
RTL Output : Yes
Global Optimization : AllClockNets
Read Cores : YES
Write Timing Constraints : NO
Cross Clock Analysis : NO
Hierarchy Separator : /
Bus Delimiter : <>
Case Specifier : Maintain
Slice Utilization Ratio : 100
BRAM Utilization Ratio : 100
DSP48 Utilization Ratio : 100
Auto BRAM Packing : NO
Slice Utilization Ratio Delta : 5

* HDL Parsing *

Parsing VHDL file "cla_gp.vhd" into library work

Parsing entity <cla_gp>.

Parsing architecture <> of entity <cla_gp>.

Parsing VHDL file "cla_add_n_bit.vhd" into library work

Parsing entity <cla_add_n_bit>.

Parsing architecture <> of entity <cla_add_n_bit>.

Parsing VHDL file "alu_cla.vhd" into library work

Parsing entity <alu_cla>.

Parsing architecture <> of entity <alu_cla>.

* HDL Elaboration *

Elaborating entity <alu_cla> (architecture <>) with generics from library <work>.

Elaborating entity <cla_add_n_bit> (architecture <>) with generics from library <work>.

* HDL Synthesis *

Synthesizing Unit <alu_cla>.

Related source file is "alu_cla.vhd".

n = 8

Found 8-bit 12-to-1 multiplexer for signal <S> created at line 103.

Summary:

inferred 28 Multiplexer(s).

Unit <alu_cla> synthesized.

Synthesizing Unit <cla_add_n_bit>.

Related source file is "\cla_add_n_bit.vhd".

n = 8

Summary:

Unit <cla_add_n_bit> synthesized.

HDL Synthesis Report

Macro Statistics

# Multiplexers	: 28
1-bit 2-to-1 multiplexer	: 21
8-bit 12-to-1 multiplexer	: 1
8-bit 2-to-1 multiplexer	: 6
# Xors	: 17
1-bit xor2	: 16
8-bit xor2	: 1

* Advanced HDL Synthesis *

Advanced HDL Synthesis Report

Macro Statistics

# Multiplexers	: 28
1-bit 2-to-1 multiplexer	: 21
8-bit 12-to-1 multiplexer	: 1
8-bit 2-to-1 multiplexer	: 6
# Xors	: 17
1-bit xor2	: 16
8-bit xor2	: 1

* Low Level Synthesis *

Optimizing unit <alu_cla> ...

Optimizing unit <cla_add_n_bit> ...

Mapping all equations...

Building and optimizing final netlist ...

Found area constraint ratio of 100 (+ 5) on block alu_cla, actual ratio is 4.

Final Macro Processing ...

Final Register Report

Found no macro

* Partition Report *

Partition Implementation Status

No Partitions were found in this design.

* Design Summary *

Top Level Output File Name : alu_cla.ngc

Primitive and Black Box Usage:

BELS : 62
LUT3 : 4
LUT5 : 13
LUT6 : 43
MUXF7 : 2
IO Buffers : 34
IBUF : 20
OBUF : 14

Device utilization summary:

Selected Device : 6slx4tqg144-3

Slice Logic Utilization:

Number of Slice LUTs:	60	out of	2400	2%
Number used as Logic:	60	out of	2400	2%

Slice Logic Distribution:

Number of LUT Flip Flop pairs used:	60
Number with an unused Flip Flop:	60 out of 60 100%

Number with an unused LUT: 0 out of 60 0%
Number of fully used LUT-FF pairs: 0 out of 60 0%
Number of unique control sets: 0

IO Utilization:

Number of IOs: 34
Number of bonded IOBs: 34 out of 102 33%

Specific Feature Utilization:

Partition Resource Summary:

No Partitions were found in this design.

Timing Report

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.

FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT
GENERATED AFTER PLACE-and-ROUTE.

Clock Information:

No clock signals found in this design

Asynchronous Control Signals Information:

No asynchronous control signals found in this design

Timing Summary:

Speed Grade: -3

Minimum period: No path found
Minimum input arrival time before clock: No path found
Maximum output required time after clock: No path found
Maximum combinational path delay: 11.243ns

Timing Details:

All values displayed in nanoseconds (ns)

Timing constraint: Default path analysis

Total number of paths / destination ports: 1252 / 14

Delay: 11.243ns (Levels of Logic = 9)

Source: F<2> (PAD)

Destination: Overflow (PAD)

Data Path: F<2> to Overflow

		Gate	Net		
Cell:in->out	fanout	Delay	Delay	Logical Name (Net Name)	
IBUF:I->O	37	1.222	1.707	F_2_IBUF (F_2_IBUF)	
LUT6:I1->O	6	0.203	0.973	Mmux_Y_sig31 (Y_sig<1>)	
LUT5:I2->O	4	0.205	1.028	U1/Cint_xtd<3>2 (U1/Cint_xtd<3>)	
LUT6:I1->O	1	0.203	0.000	U1/Cint_xtd<6>_G (N23)	
MUXF7:I1->O	4	0.140	0.912	U1/Cint_xtd<6> (U1/Cint_xtd<6>)	
LUT5:I2->O	5	0.205	0.962	U1/Mxor_S<7>_xo<0>1 (Sum_sig<7>)	
LUT6:I2->O	1	0.203	0.000	Mmux_Overflow2_F (N24)	
MUXF7:I0->O	1	0.131	0.579	Mmux_Overflow2 (Overflow_OBUF)	
OBUF:I->O		2.571		Overflow_OBUF (Overflow)	

Total 11.243ns (5.083ns logic, 6.160ns route)
(45.2% logic, 54.8% route)

Cross Clock Domains Report:

Total REAL time to Xst completion: 9.00 secs
Total CPU time to Xst completion: 8.99 secs

```

-->
Total memory usage is 4487500 kilobytes
Number of errors : 0 ( 0 filtered)
Number of warnings : 0 ( 0 filtered)
Number of infos : 0 ( 0 filtered)
>fuse -incremental -o alu_cla_tb_isim_beh.exe -prj alu_cla_tb.prj -top alu_cla_tb
ISim P.20131013 (signature 0x7708f090)
Number of CPUs detected in this system: 8
Turning on mult-threading, number of parallel sub-compilation jobs: 16
Determining compilation order of HDL files
Parsing VHDL file "cla_gp.vhd" into library work
Parsing VHDL file "cla_add_n_bit.vhd" into library work
Parsing VHDL file "alu_cla.vhd" into library work
Parsing VHDL file "alu_cla_tb.vhd" into library work
Starting static elaboration
Completed static elaboration
Compiling package standard
Compiling package std_logic_1164
Compiling package textio
Compiling package std_logic_textio
Compiling package numeric_std
Compiling package attributes
Compiling package std_logic_misc
Compiling architecture of entity cla_add_n_bit [cla_add_n_bit(8)]
Compiling architecture of entity alu_cla [alu_cla(8)]
Compiling architecture testbench_arch of entity alu_cla_tb
Time Resolution for simulation is 1ps.
Waiting for 1 sub-compilation(s) to finish...
Compiled 12 VHDL Units
Built simulation executable alu_cla_tb_isim_beh.exe
Fuse Memory Usage: 37672 KB
Fuse CPU Usage: 968 ms
>alu_cla_tb_isim_beh.exe -tclbatch isim.tcl -wdb alu_cla_tb_isim_beh.wdb
ISim P.20131013 (signature 0x7708f090)
WARNING: A WEBPACK license was found.
WARNING: Please use Xilinx License Configuration Manager to check out a full ISim license.
WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for more information on t
This is a Lite version of ISim.
Time resolution is 1 ps
Simulator is doing circuit initialization process.
Finished circuit initialization process.
at 7864320 ns, Instance /alu_cla_tb/: Warning: NUMERIC_STD.TO_UNSIGNED: vector truncated
at 8847360 ns, Instance /alu_cla_tb/: Warning: NUMERIC_STD.TO_UNSIGNED: vector truncated
at 9830400 ns, Instance /alu_cla_tb/: Warning: NUMERIC_STD.TO_UNSIGNED: vector truncated
at 10813440 ns, Instance /alu_cla_tb/: Warning: NUMERIC_STD.TO_UNSIGNED: vector truncated
at 11796480 ns, Instance /alu_cla_tb/: Warning: NUMERIC_STD.TO_UNSIGNED: vector truncated
at 12779520 ns, Instance /alu_cla_tb/: Warning: NUMERIC_STD.TO_UNSIGNED: vector truncated
at 13762560 ns, Instance /alu_cla_tb/: Warning: NUMERIC_STD.TO_UNSIGNED: vector truncated
at 14745600 ns, Instance /alu_cla_tb/: Warning: NUMERIC_STD.TO_UNSIGNED: vector truncated
>rem ***** test alu flags
>xst -ifn alu_cla_flags.xst
Release 14.7 - xst P.20131013 (nt64)
Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.
--> Parameter TMPDIR set to xst/projnav.tmp
Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.23 secs

--> Parameter xsthdpdir set to xst
Total REAL time to Xst completion: 0.00 secs

```

Total CPU time to Xst completion: 0.23 secs

-->

TABLE OF CONTENTS

- 1) Synthesis Options Summary
- 2) HDL Parsing
- 3) HDL Elaboration
- 4) HDL Synthesis
 - 4.1) HDL Synthesis Report
- 5) Advanced HDL Synthesis
 - 5.1) Advanced HDL Synthesis Report
- 6) Low Level Synthesis
- 7) Partition Report
- 8) Design Summary
 - 8.1) Primitive and Black Box Usage
 - 8.2) Device utilization summary
 - 8.3) Partition Resource Summary
 - 8.4) Timing Report
 - 8.4.1) Clock Information
 - 8.4.2) Asynchronous Control Signals Information
 - 8.4.3) Timing Summary
 - 8.4.4) Timing Details
 - 8.4.5) Cross Clock Domains Report

* Synthesis Options Summary *

---- Source Parameters

Input File Name : "alu_cla_flags_tb.prj"

Ignore Synthesis Constraint File : NO

---- Target Parameters

Output File Name : "alu_cla_flags_tb"

Output Format : NGC

Target Device : xc6slx4-3-tqg144

---- Source Options

Top Module Name : alu_cla_flags_tb

Automatic FSM Extraction : YES

FSM Encoding Algorithm : Auto

Safe Implementation : No

FSM Style : LUT

RAM Extraction : Yes

RAM Style : Auto

ROM Extraction : Yes

Shift Register Extraction : YES

ROM Style : Auto

Resource Sharing : YES

Asynchronous To Synchronous : NO

Shift Register Minimum Size : 2

Use DSP Block : Auto

Automatic Register Balancing : No

---- Target Options

LUT Combining : Auto

Reduce Control Sets : Auto

Add IO Buffers : YES

Global Maximum Fanout : 100000

Add Generic Clock Buffer(BUFG) : 16

Register Duplication : YES

Optimize Instantiated Primitives : NO

Use Clock Enable : Auto

Use Synchronous Set : Auto

Use Synchronous Reset : Auto

Pack IO Registers into IOBs : Auto

Equivalent register Removal : YES

---- General Options

Optimization Goal : Speed
Optimization Effort : 1
Power Reduction : NO
Keep Hierarchy : No
Netlist Hierarchy : As_Optimized
RTL Output : Yes
Global Optimization : AllClockNets
Read Cores : YES
Write Timing Constraints : NO
Cross Clock Analysis : NO
Hierarchy Separator : /
Bus Delimiter : <>
Case Specifier : Maintain
Slice Utilization Ratio : 100
BRAM Utilization Ratio : 100
DSP48 Utilization Ratio : 100
Auto BRAM Packing : NO
Slice Utilization Ratio Delta : 5

* HDL Parsing *

Parsing VHDL file "cla_gp.vhd" into library work

Parsing entity <cla_gp>.

Parsing architecture <> of entity <cla_gp>.

Parsing VHDL file "cla_add_n_bit.vhd" into library work

Parsing entity <cla_add_n_bit>.

Parsing architecture <> of entity <cla_add_n_bit>.

Parsing VHDL file "alu_cla.vhd" into library work

Parsing entity <alu_cla>.

Parsing architecture <> of entity <alu_cla>.

Parsing VHDL file "alu_cla_tb_FLAGS_.vhd" into library work

Parsing entity <alu_cla_flags_tb>.

Parsing architecture <test_alu_flags> of entity <alu_cla_flags_tb>.

* HDL Elaboration *

Elaborating entity <alu_cla_flags_tb> (architecture <test_alu_flags>) with generics from library <work>.

Elaborating entity <alu_cla> (architecture <>) with generics from library <work>.

Elaborating entity <cla_add_n_bit> (architecture <>) with generics from library <work>.

ERROR:HDLCompiler:890 - "alu_cla_tb_FLAGS_.vhd" Line 144: wait statement without UNTIL clause

Netlist alu_cla_flags_tb(8)(test_alu_flags) remains a blackbox, due to errors in its contents

-->

Total memory usage is 4466680 kilobytes

Number of errors : 1 (0 filtered)

Number of warnings : 0 (0 filtered)

Number of infos : 0 (0 filtered)

>fuse -incremental -o alu_cla_flags_tb_isim_beh.exe -prj alu_cla_flags_tb.prj -top alu_cla_flags_tb

ISim P.20131013 (signature 0x7708f090)

Number of CPUs detected in this system: 8

Turning on mult-threading, number of parallel sub-compilation jobs: 16

Determining compilation order of HDL files

Parsing VHDL file "cla_gp.vhd" into library work

Parsing VHDL file "cla_add_n_bit.vhd" into library work

Parsing VHDL file "alu_cla.vhd" into library work

Parsing VHDL file "alu_cla_tb_FLAGS_.vhd" into library work

Starting static elaboration

Completed static elaboration

Compiling package standard

Compiling package std_logic_1164

Compiling package textio

Compiling package std_logic_textio

Compiling package numeric_std
Compiling package attributes
Compiling package std_logic_misc
Compiling architecture of entity cla_add_n_bit [\cla_add_n_bit(8)\]
Compiling architecture of entity alu_cla [\alu_cla(8)\]
Compiling architecture test_alu_flags of entity alu_cla_flags_tb
Time Resolution for simulation is 1ps.
Waiting for 1 sub-compilation(s) to finish...
Compiled 12 VHDL Units
Built simulation executable alu_cla_flags_tb_isim_beh.exe
Fuse Memory Usage: 37632 KB
Fuse CPU Usage: 906 ms
>alu_cla_flags_tb_isim_beh.exe -tclbatch isim.tcl -wdb alu_cla_flags_tb_isim_beh.wdb
ISim P.20131013 (signature 0x7708f090)
WARNING: A WEBPACK license was found.
WARNING: Please use Xilinx License Configuration Manager to check out a full ISim license.
WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for more information on t
This is a Lite version of ISim.
Time resolution is 1 ps
Simulator is doing circuit initialization process.
Finished circuit initialization process.

.he differences between the Lite and the Full version.

d_n_bit_flags_tb_

.he differences between the Lite and the Full version.

the differences between the Lite and the Full version.

not supported for synthesis

the differences between the Lite and the Full version.